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Surge driven evolution of Schottky barrier height on 4H-SiC JBS diodes

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Abstract. In this paper we will present the results of repetitive surge stress carried out on six 3.3 kV-5A Ti/Ni 4H-SiC JBS diodes. Repetitive current peaks between 10 A and 24 A have been applied and some diodes were able to endure 100,000 cycles while others failed before. The causes of failure have not been determined but a correlation between peak surge current and physical parameters evolution rate has been proven. Simulations show that contact temperature during surge can reach 300 °C, which is very close to Schottky contact annealing temperatures.

Introduction

4H-SiC Schottky/JBS diodes are already marketed and have shown good properties in static as well as in dynamic functioning [1]. The ruggedness of such devices seems to be achieved [2]. Nevertheless, understanding the degradation mechanisms induced by harsh operating conditions can give clues for further improvements to these diodes.

Repetitive surge is one of the tests which can put to stress these devices [3,4]. In order to apply repetitive surge cycles we developed an automated setup, that we will detail further in the test setup section. Performing the measurement between each predefined set of surge pulses allows us to plot the evolution of physical parameters (Φ , n).

Device Fabrication

Tested devices are 3.3 kV - 5 A JBS diodes. The fabrication process is carried out on 4" SiC wafer, on top of which 30 μm epitaxy is grown doped at 3×10^{15} atoms/ cm^3 of Nitrogen. Peripheral protection is ensured by a JTE of 400 μm length with a doping dose of 9.4×10^{12} atoms/ cm^2 of Aluminium achieved by ion beam implantation. 1.5 μm PECVD oxide is deposited on top of 30 nm of grown oxide as passivation layer. Then the wafers are annealed during 1 hour at 1100 °C. Backside ohmic contact is made of Ti/Ni annealed at 900 °C. Schottky metal is Ti/Ni annealed at 350°C by RTA. A layer of 18 μm of polyimide is deposited and annealed at 300 °C. At last dies are cut and packaged on an isolated TO-247 metallic case.

Test setup

Tested devices were stressed by repetitive voltage surge. In our case, surge conditions were 10 ms half-sine voltage pulses delivered periodically every second and inducing a peak current between 10 A and 24 A. Electrical and physical parameters were monitored after 1, 10, 100, 1.000, 10.000 and 100.000 pulses. These parameters are extracted from forward and a reverse HV characteristic measured with a Keithley 2410 Source Meter Unit (SMU) and a FUG 12,5kV Power Supply unit in series with a Keithley Pico-amperemeter respectively.

The test setup block diagram is illustrated in figure 1. A general purpose generator is connected to the surge amplifier in order to be able to deliver 10 ms half-sine of maximum 40 V peak voltage and

up to 50 A peak current. The voltage signal applied to the stressed device and the current passing through it are monitored with an Oscilloscope (Tektronix DPO 4032) and saved periodically. In order to alternate surge cycles with forward and reverse high voltage I(V) characterisation we developed a switch matrix that we can control depending on the cycling pattern we chose. The control sequence of the relays acting as switches depends on the state and is defined in table 1:

Table 1

Relay	1	2	3	4	5
Idle	off	off	of	ON	off
Surge Cycling	ON	off	ON	off	off
Forward I(V)	off	ON	ON	off	off
Reverse I(V)	off	off	off	off	ON

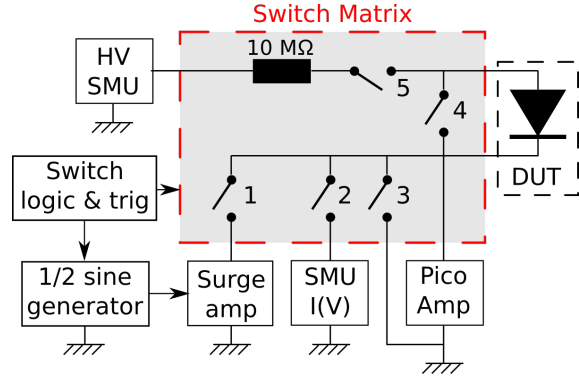


Fig. 1. The schematics of the surge setup.

Surge stress results

Several diodes that we tested were able to endure 100.000 cycles of surge pulses, whereas others failed before. Table 2 shows the peak current applied during surge stress and number of cycles endured by tested devices. We can see that similar components stressed at same peak current do not necessarily endure the same number of cycles, even though there is a correlation between relative evolution of physical parameters and peak current.

Forward and reverse characteristic of the devices were impacted by the surge process. Figure 2 shows an example of the evolution of the diode characteristic. All curves are shifted to the right because of surge stress. The same tendency can be observed for low voltages of the reverse characteristic.

Table 2

	IPeak (A)	Applied cycles to failure
HL6	10	100 000
HL8		≈ 2 000
AJ2	20	100 000
HL3		≈ 60 000
HL11	24	122
HL12		≈ 1 000

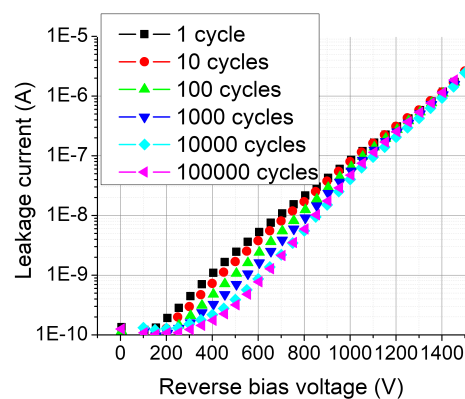
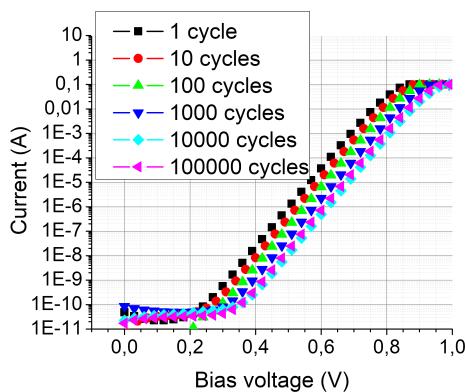


Fig. 2. Forward semi-log characteristic (left) and reverse characteristic (right) of AJ2 diode.

A correlation between the relative evolution of physical parameters and the peak current during stress is shown in figure 3. We can notice as well that the relationship between number of cycles and relative evolution of barrier height is logarithmic, whereas ideality factor does not respect any tendency. In fact, its evolution is relatively small and shows that the main conduction mechanism is

caused by thermionic emission. Since ideality factor is never higher than 1.1 we can state that during the stress process the Schottky contact quality is not altered. Nevertheless, the failure that occurs in some cases is unpredictable. Devices behave as an open circuit afterwards. Further structural analysis may help understand the degradation mechanisms taking place during surge stress.

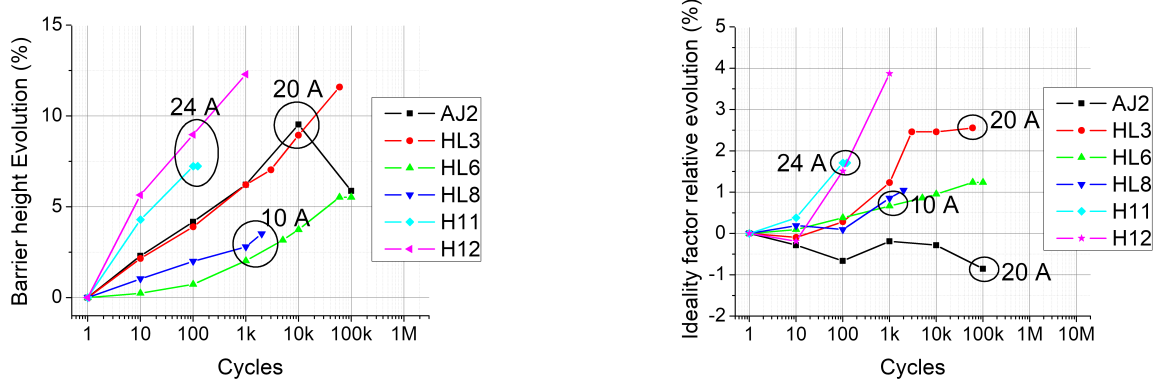


Fig. 3. Relative evolution of barrier height (left) and ideality factor due to surge stress (right).

Junction temperature estimation

We saw that surge stress test modifies the barrier height of our diodes, but we were not able to measure the junction's temperature during stress and analyse its impact. In order to estimate the average junction temperature, we built an electrothermal model shown in figure 4. As we can notice, we have an electric circuit related to a thermal circuit by its junction temperature T_j . The thermal dependence of the diode threshold voltage V_d is neglected compared to the dynamic resistance thermal behaviour. The latter is irrelevant in this case since the applied voltage during the surge event (up to 30V) is far greater than V_d .

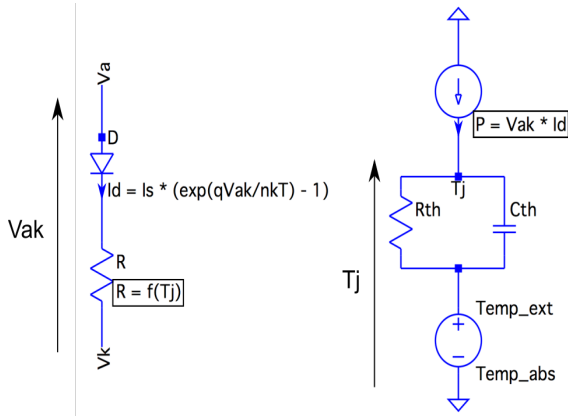


Fig. 4. Electrothermal model of the diode under surge stress.

The link between both parts of the model are the dependence of the electrical resistance on the junction temperature and the thermal resistance of the packaged device. The first was determined by forward $I(V,T)$ technique while the thermal impedance has been estimated by FEM simulation.

The forward $I(V,T)$ technique consists in measuring the pulsed forward characteristic of the diode at different temperatures going from RT to 200 °C and fitting the thermal dependence of the dynamic conductance. This gives us the equation (1) where the coefficients are $y_0 = 0.08 \pm 0.011$ S, $A_1 = 3.2 \pm 0.12$ S and $\tau = 164 \pm 8.5$ K.

$$R = \frac{1}{y_0 + A_1 \exp\left(-\frac{T}{\tau}\right)} \quad (1)$$

$$Z_{TH}(t) = R_{TH} - R_1 \exp\left(-\frac{t}{R_1 C_1}\right) - R_2 \exp\left(-\frac{t}{R_2 C_2}\right) - R_3 \exp\left(-\frac{t}{R_3 C_3}\right) \quad (2)$$

FEM simulations were carried out on AGROS2D [5] software led to the determination of thermal impedance of the packaged device. By extracting the simulated temperature for different durations of power dissipation we obtained the computed thermal impedance (2) as a function of time. Then, this numerical solution is fitted with a sum of 3 exponential functions taking into account the several thermal time constants of the device. It corresponds to a Foster RC network. The values obtained in our case are given in table 3.

Table 3

	R_1 (K/W)	C_1 (K/Ws)	R_2 (K/W)	C_2 (K/Ws)	R_3 (K/W)	C_3 (K/Ws)
Value	0.56	0.00325	0.689	0.00071	0.861	0.022

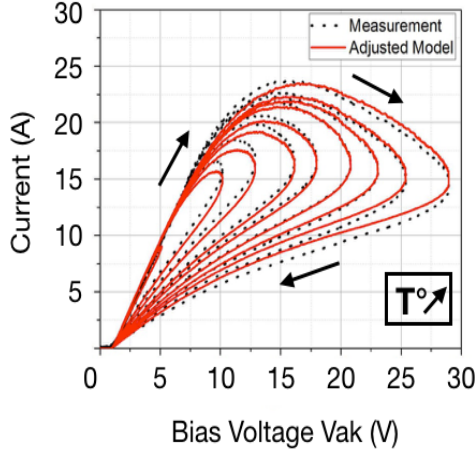


Fig. 5. Validation of electrothermal model.

Having obtained the expressions of dynamic resistance and thermal impedance it was possible to simulate the model in LTspice software, which after adjustments could be validated. Figure 5 shows the comparison between a measured and a simulated forward characteristic for different surge pulses. We can notice that increasing peak current of the surge pulse increases the resistance of the device because of the power dissipated in the device. With this model we estimated the average junction temperature of the Schottky contact during surge pulses as a function of time. We can see in figure 6 that for surge pulses higher than 20 A (~ 450 W dissipated power) the average junction temperature can reach 300°C. Considering this relatively high temperature and the surge duration, it is likely that the die attach (PbSn brazing) could have been degraded and thus failed.

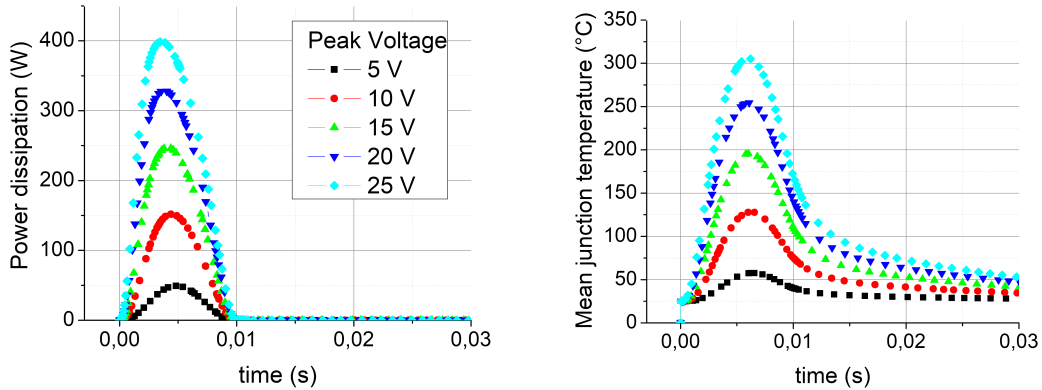


Fig. 6. Simulation of power dissipation in 3.3 kV-5A Ti/Ni 4H-SiC JBS diodes as a function of time (left), and the impact on the average junction temperature over time (right).

Conclusions

This study showed a correlation between peak surge current and relative evolution of physical parameters of 3.3 kV-5A Ti/Ni 4H-SiC JBS diodes. We noticed that some devices can endure 100.000 surge cycles whereas others fail unpredictably. This is probably related to the brazing layer alteration rather than device failure itself. Electrothermal modelling helped us estimate the average junction temperature of the Schottky contact and showed that in our test conditions temperature can grow up to 300 °C. Such high temperatures are used in RTA annealing of Schottky.

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