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A Chip-Interleaving Pattern Retaining Orthogonality In DS-CDMA Systems: Application To The Multicode Downlink

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***Abstract*— Interleaving the chip-level sequence resulting from spreading before transmission in direct spread code division multiple access (DS-CDMA) systems have been reported to allow significant improvements over conventional (non chip-interleaved) DS-CDMA. This transmission scheme has been shown to be of particular interest when used in conjunction with iterative receivers, allowing performance close to the multiple access (MAI) and intersymbol (ISI) interference-free case to be reached. This paper addresses the application of chip-interleaving to existing or near-future DS-CDMA systems. An interleaving pattern is introduced that allows the orthogonality property to be retained between interleaved and non-interleaved signals. In addition, a low-complexity receiver based on iterative channel equalization is designed for the multicode downlink of chip-interleaved DS-CDMA systems. Numerical simulations show that used in conjunction with the proposed interleaving scheme, the proposed receiver allows the interference-free performance of the non-interleaved case to be attained.**

I. Introduction

Interleaving the chip-level sequence resulting from spreading before transmission in direct spread code division multiple access (DS-CDMA) systems has been reported to allow significant improvements over conventional (non chip-interleaved) DS-CDMA [1] (and the references therein). This transmission scheme has been shown to be of particular interest when used in conjunction with iterative receivers, allowing performance close to the multiple access (MAI) and intersymbol interference-free case to be reached with tractable complexity.

However, the practical introduction of chip-interleaving into third generation (3G) DS-CDMA systems raises the problem of retaining the orthogonality between chip-interleaved (CI) and non-CI signals. The coexistence of both kinds of signals in practical systems, not addressed so far to our knowledge, is justified by (at least) the fact that interleaving all the signals in the system would create backward compatibility problems with older mobile terminals. As practical DS-CDMA systems rely on orthogonal spreading codes, performing chip-interleaving with any interleaving pattern would destroy the orthogonality between CI and non-CI signals. In this paper, a chip-interleaving pattern is designed which preserves the orthogonality between CI and non-CI signals, allowing chip-interleaving to be introduced into existing DS-CDMA systems without requiring excessive changes in the existing standards.

The remainder of this paper is organized as follows: section II introduces the proposed chip-interleaving scheme. In section III, we focus on the application of the proposed chip-interleaving to the multicode downlink, which deserves particular attention as it is the transmission scheme to be used for high data-rate downlink packet modes such as the High Speed Downlink Packet Access (HSDPA) in the UMTS standard [2]. In addition, a low-complexity receiver for the CI multicode downlink is proposed, which is a slightly modified version of the receiver introduced in [3]. Section IV shows that applying the orthogonality-preserving chip-interleaving in a simplified HSDPA context allows the performance of the conventional CDMA matched filter bound to be reached and even outperformed by the proposed receiver. Section V finally presents our conclusions.

II. Orthogonality preserving chip-interleaving schemes

The chip-interleaving process considered in this paper is designed to be used in the framework of 3G communication systems. It thus applies to a sequence $S_\pi = (s_{\pi,0}, \dots, s_{\pi,N-1})$ of N complex chips, resulting from the synchronous sum of K_π spread signals (which may belong to a same or different users, depending on whether we consider uplink or downlink transmission). The chip-interleaved sequence $S_\pi^\dagger$ is intended to be summed at the chip-rate with a conventional (non-CI) sequence $S_c = (s_{c,0}, \dots, s_{c,N-1})$, resulting from the synchronous sum of K_c spread signals, to give sequence S before the scrambling operation. The real and imaginary parts of the spread signals coming into S_c and S_π are obtained by spreading a sequence of real symbols by a signal-specific real valued Orthogonal Variable Spreading Factor (OVSF) code [4], that may be different (in pattern and/or spreading factor) along the real and imaginary parts. The various spread signals are assumed to be orthogonal to each other before chip-interleaving, which is the case if the corresponding spreading codes are chosen properly in the OVSF code tree [2, p. 91].

The aim of the chip-interleaver is to shuffle the chips of S_π within the transmission block. This section shows how the properties of the OVSF codes allow this task to be performed in a way that preserves the orthogonality between CI and non-CI signals, i.e. such that the correlations[1] 1) of $S_\pi^\dagger$ with the

[1]Throughout this section, the correlation of a chip sequence or a spreading code with another spreading code means implicitly that the latter is properly aligned on the time span of the spread symbol which would be desired.

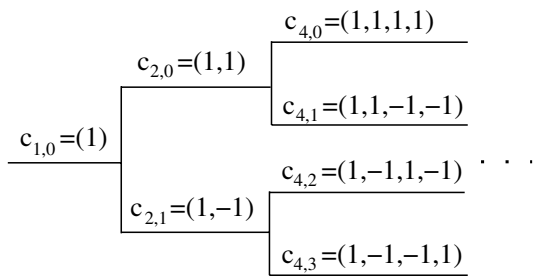

Fig. 1. The OVSF code tree up to spreading factor 4.

spreading code of a non-CI signal and 2) of the deinterleaved non-CI sequence with the spreading code of an interleaved signal remain zero.

The structure of the OVSF code tree is recalled in Fig. 1. The OVSF codes are denoted by $c_{P,n}$ where P is the spreading factor associated with the code and n indexes its position among the branches with length P in the code tree.

Two interleaving schemes are proposed, which can be combined in order to increase the chips shuffling.

A. Orthogonality retaining block-interleaving

This scheme makes use of the OVSF code properties that 1) a code $c_{L,n}$ is orthogonal to any code with the same spreading factor $c_{L,n' \neq n}$ and 2) the codes in the sub-tree originating from $c_{L,n}$ are built from sequences of $\pm c_{L,n}$ according to Fig. 1. Define $C_{L,n}$ the corresponding set of codes including $c_{L,n}$ and $C_{L,n}^{\perp}$ the set of the codes originating from and including branches $\{c_{L,m}, m \neq n\}$. Assume that the spreading codes coming into S_c and S_π belong to $C_{L,n}$ and $C_{L,n}^{\perp}$ respectively. Then if we write sequences S_c and S_π as $S_c = (B_c^0, \ldots, B_c^{M-1})$ and $S_\pi = (B_\pi^0, \ldots, B_\pi^{M-1})$ respectively, where $M = N/L$ and $B_x^n = \{s_{x,nL}, \ldots, s_{x,(n+1)L-1}\}$ with x in $\{c, \pi\}$, blocks B_π^i and B_c^j are orthogonal to each other for all i, j. Thus reordering the blocks B_π^n within S_π (B_c^n within S_c, respectively) still leads to a zero correlation with any code from $C_{L,n}$ ($C_{L,n}^{\perp}$, respectively).

Sequence S_π can then be chip-interleaved on a block-by-block basis with block size L in a way that retains orthogonality with the non-CI sequence S_c, provided the codes used to spread the signals coming into S_π and S_c belong to $C_{L,n}^{\perp}$ and $C_{L,n}$ respectively. Note that when both the real and imaginary parts are to be interleaved, this block-interleaving allows the real part of a block to be exchanged with the imaginary part of another block.

B. Orthogonality retaining chip-interleaving within the time span of an all-one code

This second scheme is based on two requirements: 1) the signals intended to be chip-interleaved are spread with spreading factors less than or equal to P_π, 2) the spreading codes allocated to the non-CI signals are chosen in the OVSF tree among the branches originating from the all-one code of length P_π, i.e. belong to $C_{P_\pi,0}$. Let $Q \geq P_\pi$ be the length of the smallest all-one sequence common to all the codes used to spread the non-CI signals. The principle behind this scheme is simple: interleaving a real chip sequence does not change the value of its cross-correlation with an all-one sequence of the same length. Then any interleaving pattern of size Q satisfying the two aforementioned requirements retains the orthogonality between CI and non-CI signals. This interleaving will be refered to in the following as intra-block interleaving.

III. The chip-interleaved multicode downlink

In this section, we focus on the application of the proposed chip-interleaving schemes to the multicode downlink, and present an efficient dedicated low-complexity receiver taking advantage of chip-interleaving.

A. System model

A packet-wise transmission for a multicode DS-CDMA downlink scenario is considered, inspired by the HSDPA standard [2]. The base station is assumed to transmit K high-rate data channels toward U users with K_u the number of channels allocated to user u, in addition to K_c low-rate common channels intended to be listened to by all users. Data and common channels are associated with spreading factor P_d and P_c respectively, each channel being spread by a specific OVSF code with unit norm. The desired user, assumed to be user 0, is transmitted in a packet $K_0 \times N_s$ high rate independent complex symbols $\{a_m^k, m = 0, \ldots, N_s - 1, k = 0, \ldots, K_0 - 1\}$ through K_0 high data-rate channels, as well as $K_c \times M_s$ low-rate independent complex symbols $\{b_m^k, m = 0, \ldots, M_s - 1, k = 0, \ldots, K_c - 1\}$ through the K_c common channels, each symbol belonging to the alphabet of a given modulation. After spreading by their respective code, the signals associated with the high rate channels from all users are summed at the chip-rate and the resulting signal is chip-interleaved within the packet. The interleaved chip sequence is then summed at the chip-rate with the spread signals associated with the common channels, before scrambling by a cell-specific long pseudo-random sequence. Define the chip-rate multiuser signal $\{d_n\}$ as the discrete-time resulting signal. Because of the pseudo-random scrambling sequence, the multiuser signal can be modeled as stationary, white and zero-mean with power σ_d^2. This multiuser signal is finally pulse-shaped and transmitted through a multipath channel. At the receiver end, the continuous received signal is filtered by a waveform-matched filter and sampled at the chip-rate to provide the discrete sequence $\{r_n\}$. The latter operations can be modeled by a discrete equivalent transmission channel $\mathbf{h} = [h_0, \ldots, h_{Lh}]^T$, which encompasses the effects of pulse shaping, multipath channel and reception filtering. The output of the transmission channel is corrupted by a complex additive white Gaussian noise w_n, with zero-mean and variance $\sigma_w^2 = 2N_0$, where N_0 is the single-sided power spectral density of the noise, that models both thermal noise and inter-cell interference.

B. A specific chip-interleaving pattern

Consider the case where all the codes associated with a given spreading factor P_d are reserved for high data-rate channels except code $c_{P_d,0}$, one of whose originating branches

gives the code used for a pilot channel. With the notations of section II, all the codes available to the system for transmitting lower data-rate signals with spreading factor $P_c \geq P_d$ then belong to $C_{P_d,0}$, which comprises $\frac{P_c}{P_d}$ codes with length P_c.

In order to maximize the interleaving efficiency, block chip-interleaving allowing exchanges between the real and imaginary parts may be performed first with block size L in $\{2,4,\ldots,P_d\}$; the resulting interleaved sequence may be subsequently interleaved within blocks of size Q in $\{P_d, 2P_d, ..,\}$. Such chip-interleaving patterns will be indexed as $CIP(L,Q)$. In order to satisfy the constraints defined in sections II-A and II-B, block interleaving implies limiting the number of available high rate codes to $P_d(1-\frac{1}{L})$, while intra-block interleaving reduces to $\frac{P_c}{Q}$ the number of codes with length P_c in $C_{P_d,0}$ usable by the system.

The HSDPA standard satisfies the above conditions with $P_d = 16$, thus enabling $CIP(16,16)$ to be performed without requiring any change in the code allocation strategy of the standard. However, it appears that this interleaving scheme is not sufficient to yield improved performance compared to the non-CI case. In the case where not all the 15 high rate codes are to be used by the system, it is then more valuable to perform block-interleaving with length $\{2,4,8\}$, which only leads to reducing the number of usable high data-rate codes to $\{8,12,14\}$ respectively.

C. Iterative equalization for the CI multicode downlink

In the downlink, multipaths generate inter-chip interference (ICI) between the chips of the composite multiuser signal, leading to MAI between the transmitted communication channels and inter-path interference for a single channel. Chip-rate channel equalization of the received multiuser signal [5] has proved to be an efficient method in combatting the detrimental effect of multipaths. The proposed receiver is based on iterative channel equalization and derives from the receiver introduced in [3]. Compared to the latter, the equalization process does not make use of channel decoding, the presence of chip-interleaving allowing spreading to be considered as an inner coding and the multipath channel as an outer coding according to the turbo principle [6]. Due to lack of space, the features of this receiver are only outlined in the following. The reader is invited to refer to [3] for a detailed description.

The proposed receiver can be implemented in a multistage fashion, the structure of one stage being depicted in Fig. 2. It involves a chip-rate equalizer that attempts to remove the ICI generated by the multipath channel using soft estimates of the multiuser chips provided by the previous stage.

1) The minimum unbiased MSE equalizer: The equalizer is made up of two linear filters: at stage (l), a forward filter $\mathbf{p}^{(l)}$ processes the received samples $\{r_n\}$ while a feedback filter $\mathbf{q}^{(l)}$ generates an estimate of the ICI from the multiuser chip soft estimates $\{\overline{d}_n^{(l-1)}\}$, subsequently subtracted from the output of filter $\mathbf{p}^{(l)}$ in order to deliver a refined estimate $\hat{d}_n^{(l)}$ of the current multiuser chip. In order to alleviate notation, the superscript (l) is omitted in the remainder of this paragraph. The vectors containing the impulse reponses of these filters are defined as $\mathbf{p} = [p_{-Lp1} \ldots p_0 \ldots p_{Lp2}]^T$ and $\mathbf{q} = [q_{-Lq1} \ldots q_0 \ldots q_{Lq2}]^T$, with length L_p and L_q respectively. If we call g_0 the bias coefficient affecting the contribution of the desired multiuser chip at the equalizer output, we show in [3] that the equalizer filters minimizing the unbiased MSE at the equalizer output $\overline{MSE} = E\left\{|\hat{d}_n - g_0 d_n|^2\right\}$ are given by

$$\begin{cases} \mathbf{p} = \lambda \left[(\sigma_d^2 - \sigma_{\overline{d}}^2)\mathbf{H}^H\mathbf{H} + \sigma_w^2\mathbf{I}\right]^{-1}\mathbf{H}^H\mathbf{e}_\Delta \\ \mathbf{q} = \mathbf{H}\mathbf{p} \quad \text{with } q_0 = 0,\ L_{q1} = L_{p1} \text{ and } L_q = L_h + L_p \end{cases} \tag{1}$$

where $\sigma_{\overline{d}}^2$ is the power of the multiuser chip soft estimates provided by the previous stage, $\mathbf{H}$ is the $(L_h+L_p)\times(L_p)$ lower triangular Toeplitz matrix with $[\mathbf{h}^T 0 \ldots 0]^T$ as the first column, $\mathbf{I}$ is the $L_p \times L_p$ identity matrix and $\mathbf{e}_\Delta$ is a null column-vector except its $\Delta+1$th coefficient equal to unity, where we set $\Delta \triangleq L_{p1}$. λ is a real scaling factor, strictly positive provided the noise power is non-zero, given by

$$\lambda = \left\{\mathbf{e}_\Delta^T\mathbf{H}\left[(\sigma_d^2 - \sigma_{\overline{d}}^2)\mathbf{H}^H\mathbf{H} + \sigma_w^2\mathbf{I}\right]^{-1}\mathbf{H}^H\mathbf{e}_\Delta\right\}^{-1} \tag{2}$$

under the constraint $g_0 = 1$. With the above equalizer filters, it can be shown that the unbiased MSE finally reduces to

$$\overline{MSE} = \lambda - (\sigma_d^2 - \sigma_{\overline{d}}^2). \tag{3}$$

At the first stage, no multiuser chip soft estimates are available, so $\sigma_{\overline{d}}^2 = 0$. Then filter $\mathbf{p}$ reduces to the impulse reponse of an MMSE linear equalizer scaled by a real positive factor, while filter $\mathbf{q}$ is unused. When all the active codes are known from the receiver and all the symbols are perfectly estimated, the multiuser chips are equal to their true value and $\sigma_{\overline{d}}^2 = \sigma_d^2$, leading to the forward and feedback filters of an MMSE ICI canceller scaled by a real positive factor, which removes all the ICI while providing channel-matched filtering. Between these two configurations, as well as when only partial knowledge about the active codes is available, the equalizer takes the form of a hybrid structure between the linear MMSE equalizer and the ICI canceller, which achieves the minimum unbiased MSE permitted by the available information. This equalizer has then the ability to evolve through the stages as a function of the reliability of the multiuser chip estimates, represented by $\sigma_{\overline{d}}^2$.

2) Soft estimation of the multiuser chips: The chip-rate signal output by the equalizer at stage l is processed according to Fig. 2, where Π and Π^{-1} represent the interleaving and deinterleaving operations respectively. Soft estimates on the despread symbols are obtained from a set of log likelihood ratios (LLRs) on the samples $\{\hat{a}_m^{k(l)}\}$ and $\{\hat{b}_m^{k(l)}\}$ yielded by the despreading operation along the various codes known from the receiver. Under a Gaussian assumption on the statistics of the interference contribution at the despreader output, the LLRs on the transmitted symbols are given in the QPSK case by

$$\begin{cases} L^{(l)}(\mathrm{Re}\{.\}) = 2\sqrt{2}g_0\mathrm{Re}\{.\}/\sigma_\eta^{2(l)} \\ L^{(l)}(\mathrm{Im}\{.\}) = 2\sqrt{2}g_0\mathrm{Im}\{.\}/\sigma_\eta^{2(l)} \end{cases} \tag{4}$$

where $(.)$ can be either $\hat{a}_m^{k(l)}$ or $\hat{b}_m^{k(l)}$, g_0 being the coefficient affecting the desired multiuser chip at the equalizer output. The

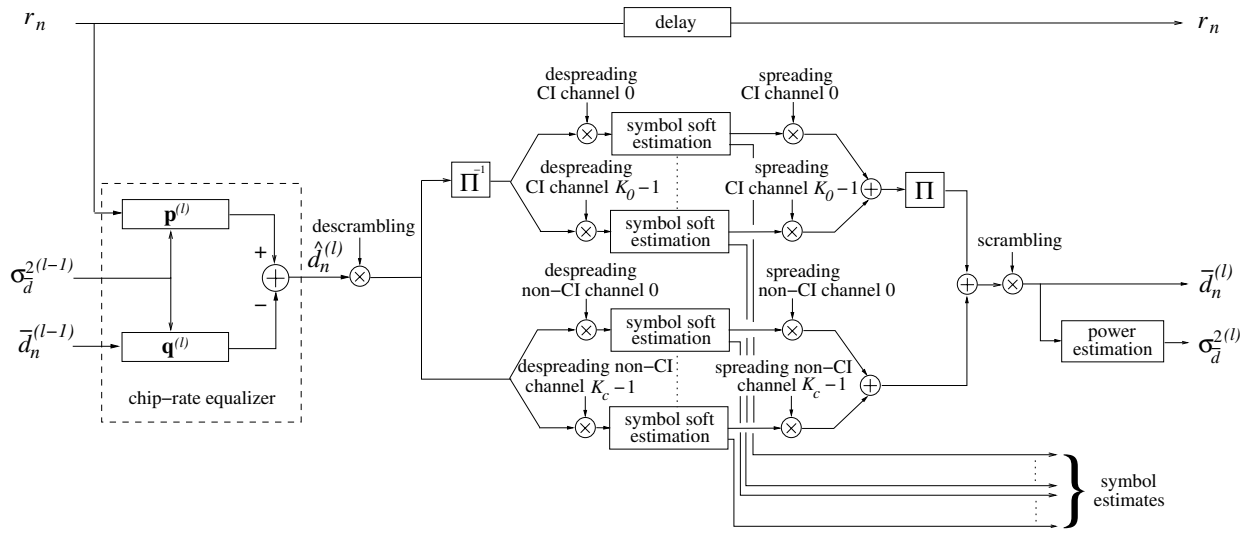

Fig. 2. The lth stage of the proposed receiver in the case of both CI and non-CI channels allocated to the user of interest.

variance $\sigma_\eta^{2(l)}$ of the interference term at any despreader output can be shown to be equal to the unbiased MSE on the multiuser chips at the equalizer output [3], which can be computed using (3). This set of LLRs, denoted as $\mathbf{L}^{(l)}$, represents the knowledge available to the receiver about the transmitted symbols after the estimation process of stage l. The complex symbol soft estimates are then defined as $\overline{a}_m^{k(l)} = E\{a_m^{k(l)}|\mathbf{L}^{(l)}\}$ and $\overline{b}_m^{k(l)} = E\{b_m^{k(l)}|\mathbf{L}^{(l)}\}$, which can be computed in the QPSK case according to

$$\begin{aligned}\overline{a}_m^{k(l)} = \Big(&\tanh\big[L^{(l)}\big(\mathrm{Re}\{\hat{a}_m^{k(l)}\}\big)/2\big] \\ &+ j.\tanh\big[L^{(l)}\big(\mathrm{Im}\{\hat{a}_m^{k(l)}\}\big)/2\big]\Big)/\sqrt{2},\end{aligned} \tag{5}$$

the sequence $\{\overline{b}_m^{k(l)}\}$ being obtained in the same way. The soft estimates on the complex symbols are then respread along their respective code, re-interleaved if necessary, summed at the chip-rate and scrambled in order to give the soft estimates on the multiuser chips $\{\overline{d}_n^{(l)}\}$. As the equalizer filters depend on the power $\sigma_{\overline{d}}^{2(l)}$, it may be estimated by a temporal mean over the sequence $\{\overline{d}_n^{(l)}\}$. Note that (5) implies the relation $\sigma_{\overline{d}}^{2(l)} \leq \sigma_d^2$, with equality when all the active codes are known from the receiver and the transmitted symbols are perfectly estimated, i.e. $\overline{a}_m^k = a_m^{k(l)}$ and $\overline{b}_m^k = b_m^{k(l)}$ for all k, m.

IV. Simulation results

The performance of the proposed receiver with various chip-interleaving patterns is evaluated by means of Monte-Carlo simulations of a non-coded CDMA downlink. The system parameters are chosen in accordance with the HSDPA standard [2]: the spreading factor of high data-rate channels is $P_d = 16$, the packet length is set to 7680 chips and the chip rate to $1/T_c = 3.84$ Mchips/s. Only QPSK modulation is employed. The user of interest, assumed to be alone in the system, is allocated $K = K_0 = 10$ high rate channels with equal power, while the number of common channels is set to 0 in order to assess the performance of the interleaving. The multipath channel is the time-varying ITU Vehicular A Rayleigh fading channel, which comprises 6 paths spanning 11 chip-durations whose delays were rounded to the closest T_c multiple. The speed of the mobile user is 120 km/h unless otherwise stated. We assumed the receiver had perfect knowledge of the channel delays. Path amplitudes were supplied by sampling the true amplitudes every 160 chips, which corresponds to $160.B_D.T_c = 9.10^{-3}$, with B_D the Doppler spread. The total transmitted power σ_d^2 as well as the noise power σ_w^2 are assumed to be known in order to compute the optimal equalizer filters (1). The results presented here should consequently be seen as lower bounds for the receiver performance. The latter was implemented with four stages. The length of filter $\mathbf{p}$ was set to $L_p = 51$ complex coefficients while filter $\mathbf{q}$ comprised the optimal number of coefficients $L_q = L_p + L_h$ where $L_h = 10$.

The results are presented in terms of bit error rate (BER) with respect to E_b/N_0, where E_b is the energy per bit of the user of interest. The matched filter (MF) bound was obtained by setting the proposed receiver to its ICI canceller mode and feeding filter $\mathbf{q}$ with the true multiuser chips.

Several types of chip-interleaving pattern $CIP(L,Q)$ defined according to section III-B were considered, a different realization of each pattern being generated randomly for each point in the curves presented. Each pattern used the block-wise real and imaginary part exchange enabled by block-interleaving.

Fig. 3 shows the performance of the proposed receiver as a function of the number of stages with $CIP(4,16)$. It can be seen that only three stages are needed to reach a steady state performance level, which outperforms the conventional MF bound for $E_b/N_0 \geq 9$. Note however that adding a non-CI channel could degrade the receiver performance in spite of the orthogonality between CI and non-CI signals, in the sense that the possibly lower reliability of the soft estimates on the symbols carried by non-CI channels would influence the power $\sigma_{\overline{d}}^2$ and then the impulse response of the equalizer

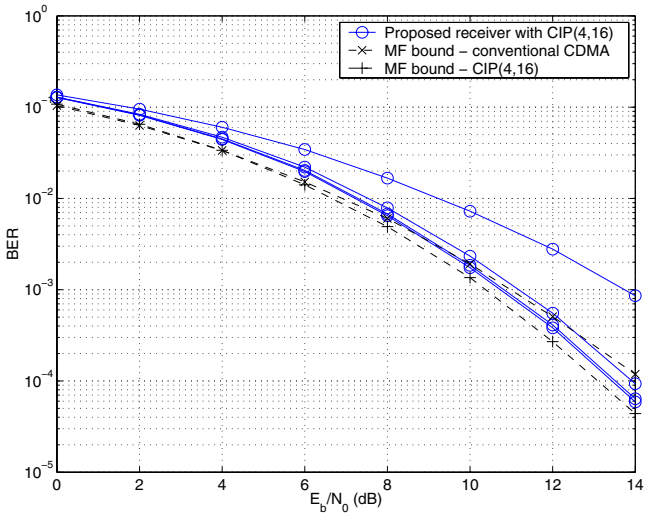

Fig. 3. Performance of the proposed receiver with $CIP(4,16)$ for 1,2,3 and 4 stages respectively.

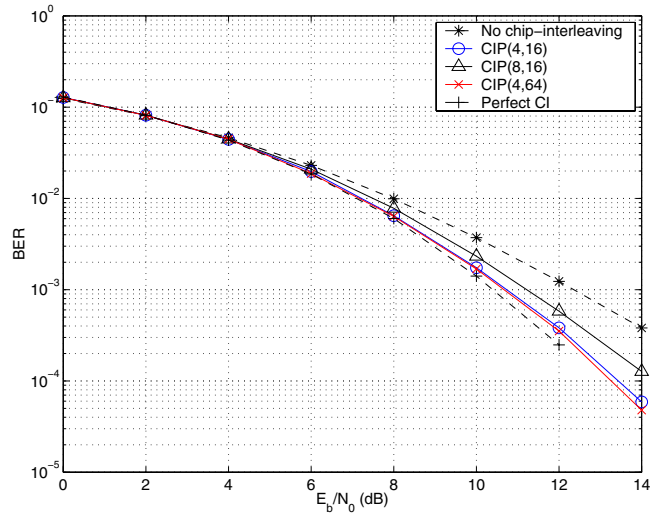

Fig. 4. Performance reached at the last stage by the proposed receiver with different interleaving schemes.

filters. Nevertheless, the degradation is expected to be weak as most of the downlink power should be allocated to the high data-rate channels.

Various interleaving patterns are compared in Fig. 4, perfect CI designating a random shuffling (including permutations between real and imaginary parts) of the chips within the time span of the whole packet without orthogonality-preserving constraint. It can be seen that $CIP(4,16)$ allows a 2 dB gain at a BER of 10^{-3} compared with the non-CI case, while the loss with respect to perfect interleaving is only 0.3 dB. The very small difference between the performance of $CIP(4,16)$ and $CIP(4,64)$ suggests that the intra-block interleaving is hardly involved in the interleaving gain. Finally, it can be seen that $CIP(8,16)$ allows the proposed receiver to almost reach the performance of the conventional MF bound, while enabling 14 high rate codes on 15 to be used by the system.

Simulations (not presented here) of a Vehicular A channel without Doppler spread (i.e. with an independent channel realization for each packet but not time-varying within a packet) have shown that the gain yielded by $CIP(4,16)$ compared to the non-CI case reduces to 0.6 dB at a BER of 10^{-3}. This suggests that the large gain in Fig. 4 originates mostly from the diversity gained by interleaving with respect to the channel conditions. However, particular realizations of the channel can still generate important differences between the CI and non-CI cases, as illustrated in Fig. 5. This gain can be explained by the fact that the noise and ICI samples processed by the code-matched filter after deinterleaving are statistically white, and that such a matched filtering is optimal in the presence of white interference.

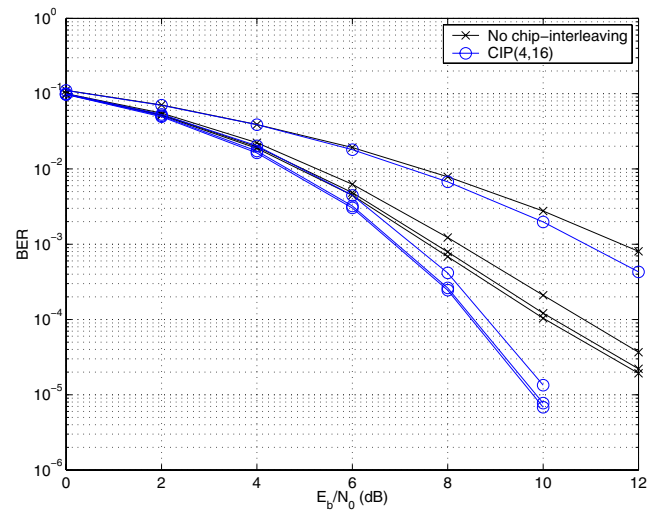

Fig. 5. Comparison of the proposed receiver performance with and without chip-interleaving for a particular realization of Vehicular A channel.

V. Conclusion

The proposed interleaving scheme allows chip-interleaving to be introduced into existing DS-CDMA systems at the expense of constraints on the number of spreading codes available to the system, as well as a potential reorganization in their distribution between the physical channels. Although studied in this paper in the context of the multicode downlink, this chip-interleaving may be applied in various other situations.

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