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## Real-time turbo-equalization on the TMS320C5509 – Improving the reliability of broadband wireless links

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### Introduction

Digital transmission over wireless links will typically encounter two major impediments to reliable communications, namely *additive noise* and *intersymbol interference* (ISI). Additive noise is a phenomenon of all practical transmission systems and is usually mitigated through the use of *channel coding* techniques, which add redundancy to the information message and thereby provide the receiver with the ability to detect and/or correct errors. ISI results from some form of time dispersion over the transmission medium. It arises when successive transmitted symbols are smeared in time and thus overlap at the receiver input up to the point that they may be no longer distinguishable as distinct pulses. Over radio links, this time dispersion is the natural consequence of multi-path propagation where the transmitted signal is received after it reflects off buildings or other obstacles. From a frequency domain perspective, the channel transfer function then exhibits frequency-dependent attenuations and delays over the transmission bandwidth, hence the alternative name *frequency-selective* channels (figure 1).

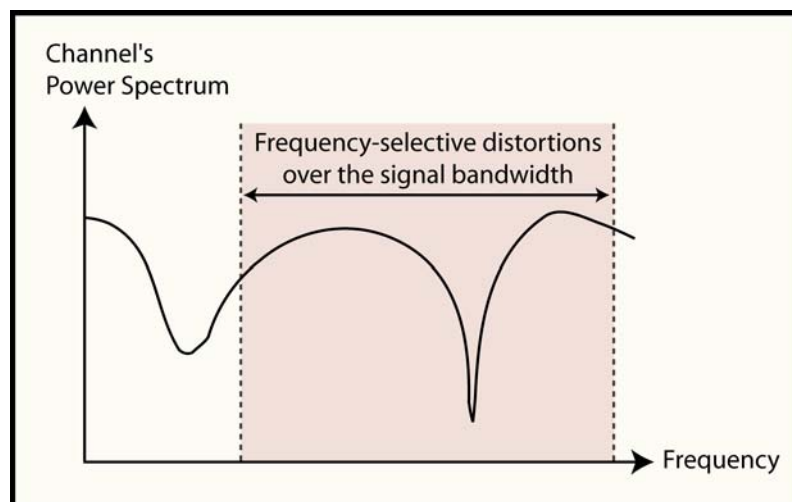


Figure 1: Frequency response of a typical ISI channel

The impairments caused by ISI are greater when successive symbols are spaced more closely in time in order to increase the data rate, and when the bandwidth restrictions become more stringent. The effects of ISI may be so large in some pathological channel conditions as to preclude reliable transmission even in the

absence of noise. Considering, for example, the recently approved IEEE 802.16a standard for wireless metropolitan area networks, specially designed to operate in non line-of-sight propagation's conditions, it is not uncommon to encounter highly dispersive channels exhibiting delay spreads that span up to a hundred symbol periods. Appropriate signal processing is then required at the receiver side to combat the distortion caused by ISI. Multicarrier modulation, such as *Orthogonal Frequency Division Multiplexing* (OFDM), is a well-established technology to eliminate transmission problems with multipath propagation. However, we focus here on the more traditional approach which combines single-carrier transmission with *equalization* at the receiver unit, a solution dating back to the early days of digital communication. The equalization process may be understood in the broad sense as an attempt to compensate for channel distortions.

**Combining equalization and decoding**

To be more specific, let us consider the basic transmitter configuration shown at the top of figure 2. Source bits go first through a channel encoder (a convolutional encoder, for instance) which adds redundancy to the transmitted message. The resulting coded message is then interleaved at bit level, and finally modulated for passband transmission over a frequency-selective channel.

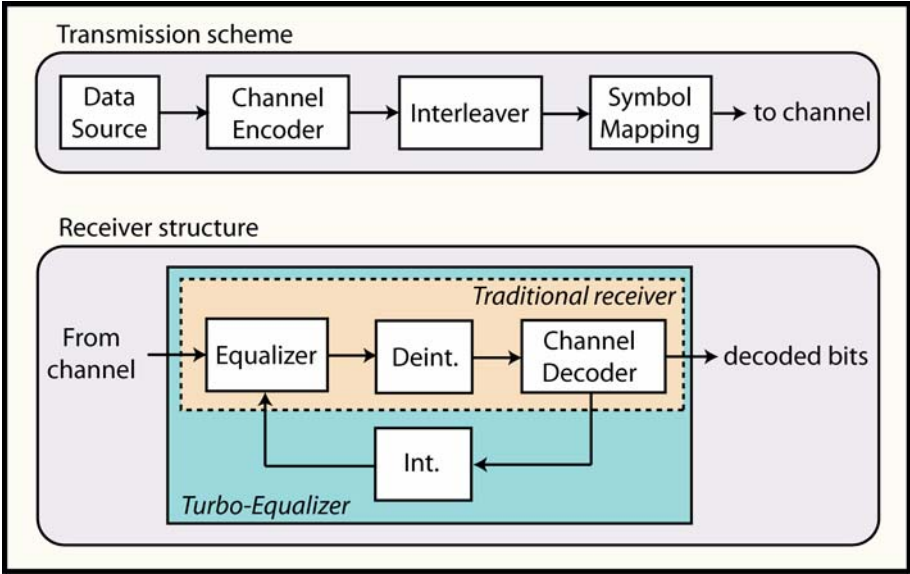


Figure 2: Block diagram of the overall transmission scheme

We now turn our attention to the receiver design. In the presence of channel coding at the transmitter, it seems intuitively desirable to take advantage of the error-correction capability (the so-called *coding gain*) offered by the code redundancy in order to improve the equalization process. Classical estimation theory tells us that the optimal receiver minimizing the bit-error rate (BER) should then perform equalization and decoding in a joint manner, by taking simultaneously the constraints imposed by the code, the interleaver and the ISI channel. However, the resulting receiver is known to be intractable in practice since its complexity grows exponentially with

message length. Hence, communication system designers usually resort to a suboptimal but nonetheless more practical two-stage approach where equalization and decoding are performed separately (as done, for example, in GSM mobile phones). A major breakthrough occurred in 1995 with the pioneering work of Douillard *et al* on *Turbo-Equalization* [1]. The turbo-equalizer establishes an *iterative* exchange of probabilistic “*soft*” information between the equalizer and decoder, so that each function benefits from the result of the other task (figure 2). The resulting iterative receiver has been shown to significantly outperform the previous approach, while maintaining a reasonable complexity with respect to the optimal solution.

Turbo-equalization is a receiver structure that has evolved over almost a decade of academic research into a mature technology with remarkable performance gains over conventional systems, and for which we now foresee practical applications. The remainder of this article focuses on the real-time implementation of a so-called *Minimum Mean-Square Error* (MMSE) turbo-equalizer on a Texas Instruments TMS320VC5509 device, a low-cost 16-bit fixed-point DSP typically targeted towards embedded communication applications such as signal processing for mobile handsets. This work was conducted as a proof of concept, driven by the desire to demonstrate that such receivers can be realized in practice with current software / hardware capabilities.

### **The considered turbo-equalizer**

The turbo-equalizer is shown in figure 2 and essentially consists of two main building blocks, a *Soft-Input Soft-Output* (SISO) equalizer and a SISO channel decoder, separated by a pair of interleaving / deinterleaving functions. Starting with the received signal, the SISO equalizer delivers *soft decisions* about the transmitted coded bits. A soft decision may be viewed as a real (or quantized) number whose sign gives the hard decision about the bit, and whose magnitude measures the reliability of the decision – a high magnitude meaning a high probability of correct decision. These soft decisions are deinterleaved and sent to the SISO decoder input. On the basis of this information, the decoder then delivers hard decisions on the information message, as well as updated soft decisions on the coded bits. The latter are then interleaved and fed back to the equalizer where they are exploited as a *priori* information for a new equalization attempt. Iterating the process a few times usually yields remarkable performance gains.

The SISO equalizer considered in this paper is called an *MMSE Interference Canceller – Linear Equalizer* (MMSE IC-LE). It generalizes the conventional MMSE linear equalizer by exploiting the reliability of a *priori* information available from the decoder to adapt the equalization strategy accordingly. Specifically, the IC-LE reduces to an MMSE linear equalizer in the absence of particular prior information about the coded bits. In contrast, it switches towards an ideal interference canceller when supplied with perfect *a priori* information. The latter structure theoretically eliminates all ISI *without noise enhancement*. The MMSE IC-LE comprises three processing functions, as shown in figure 3. The soft mapper first generates soft estimates about the transmitted symbols from the soft decisions delivered by the decoder. These estimates then enter an interference cancellation structure, together with the received distorted signal samples. The interference canceller is made up of

two transversal finite impulse response (FIR) filters whose outputs are subtracted to yield the equalized signal. Finally, the SISO demapper produces updated soft decisions about the coded bits from the equalized samples available at the canceller output. The MMSE IC-LE maintains a reasonable complexity that grows essentially linearly with the dimension of the signal set and the number of interfering symbols. Hence, this SISO equalizer appears as an attractive candidate for single-carrier broadband wireless transmissions in severe multipath environments and, furthermore, seems suitable for a practical implementation. A full description of the MMSE IC-LE is available in [2].

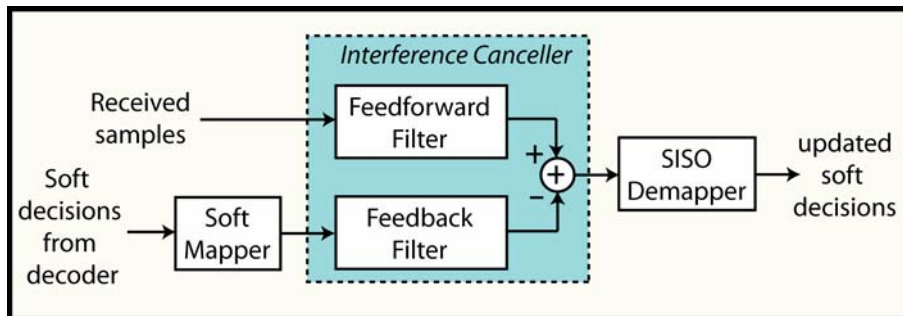


Figure 3: The MMSE Interference Canceller – Linear Equalizer (IC-LE)

### The demonstration platform

The demonstration platform is composed of a host PC communicating with a target DSP evaluation module, as depicted in figure 4. The host PC runs a monitoring application which is responsible for the tasks of configuring the transmission link and the DSP board, generating test data at the channel output, sending the resulting signal to the DSP that implements the turbo-equalizer, retrieving the processed data and updating the link metrology (bit-error rate and signal constellation monitoring). The DSP board is a stand-alone evaluation card from Spectrum Digital, Inc. It features in particular a Texas Instruments TMS320VC5509 DSP operating at 120 MHz (240 MIPS), 128 Kwords of on-chip memory, and 4 Mwords of on-board DRAM memory. Communication between the DSP board and the host PC relies on Texas Instruments *Real-Time Data eXchange* (RTDX) technology. RTDX allows non intrusive data transfers between host and target, with data rates typically ranging from 30 to 50 Kbit/s, the latest improvement (*High-Speed RTDX*) offering up to 2 Mbit/s.

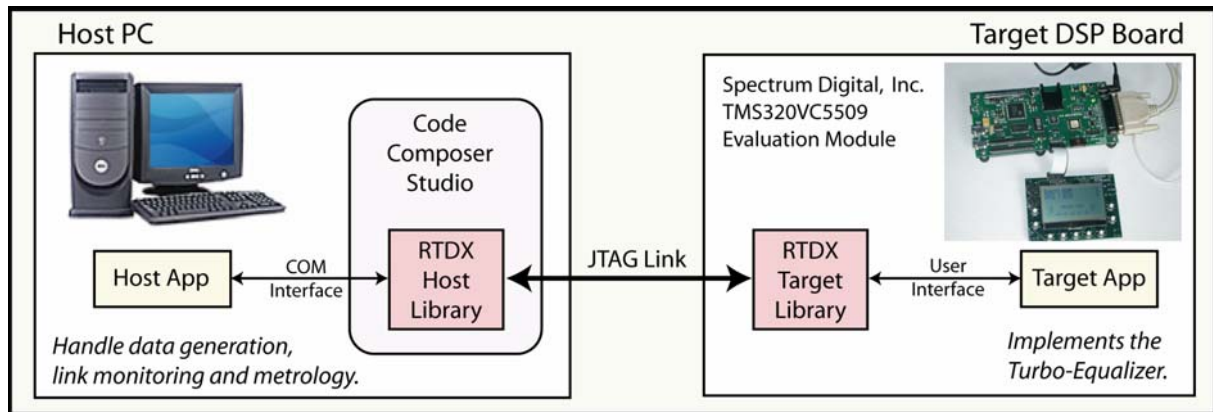


Figure 4: Overview of the demonstration platform

## Receiver implementation

The turbo-equalizer has been designed to operate with signal to noise ratio values in the 0...20 dB range, over channels with delay spreads spanning at most 16 symbol periods. Perfect knowledge of the channel impulse response and noise variance was assumed. We have chosen to implement the turbo-equalizer using the C language in order to speed up the development process and favor code portability. However, the equalizer implementation takes advantage of the assembly hand-optimized functions provided by Texas Instruments Digital Signal Processing Library (DSPLIB) whenever possible, so as to remain compatible with real-time constraints. Data quantization was carefully optimized at each stage of the receiver in order to maintain the highest possible precision while avoiding underflows or overflows resulting from the use of 16-bit fixed point arithmetic. Preliminary simulations were performed with a floating-point C model of the receiver in order to find the proper number of bits required to accurately represent the quantities involved in the iterative process. Additional details about the implementation of the SISO equalizer and decoder can be found in [2].

## Experimental performance

The performance of the aforementioned receiver was evaluated in the context of a simple transmission scenario relying on a rate- $\frac{1}{2}$  4-states convolutional encoder followed by a precomputed pseudo-random interleaving function and a *Quadrature Phase Shift Keying* (QPSK) modulator. Several channel models were investigated, including the class of *quasi-static* channels whose impulse response varies between successive transmitted data bursts.

Our measurements showed that the DSP receiver is able to operate with a maximum rate of 207 Kbit/s per iteration, or equivalently, 41 Kbit/s for 5 iterations. Additional studies demonstrated that the SISO equalizer and decoder account for 53% and 43% of the running time per iteration respectively. We ought to mention that the latter function may benefit from assembly language optimizations by taking advantage of the dedicated Add-Compare-Select instructions provided by the C55x DSP family. The resulting implementation has a code size of 3747 words (1 word accounting for



16 bits) and uses 10118 words of data. These values are fully compatible with the 32 Kwords of on-chip dual-access RAM (DARAM) available on the C5509.

In order to evaluate the performance loss caused by data quantization, comparative simulations were conducted both with the DSP demonstration platform and with an ideal (unquantized) floating-point C implementation of the turbo-equalizer. Bit-error rate measurements showed that our fixed-point DSP turbo-equalizer exhibits virtually no performance degradation in comparison with the floating-point receiver. These results were further confirmed by additional simulations over other channel models.

Finally, figure 5 graphically depicts the performance improvement offered by the turbo-equalization process during the iterations. The image *Lenna* was transmitted over a severe-ISI channel at a signal-to-noise ratio of 9 dB. It is worth noting that a conventional receiver implementing one-time equalization and decoding (iteration #1) only achieves a moderate bit-error rate of  $1.1 \cdot 10^{-1}$ . In contrast, the image is decoded error-free at the fifth iteration with our DSP prototype.

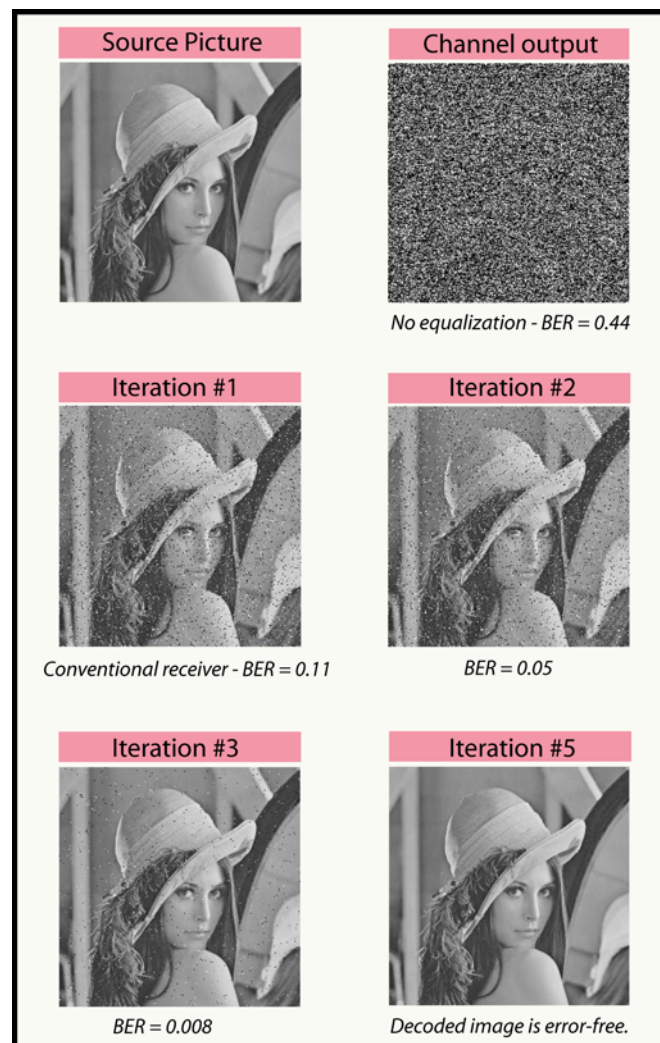


Figure 5: Illustration of the performance improvement offered by turbo-equalization

## Perspectives

This work has demonstrated the possibility of implementing advanced receiver structures in practice, such as low-complexity turbo-equalizers, on mobile terminals. Future work will include rewriting critical code sections in optimized assembly language and adding support for higher-order signal sets, such as *Quadrature Amplitude Modulation* (QAM). This project also constitutes the first step towards the realization of an FPGA prototype able to operate at data rates compatible with the requirements of broadband wireless transmissions, i.e. several Mbit/s. A flexible solution in this context could involve realizing the computation of the equalizer's coefficients on a general purpose DSP core, and then performing the costly filtering operations directly in hardware. The DSP core may then include other modem functions as well.

## Acknowledgments

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## References

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## About the authors

Raphaël Le Bidan, Christophe Laot, Dominique Leroux and Annie Godet are associate professors at ENST Bretagne, Signal & Communications Lab., Brest, France. Their research interests encompass both theoretical aspects and the practical implementation of digital communication systems and related signal processing algorithms.