Design of an integrated power converter in Wide Band Gap for harsh environments

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Abstract

AMPERE laboratory (Lyon, France) and Center National Microelectronics of Barcelona (SPAIN) have recently developed lateral MESFETs in SiC. The current purpose is to develop electronic systems based on these MESFETs for applications operating in harsh environments (e.g : High Temperature > 300°C). This paper presents the design of an integrated power converter with its driver in SiC and the characterisation of elementary functions.

1 Introduction

The emergence of SiC power devices (BJT, JFET, Thyristor) allows to consider the design of high power converters able to operate in harsh environment especially at very high voltages (>10kV) and high temperatures (>300°C). The driving circuitry converters doesn't exist in this temperature range. The development of basic electronic functions in SiC (comparator, oscillator...) is a preliminary step to conceive a full driver demonstrator.
Several laboratories have developed elementary functions, based on either JFET [1], BJT [2] or MOSFET [3] devices. High temperature operations have been reported (up to 500°C for hundreds hours).
However theses developments have mostly been focused on the design of “logic functions” and not on integrated power converters.

Ampere and CNM laboratories have fabricated elementary dual-gate SiC MESFET. The methodology is now detailed:
- the determination of simulation models in order to establish a “design-kit” of SiC components,
- the conception of analog electronic functions,
- the design and fabrication of an integrated power converter composed of both power switches and logic control circuitry,
- the evaluation of performances and limitations of the demonstrator by means of simulations and experimental characterizations.

After the presentation of the devices layout, a spice model determination is presented and the elementary functions described. An experimental analysis of a ring-oscillator is detailed, and simulation results of the integrated power converter based on SiC dual-gate MESFETs are presented.

2 Topology of lateral double-gate MESFET

Lateral SiC-MESFETs have been fabricated (figure 1) at CNM of Barcelona [4] [5]. These components have a dual-gate (gate (schottky) and body (pn)), which enable to consider new ways of controlling power switches. These MESFETs width channels is varying from 2 µm to 4 µm. The insulation of each component is made either by a “box” P+ on the sides and semi-insulating at the bottom or deep etching down-to the semi-insulating substrate. Semi-insulating substrates have been used in order to reduce bulk leakage current. A 5 µm tick P-type epilayer has been grown on-top of the SI-substrate in order to act as a RESURF depletion layer to improve the blocking voltage of the dual-gate MESFETs. Maximum blocking voltage is also tunable adjusting gate-drain dimension (V_{MAX} < 300V). As a first step, standard metallization process (operating as high as 200°C) has been implemented.

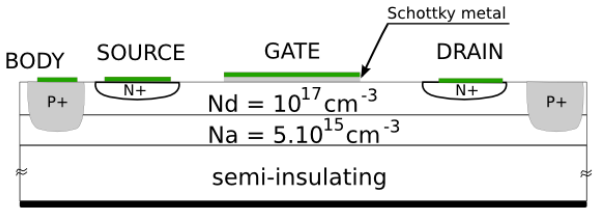

Figure 1 Cross section of the elementary SiC dual-gate MESFET

3 SPICE modeling of the dual-gate SiC MESFET

3.1 Static model

From static SiC-MESFET characterizations, a SPICE model has been developed. This is an empiric model

based on the JFET equations, which doesn't consider the buried gate feature. In static mode ($I_{DS} = f(V_{DS})$), this model presents a relatively good correspondence in saturated region (as inferred in figure 2) and can be use for simulating the behaviour of MESFETs in this mode.

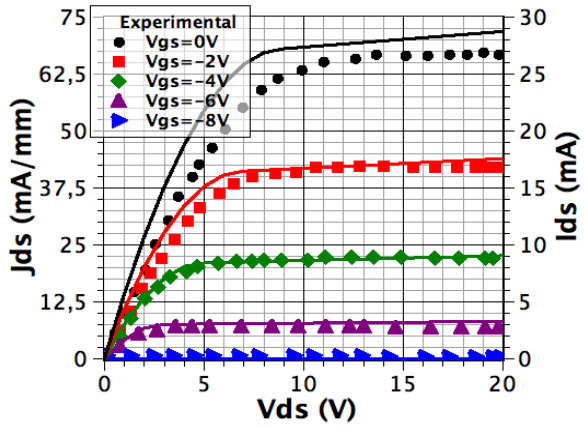

Figure 2 Comparison between simulated (lines) and experimental (symbols) static characteristics of an elementary MESFET. V_{GS} = -2V steps.

3.2 Dynamic model

In order to simulate the dynamic behaviour of the SiC MESFET, it is necessary to estimate the value of the inter-electrodes capacitances C_{GD} and C_{GS}. An HP 4194 has been used to extract those parameters.
Switching RL measurements using circuit shown in figure 3 have been performed to check the accuracy of the dynamic MESFET model. The comparison of both measurements and simulation is shown in figure 4.

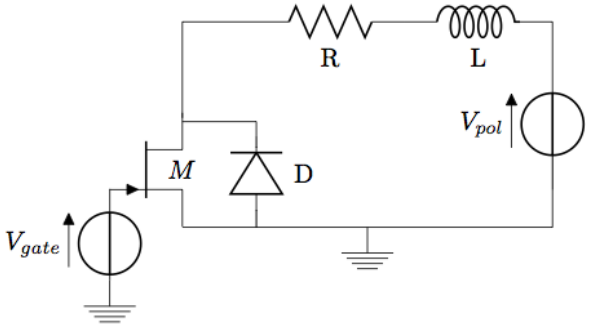

Figure 3 RL circuit used for dynamic characterisation.

The correspondence between the simulation and the measurements is relatively good in-on state and for the first over-voltage oscillation, and slightly different in off-state.The origin of the mismatch can be due to the approximations of the circuit model and to the the fact that the SPICE model doesn't allow to model properly the voltage dependence of internal capacitance.

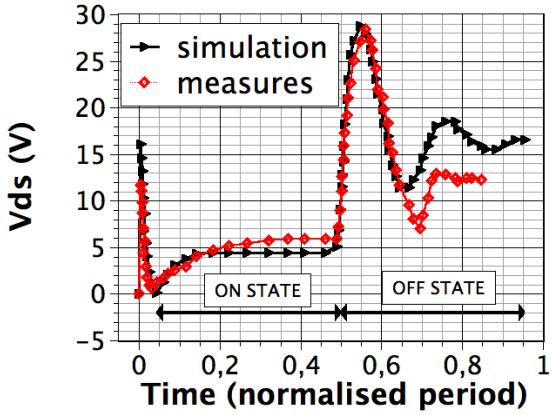

Figure 4 Comparison between simulated and measured characteristics (switching on an RL load (R : 1.1kOhm – L : 620 µH)). (MESFET parameters : C_{GS} = 5pF, C_{GD} = 3pF)

Even with approximated capacitor values, this model is relatively suitable to analyse the behaviour of this component and elementary functions and has been used to establish the DG-MESFETs functions "library".

4 Design of elementary functions using dual-gate SiC MESFETs.

For a functional approach, elementary blocks based on the model have been developed. This work was not straightforward because only normally-on n-type MESFETs are available. These constraints implies to rethink the topology of each function.

4.1 Theoretical design of elementary functions

Using the simulation model, numerous electronic functions (table 1) have been designed.

Common source amplifier	**Comparator**
Differential pair	Level-shifter
Logical gates (Nor-Nand)	Push-pull
Ring oscillator	**Schmitt Trigger**

Table 1 Summary of elementary functions optimized using the SPICE MESFET model.

4.1.1 The comparator

The topology of a comparator based on MESFETs (figure 5) implies that the gate voltages V_{IN} and V_{REF} are negative. The circuit is not appropriate for the comparison of positive voltages and implies to use intermediary circuits like level-shifter to translate the voltages on a range of specific polarization.

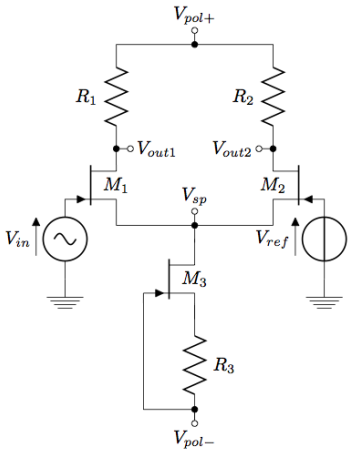

Figure 5 Comparator based on 3 SiC MESFETs

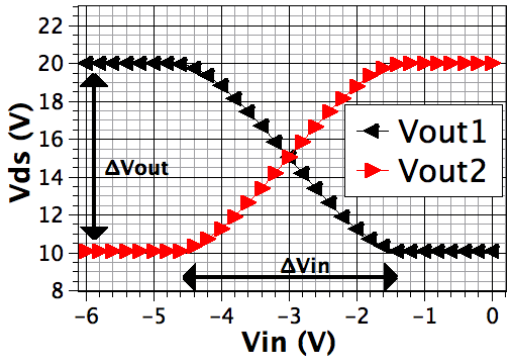

Figure 6 Simulated transfer function $V_{DS} = f(V_{IN})$ of the comparator for V_{REF} = -3V (figure 5).

The transfer function $V_{DS} = f(V_{IN})$ has been simulated (figure 6). This figure shows the particular voltage, when V_{IN} is equal to V_{REF} (-3V). For this value, M1 and M2 have identical drain currents ($R_1 = R_2$). Consequently V_{OUT1} and V_{OUT2} have the same level. This feature allows to know the input voltages to apply at the circuit. For example, if V_{IN} is a sine wave signal (V_{POL} : -3V, amplitude : $\Delta V_{IN}/2$, freq : 300kHz). The output signals (V_{OUT1} and V_{OUT2}) will be square wave signals with ΔV_{OUT} amplitude of 10V and a 50% duty cycle.

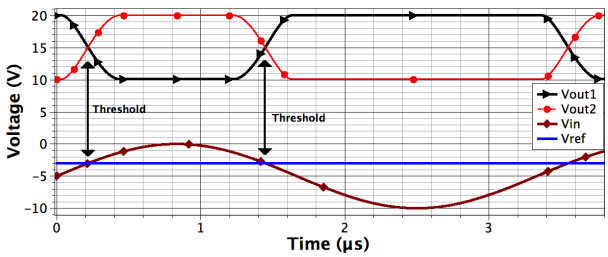

Figure 7 SPICE simulation showing evolution of the comparator's voltages for V_{REF} = -3V

This topology could be conveniently used as a pulse width generator with a tunable duty cycle.

4.1.2 The Schmitt trigger

A Schmitt trigger (figure 8) has been designed from the comparator circuit (figure 5). The output V_{OUT1} (figure 5) has been connected to the gate of the MESFET M2 (instead V_{REF}). This connection is a positive feedback, which allows to get a comparator with 2 thresholds commonly known as Schmitt trigger. The threshold trigger conditions have been set at V_{TH}-=-5.95V and V_{TH}+=-3.90V from the bias resistance R_{TH1} and R_{TH2}.

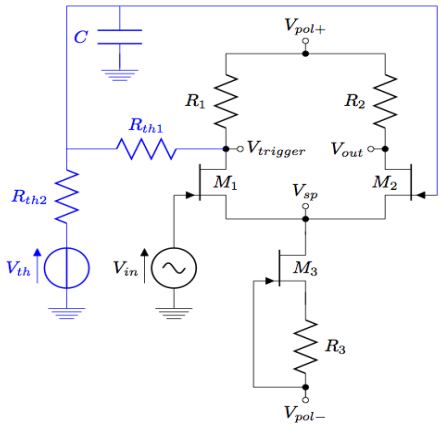

Figure 8 Schmitt trigger schematic

Schmitt trigger circuit transfer function simulation (figure 9) is illustrating the matching of the hysteresis switches bias with the theoretical thresholds (V_{TH}+ and V_{TH}-). The addition of the external capacitor C (figure 8) allows to adjust the value of the hysteresis threshold voltage ΔVth as shown in figure 9.

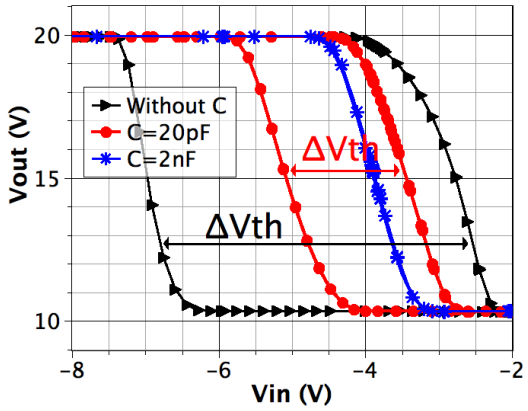

Figure 9 SPICE simulation of the transfer function ($V_{OUT} = f(V_{IN})$) for different values of the capacities C giving Kp = Dvout/Dvin = 10 with tunable input saturation thresholds levels.

Such a function is useful for thresholds detection implementation of the output voltage regulation of a converter for example. The additional capacitor C "convert" the circuit into a proportional corrector with tunable input thresholds levels and feedback error voltage average integration (figure 9, C = 2nF).

4.1.3 Ring oscillator

A ring oscillator is composed of several transistors connected in cascade, where the output of the last transistor is connected to the input of the previous one. A structure based on 3 SiC MESFETs has been designed to oscillate at 1MHz (figure 10). The determination of the oscillation frequency is based on the static spice model and the approximated dynamic model of the DG-MESFETs.

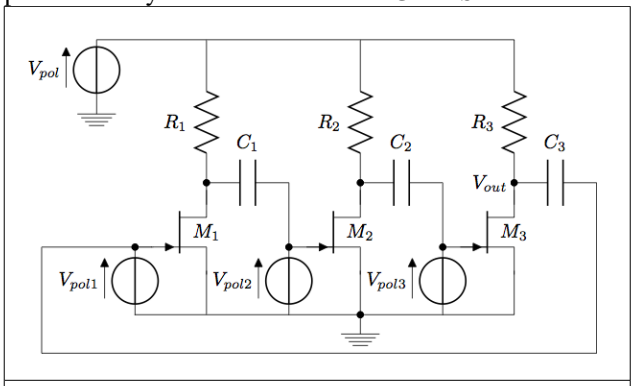

Figure 10 Ring oscillator based on 3 MESFETs Ri = 18kΩ; Ci = 33nF)

The oscillation frequency and the parameters circuit values (R, C, W/L) of the circuit has been checked in simulations (figure 11). The SPICE simulation shows the presence of harmonics, that shouldn't disturb the circuit because the peak magnitudes are more than 12 dB lower than the fundamental (figure 11).

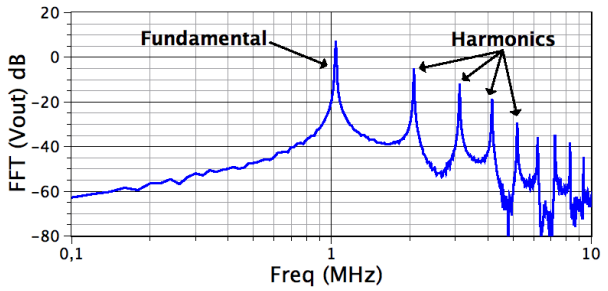

Figure 11 SPICE simulated FFT of the ring oscillator

Different elementary functions have been designed and both static and dynamic behaviour were investigated.

4.2 Experimental verifications

Different functions have been tested successfully (differential amplifier, comparator, push-pull stage …). The figure 12 is presenting a microscope view of those functions and the ring-oscillator used for the electrical tests [6].

The ring oscillator has been experimentally tested to validate the MESFET modelling and the theoretical design.
The circuit oscillated in a frequency range between 490kHz and 560kHz (figure 13), depending on the drain bias. The drain bias impact on frequency has been extracted from measurements and compared to simulation ($\Delta_{FOSC}/\Delta V_{DS}$=8.75kHz/V). As inferred in figure 13, the slopes of the simulated and measured curves are almost similar. The middle-range oscillating frequency value ($f_{MID}@V_{DS}$=26V) is depending on the MESFET capacitors implemented in the SPICE model.
This shift (from 1MHz down to 500kHz) could be due to either the non-polarization of the buried P-type gate or the error in the estimation of the internal MESFET capacitors.

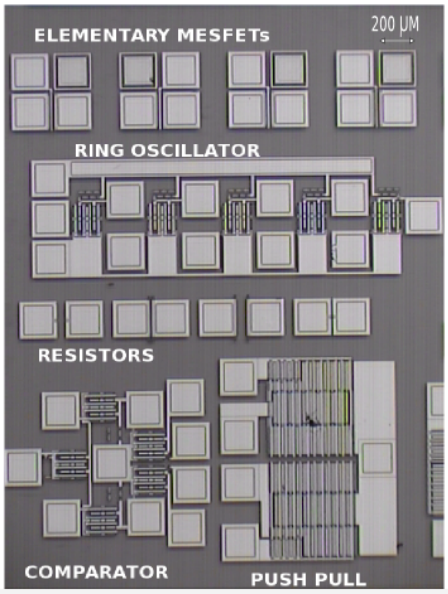

Figure 12 Photography of the fabricated wafer showing various SiC functions

Indeed, the MESFET topology used for the test impeded the polarization buried gate, meaning that the P-buried layer bias is floating and depending on the drain polarization (figure 13 and 14).

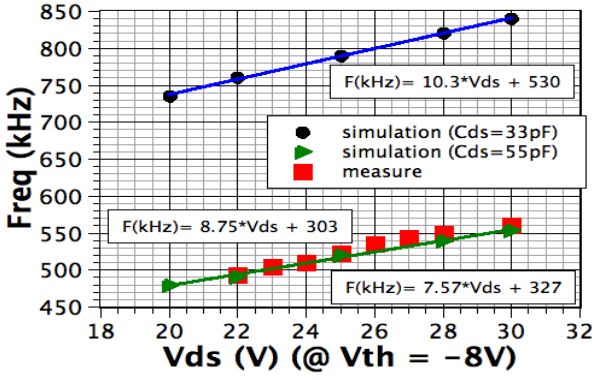

Figure 13 Drain bias influence on the output frequency : simulations and measurement comparison (for V_{TH} = -8V)

A mismatch of 40% in C_{DS} estimation impacts F_{OSC} of 200kHz, while a variation of the buried gate polarisation will impact the channel geometry, reducing the threshold

voltage, i.e. changing both oscillation range and frequency. Both effects, capacitor estimation error and mostly buried layer self polarization, are modifying the MESFET channel dimension i.e. the saturation current, thresholds voltage and consequently the oscillation frequency (figures 13 and 14). The buried layer self polarization implies a threshold voltage V_{TH} reduction. As inferred from figure 14, a 1V variation associated to the low accuracy of the estimation of C_{DS}, will impact dramatically on the oscillation frequency ($\Delta f_{OUT}/\Delta V_{TH}$ = 275kHz/V (black), $\Delta f_{OUT}/\Delta V_{TH}$ = 212kHz/V (red)).

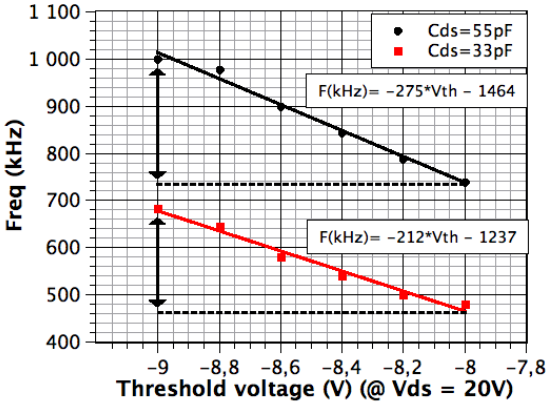

Figure 14 Influence of the voltage threshold on the output frequency

In conclusion, the difference between the simulations and the measurements of the ring oscillator can be explained by the variation of the buried gate bias (V_{TH} reduction) and the approximated values of the capacitors. However, the external capacitors gives flexibility to tune the swing frequency (figure 10, C1, C2, C3).
The simulation results show that the oscillator presents a weak drain bias sensitivity (figure 13). Furthermore, the circuit has a strong V_{TH} sensitivity (figure 14) depending on the buried gate polarisation. This last aspect is an advantage, which makes this devices suitable for VCO function implementation.

5 Design of the integrated power converter

Based on these previous functions, a monolithic power converter and it's driver has been designed (figure 15).
The converter (AC-DC regulated boost converter) is composed of a power part and a logic-control-one. A full bridge rectifier and a regulated boost converter have been implemented. The driver has been partitioned into several functional blocks : signal, buffer and regulation.
The power converter has been designed to supply an output power of 40W for 0.27cm², corresponding to a power density of 150W/cm². The power switch being a dual-gate MESFETs, the gate G_1 is used to apply a fixed frequency signal (1MHz) on the power switch, the G_2 gate enabling to apply in parallel a signal control.

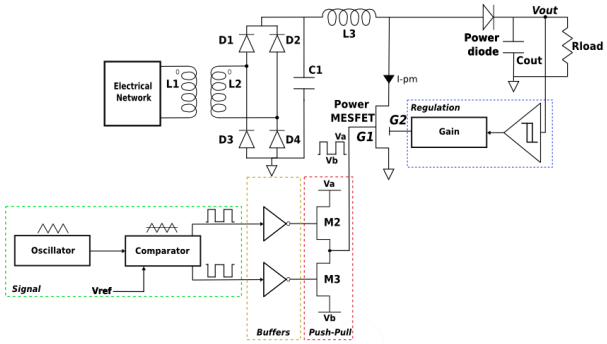

Figure 15 Boost circuit based on lateral DG-MESFETs

The figure 16 shows a SPICE simulation operation of the converter and an its response to an over-load at t=20us. Upper graph presents the output voltage V_{OUT} (red), and output current I_{LOAD} (black) evolution as well as the power MESFET current I_{PM} (blue) . The lower graph show the control gates bias voltage V_{G2} (thick, black). In this simulation, the regulation is made by an hysteresis block, using the Capacitance-Schmitt-trigger circuit described previously.
The 1MHz gate 1 signal is modulated by the dynamic regulation gate 2 voltage V_{G2} while the output voltage increases higher than the define threshold voltage. During the overload phase (20 µs < t < 32 µs) the control gate is inactive, and start acting again while turning back in normal operating mode (t > 32 µs). In both cases the output voltage oscillation is kept lower than 270mV.

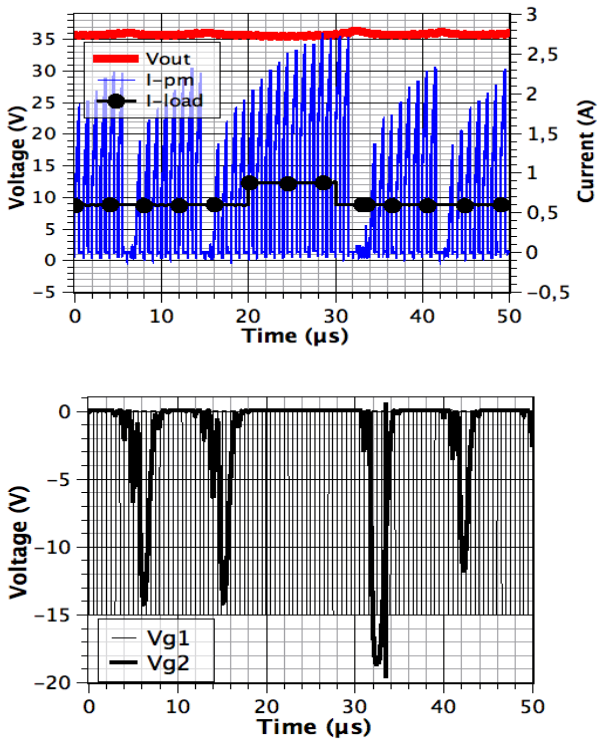

Figure 16 Simulated signals of the boost circuit based on lateral DG-MESFETs

6 Characterization of the elementary components

A picture of the first batch of SiC-MESFET integrated power converter layout is presented in figure 14. The SiC SI-wafer has been fabricated at CNM of Barcelona (Spain). Integration of inductors and capacitors has not been considered as a first step. Only the logic-circuitry, the power switch (Power MESFET), diodes and resistors of the power converter have been integrated using 5 level metallization process.

In addition of integrated circuits, elementary components like Schottky diodes, bipolar diodes, zener diodes and test devices have been implemented.

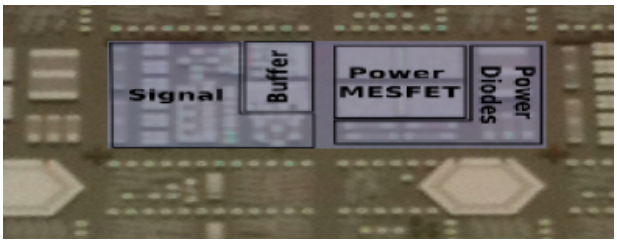

Figure 14 Photography of the elementary field of the SI-SiC integrated power converter (signal-left / control-right)

Preliminary MESFETs characterization results are shown in figure 15. The components are blocking when a negative voltage is applied to the gate of the unipolar components. However, the figure 15 shows that the behaviors of the MESFETs is scattered.

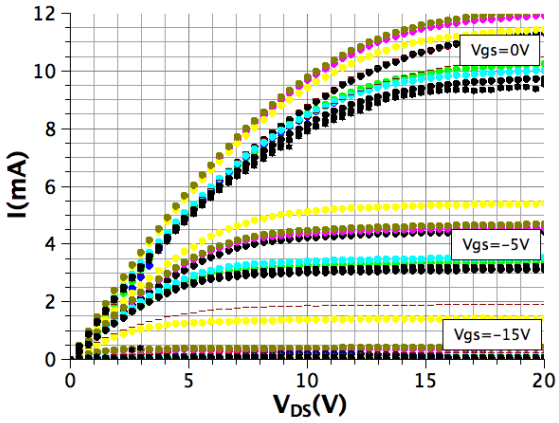

Figure 15 Experimental characteristics $I_{DS}=f(V_{DS})$ of elementary SiC MESFETs

The characteristics dispersion comes from an identified and corrected fabrication process step. Next steps will be the experimental validation of the Integrated Power Converter at high temperature.

7 Conclusion

This paper focuses on the characterization, modeling, and simulation design of a monolithic power converter. It is the first full integrated SiC driver based on double-gate lateral MESFET technology, which might be a technological solution for future High Temperature applications.

The SPICE model established in static and dynamic shows limits, especially in reason of a lack of accuracy. However, this model could be used to design elementary functions and power converters. An improved model based on analytic equations and finite elements simulations is currently developed.

Acknowledgments.

This work has been made in collaboration with the CNM of Barcelona in the framework of the "Advanced Wide Band Gap Semiconductor Devices for Rational Use of Energy" project, Spanish Ministry of Sience and Innovation (MICINN), Project Number CSD2009-00046.

8 References

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