V TH -Hysteresis and Interface States Characterisation in SiC Power MOSFETs with Planar and Trench Gate

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***Abstract*—This paper contributes to investigations on the threshold-voltage (V_{TH}) hysteresis in SiC power MOSFETs. Such effect is of relevance mainly for sub-threshold operation of the devices, but needs to be told apart from stress-related V_{TH}-drift phenomena for technology maturity and reliability validation goals. Important differences exist in commercially available devices, particularly in relation to their gate technology, planar or trench, the latter also showing a marked temperature dependence of the hysteretic range. Based on the experimental characterization of the interface capacitance and charge, this paper puts forward a methodology for determining the types of traps affecting the various devices, with the aim of contributing a tool to assist driving of technological maturity in future generation devices. This paper also shows the potential of capacitance hysteresis measurement to the estimation of the distribution of interface.**

Keywords- SiC MOSFETs, Trench gate, Planar gate, Threshold voltage hysteresis, interface traps.

NOMENCLATURE

V_{TH}	MOSFET's threshold voltage
ΔV_{TH}^{HYST}	Subthreshold domain V_{TH} hysteresis
ψ	Surface potential
ε_S	Dielectric constant of SiC
t_{OX}	Oxide thickness
D_{IT}	Density of interface states
ΔE_{VTH}	Energy span of the D_{IT}
Q_S	Total space charge of the channel
Q_{IT}	Interface trapped charge
Q	Net charge of the channel: $Q = Q_S + Q_{IT}$
τ_{ep}	Hole emission time constant
τ_{en}	Electron emission time constant
C_{OX}	Oxide capacitance
C_{iss}	Input capacitance
ΔC_{iss}	Downward C_{iss} sweep – Upwards C_{iss} sweep

I. INTRODUCTION

SiC MOSFETs are desired for power applications as they show outstanding properties compared to same rating IGBTs. Two main structures are used to manufacture vertical power MOSFET, planar and trench [1]. The planar structure is easier to fabricate, but has the disadvantage of having a higher on-state resistance compared to the same rating trench one. This is due to the channel current flowing perpendicularly to the vertical direction and the existence of the inner JFET region. In the trench structure, there is no JFET region and the channel current flows in the vertical direction, taking a shorter path. Both structures are compared in Fig. 1, where the typical current path is shown and the net resistance is modeled as a series of several components related to the structure parts.

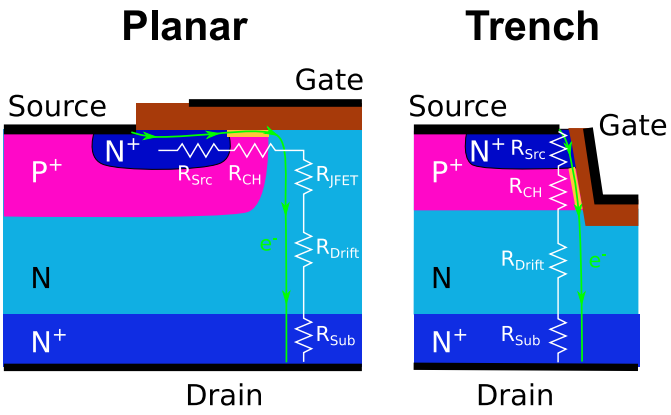

Figure 1. *Basic structures of vertical planar and trench N-MOSFETs. Channel region has been emphasized and typical current path is shown by the green lines. The net resistance is modeled as a series association of the constituting part's resistances. Notice the absence of JFET region resistance for the trench MOSFET. Same rating trench devices should have a lower on-state resistance.*

The contributions of each part have been compared for different rating on planar devices, showing that for voltage rating above 600 V the JFET region resistance constitutes a significant amount of the total resistance of the MOSFET [2]. For all these reasons, the trench type MOSFET is the most desired ones. Technology maturity is going forward, and some manufacturers are achieving to produce SiC trench MOSFETs. Nevertheless, the progress in terms of reliability needs to be put forward before attempting to replace Si-IGBTs in the 1-10 kV rating. Some of the issues plaguing SiC MOSFET's market expansion are related to threshold voltage instabilities [3]–[6]. Sub-threshold V_{TH}-hysteresis is a reversible instability that will be addressed throughout this paper.

The effect of V_{TH}-hysteresis in modern SiC power MOSFETs has been highlighted and interpreted in [7]. The effect mainly interests sub-threshold bias operational conditions, although some investigations have shown that even above threshold operation can show *memory* of the preceding bias condition, exactly as a result of the hysteresis of V_{TH} [8], [9]. However, in the context of reliability investigations, the main interest for further investigating such phenomenon is

primarily related to the development of SiC-bespoke technology validation tests, able to distinguish between the *drift* phenomena caused by the electro-thermal stress and the seemingly fully reversible hysteretic behavior [10].

Recent investigations have targeted a benchmark of commercially available devices, based in particular on differences in their gate terminal technology [11]. For illustration, Fig. 2 shows a summary of results for the measured drain current as a function of applied gate-source bias voltage, during upwards and downwards sweep of the bias parameter.

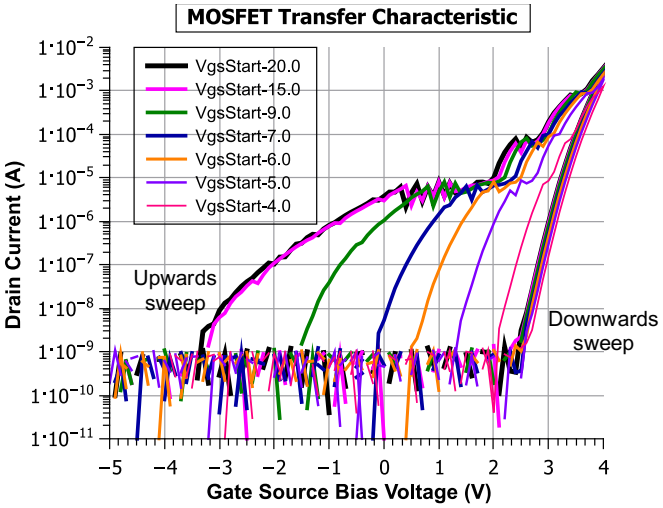

Figure 2. *Measure of V_{TH}-hysteresis in a commercial trench SiC MOSFET: wide oval contains the upward sweep and the small circle the downward sweep of V_{GS}; for increasing values of the starting gate-source voltage, the up and down curves drift apart significantly.*

As can be seen, a difference exists in the curves (here, V_{TH} refers to a drain current value of 100 nA while the drain terminal is constantly biased at 1 V), which becomes more pronounced as the value of negative bias is increased. Fig. 3 reports the measured V_{TH} as a function of starting V_{GS} value for four commercial transistors, 2 of planar gate and 2 of trench gate type, all in the nominal voltage class of 1.2 kV.

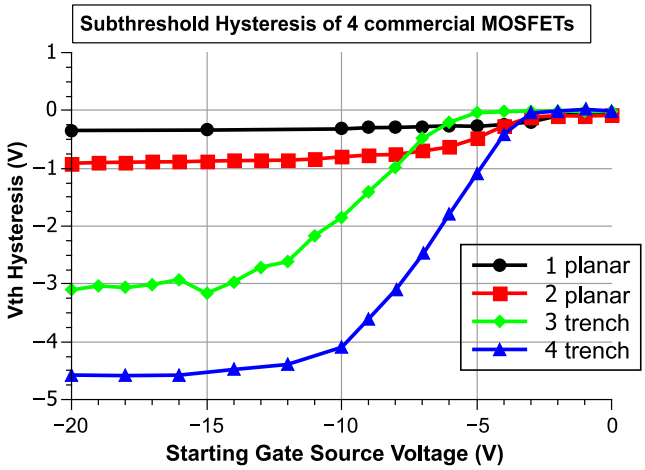

Figure 3. *V_{TH}-hysteresis measured on a number of commercial transistors, including 2 planar and 2 trench gate technology MOSFETs, all from different manufacturers. Trench devices suffer in a much more pronounced way from the hysteretic effect.*

Quantitatively, this issue is more significant for trench devices, which, as shown in Fig. 4, also exhibit non-negligible dependence on temperature.

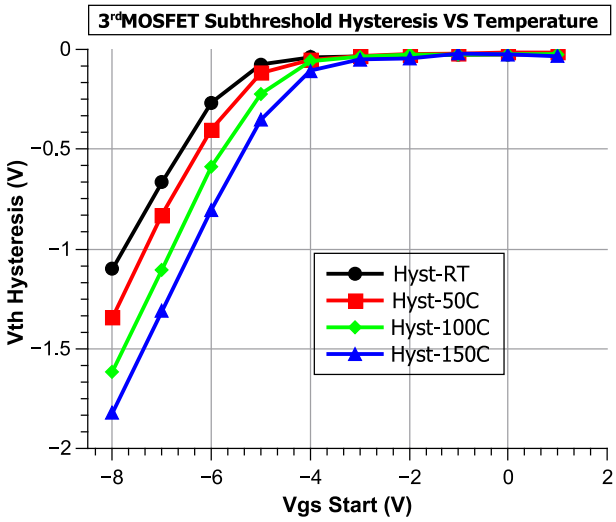

Figure 4. *Experimental data for the temperature dependence of the hysteresis effect, mostly significant for one particular trench device type (3 trench).*

It is important to ascertain specificities of the technology or manufacturing process that can yield such different results in the interface states of the two technologies. In a first approximation, the amplitude of hysteresis (ΔV_{TH}^{HYST}) can be described as follows [6]:

$$\Delta V_{TH}^{HYST} = \frac{Q_{IT}}{C_{OX}} = \frac{qD_{IT}\Delta E_{VTH}t_{OX}}{\varepsilon_r\varepsilon_0} \qquad (1)$$

where *Dit*, the density of interface defects, ΔE_{VTH}, the width of energy over which the V_{GS} is swept, and t_{OX}, the gate-oxide thickness, are all engineering dependent parameters concurring to determine the fraction of energy bandgap over which the traps are charged positively. So, a measure of the charge as a function of surface potential is considered a potentially powerful method for determining both the density and the type of trap affecting the interface.

This paper offers a benchmark of the hysteresis of the static input capacitance (C_{iss}) of 4 commercial 1200 V SiC MOSFETs denominated 1, 2, 3 and 4 throughout the document, where 1 and 2 are planar whereas 3 and 4 are trench. An empirical analysis of the interface states density is proposed and the basis of a new characterization technique of the MOS interface are shown.

II. Methodology and Results

In the bias conditions transition from accumulation to inversion, assuming presence of both donor and acceptor traps, the transistor band-diagram can be summarily schematized as in Fig. 5.

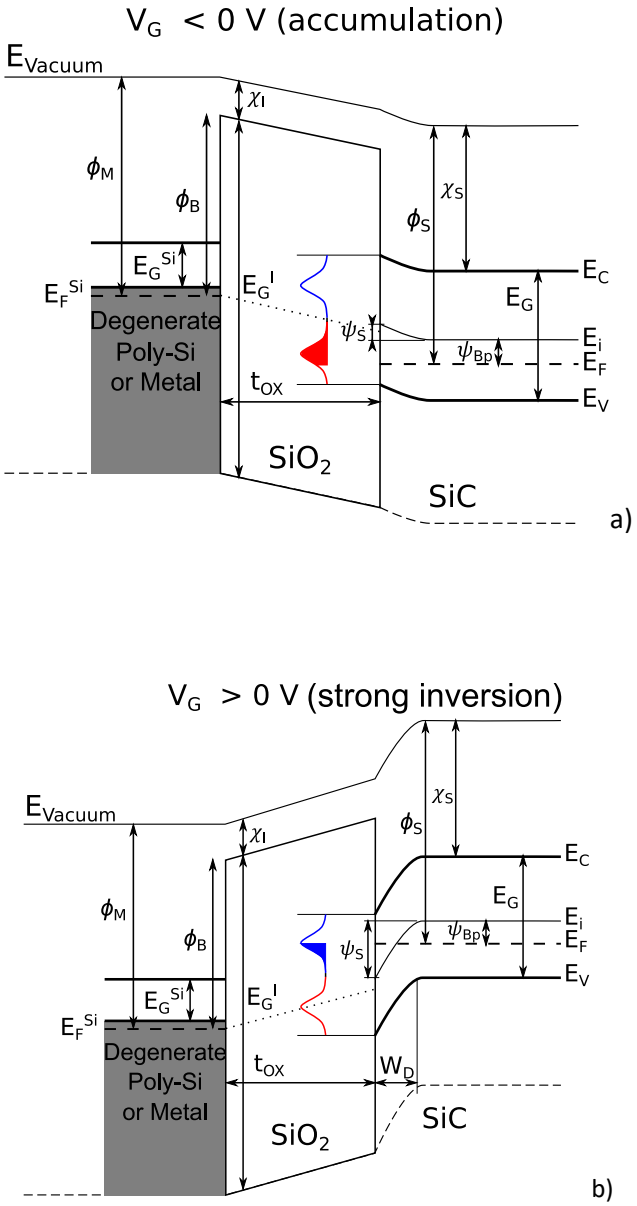

Figure 5. *Representation of the band diagram of a power N-MOSFET in accumulation a) and strong inversion b), taking into account the work-function difference between degenerate poly-Si gate or metal and SiC and containing Gaussian distributions of both donor (red, lower part of the gap) and acceptor (blue, upper part of the gap) traps in the oxide near the interface. Mobile ions and fixed charge are not taken into account.*

In this case, holes are released from the interface and electrons are captured. This results in a measurable current since the surface potential is affected. Macroscopically, this is related to an easily detectable difference of the measured input capacitance C_{iss} vs. V_{GS} bias (C_{iss}=C_{gs}+C_{gd}; source and drain are shorted), with the depletion region corresponding to a deviation from a constant capacitance value (first decrease and then increase). The hysteresis has the effect of also introducing differences in the measured capacitance values during the up and down-sweeps: representative results for planar SiC MOSFETs are reported in Fig. 6.

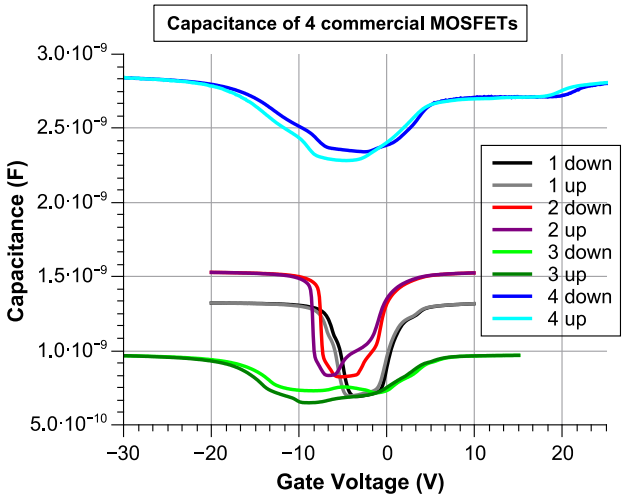

Figure 6. *Measured input capacitance Ciss of 4 commercial SiC N-MOSFET as a function of bias conditions. Notice that there is a wide discrepancy between the capacitance characteristic and that the sweep direction has a strong effect.*

This means that the captured charge at the interface and at the edge of the oxide is actually modifying the net charge of the MOS system, because the voltage sweep is too fast for the interface to reach the thermodynamic equilibrium. As a result, a measurable hysteresis of the input capacitance appears. In order to define the traps responsible for the capacitance shift, it is important to notice that in accumulation and inversion the MOS system is in equilibrium and that the applied voltage is expressed as:

$$V = \psi + \frac{Q}{C_{OX}} \tag{2}$$

where ψ is the surface potential, Q is the net charge of the channel and C_{OX} is the maximum capacitance. In case of a fast sweep from accumulation to inversion or vice versa, the voltage in the nonequilibrium part is affected by the interface states and can be accounted as follows:

$$V = \psi + \frac{Q_S}{C_{OX}} + \frac{Q_{IT}}{C_{OX}} \tag{3}$$

where Q_{IT} is the charge trapped at the interface. Depending on the sweep step amplitude and direction, dV/dt is expressed as:

$$\frac{dV}{dt} = \frac{d\psi}{dt} + \frac{{}^{dQ_S}/_{dt}}{C_{OX}} + \frac{{}^{dQ_{IT}}/_{dt}}{C_{OX}} \tag{4}$$

Which means that if dV/dt does not allow to reach the equilibrium. Equation (4) will have two different forms depending on its sign. Both the semiconductor charge and the surface potential do not depend on the time as dV/dt is very small in normal characterization conditions to yield transient behavior of these quantities, whereas dynamics of the charge trapped at the interface is related to the emission and capture time constants. The difference between the sweep rates from accumulation to inversion and from inversion to accumulation can be expressed as:

$$\left(\frac{dV}{dt}\right)_{Accu\to Inv} - \left(\frac{dV}{dt}\right)_{Inv\to Accu} = \left(\frac{{}^{dQ_{IT}}/_{dt}}{C_{OX}}\right)_{Accu\to Inv} - \left(\frac{{}^{dQ_{IT}}/_{dt}}{C_{OX}}\right)_{Inv\to Acc} \tag{5}$$

Eq. (5) is very interesting, because it can be written as (6) if the sweep is done at constant and equal step from for both directions:

$$\Delta C_{iss}\frac{dV}{dt} = \left(\frac{dQ_{IT}}{dt}\right)_{Accu\rightarrow Inv} - \left(\frac{dQ_{IT}}{dt}\right)_{Inv\rightarrow Accu} \quad (6)$$

This means that the difference among the capacitance curves is provoked by currents resulting from emissions of holes when sweeping from accumulation to inversion, $i_{e,p}$ and from emission of electrons when sweeping from inversion to accumulation, $i_{e,n}$.

$$\Delta C_{iss}\frac{dV}{dt} = i_{e,p} + i_{e,n} \quad (7)$$

The emission time constants for a discrete trap at energy level E_T is expressed as $\tau_{e,p}$ for holes and $\tau_{e,n}$ for electrons. υ and σ are the thermal drift velocity and capture cross section respectively.

$$\tau_{ep} = \frac{1}{\upsilon\sigma N_V}e^{\frac{E_T-E_V}{kT}} \text{ and } \tau_{en} = \frac{1}{\upsilon\sigma N_C}e^{\frac{E_C-E_T}{kT}} \quad (8)$$

These time constants depend on several parameters :

- the position of the trap energy levels with respect to valence/conduction band energy for hole/electron traps
- the effective density of states in the valence band,
- the effective density of states in the conduction band
- the capture section
- and the operating temperature

From literature [12]–[14], it is known that "deep" level traps can be expressed as a transient of capacitance. In the special case of MOS structures, the relation between the capacitance transient and a trap energy level is given as follows:

$$\frac{\Delta C_{iss}}{C_{iss}} = \frac{C_{iss}}{\varepsilon_S C_{OX}}\cdot\frac{N_T}{N_D}\left(e^{-\tau_{e,p}\cdot t} + e^{-\tau_{e,n}\cdot t}\right) \quad (9)$$

For a MOSFET containing a continuum of interface traps equation (9) becomes:

$$\frac{\Delta C_{iss}(E)}{C_{iss}(E)} = \frac{C_{iss}(E)}{\varepsilon_S C_{OX} N_D}\cdot\int_{E_V}^{E_C}\left(D_{IT,p}\cdot e^{-\tau_{e,p}\cdot t} + D_{IT,n}\cdot e^{-\tau_{e,n}\cdot t}\right)dE \quad (10)$$

Being able to measure the capacitance hysteresis for different voltage steps and timing can lead to the extraction of the interface density of states and their emission time constants.

$$\lim_{t\to\infty}\frac{\Delta C_{iss}(E)}{C_{iss}(E)} = \frac{C(E)}{\varepsilon_S C_{OX} N_D}\cdot\int_{E_V}^{E_C} D_{IT}(E)\,dE \quad (11)$$

This means that $D_{IT}(E)$ can be found from the derivation of equation (11)

$$D_{IT}(E) = \frac{d\left(\frac{\Delta C_{iss}(E)\varepsilon_S C_{OX} N_D}{{C_{iss}}^2(E)}\right)}{dE} \quad (12)$$

The derivative of Eq. (12) can be numerically obtained. The computation of trap levels distribution, which are responsible of the subthreshold hysteresis in SiC MOSFETs, relies only on the knowledge of the device's manufacturing parameters, such as :

- Oxide thickness
- Channel doping
- Active area

These results are encouraging since measuring ΔC_{iss} is done by means of an impedance analyzer which is a relatively low cost tool. For instance, Fig. 7 shows the ΔC_{iss} obtained from the results of Fig. 6. The measurements have been performed with a 100 mV step, without any measurement delay. The measurement timing does not satisfy Eq. (11), as timing parameters are shorter than the emissions times. For that reason, along with missing information about device parameters the D_{IT} calculation has not been performed.

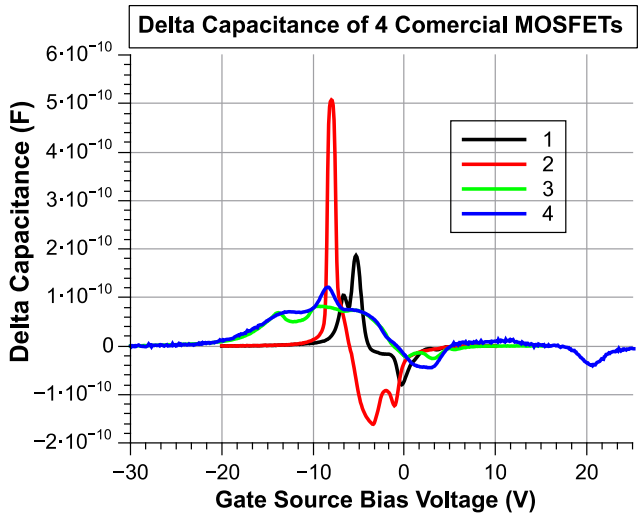

Figure 7. *Measured input Capacitance Hysteresis expressed as the difference between downward sweep and upward sweep. The sign is related to the type of traped charge, positive for holes and negative for electrons. All MOSFETs have very different densities of interface states, which are related to the semiconductor surface preparation and the quality of the oxide.*

III. Discussion And Conclusions

The interface states responsible for the *Ciss* hysteresis are relatively slow states. This means that the emission time constants are long. This claim is supported by the influence of the hysteresis on the short circuit behavior of SiC MOSFETs. As a matter of fact, even for large swings of the surface potential from accumulation to strong inversion the V_{TH} hysteresis is not completely erased and slightly enhances the drain current at room temperature [9]. For this reason, the conditions necessary for Eq. (12) are not met and the computation of the D_{IT} is not trivial. The measurement timing parameters have to be chosen carefully in order to decorrelate the influence of long emission time constants. One way to proceed is to measure the *Ciss* with different delays between

each acquisition point in order discriminate fast states from slow states. Fig. 8 shows the effect of the measurement delay on the input capacitance hysteresis of device 1 (planar). As the delay increases, the hysteresis value decreases and from one peak several peaks emerge. This means that long delays are necessary to discriminate traps of energy levels nearby. Another interesting fact is that all peaks do not follow the same progression as they do not necessarily have the same emission time constants. This is especially visible for peaks of opposite value since positive values correspond to hole traps and negative peaks correspond to electron traps.

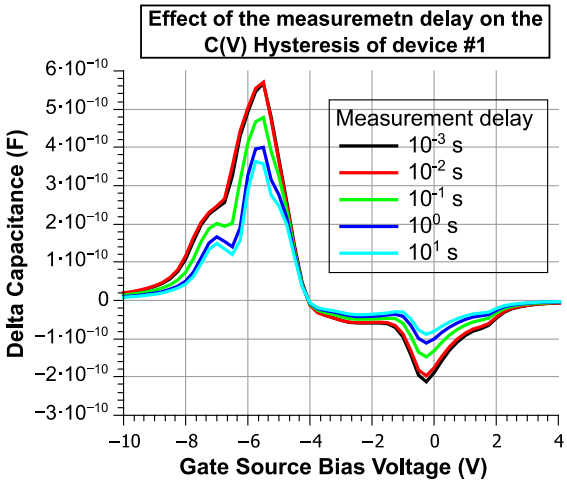

Figure 8. *The effect of the measurement delay on the capacitance hysteresis shows that the responsible traps have relatively high emission time constants. As the measurement delay is increased the different trap energy levels are better discriminated. Hole traps are responsible for positive peaks and electron traps for the negative ones.*

Important information can also be retrieved from measurements carried out at different temperatures. Since increasing the temperature will decrease the emission time constants, the input capacitance peaks decrease. This is the case in Fig. 9, where the effect of temperature on the C(V) hysteresis is explored.

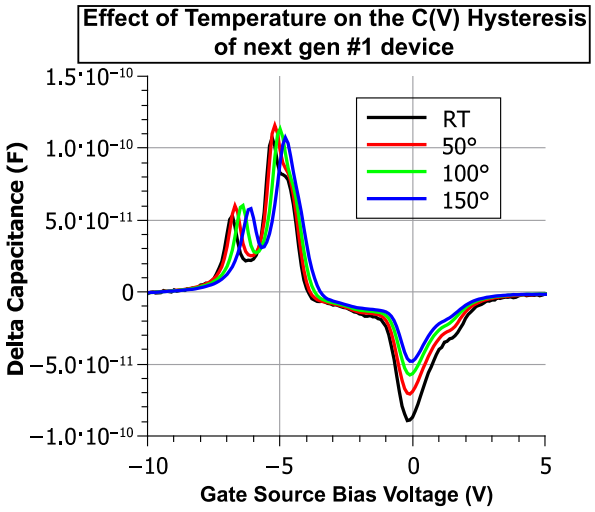

Figure 9. *The effect of temperature on the capacitance hysteresis shows that hole traps (positive peaks) have relatively higher emission time constants than electron traps (negative peaks). As the temperature is increased the different peaks start to merge.*

As it can be seen, hole traps (positive peaks) have relatively higher emission time constants than electron traps (negative peaks). This result is in accordance with previous studies of the V_{TH} hysteresis where hole traps are held responsible. As the temperature is increased the different peaks start to merge.

This results show that the input capacitance C_{iss} hysteresis measurements can constitute a powerfull tool for the analysis of the interface states of 4H-SiC MOSFETs. They show that measurement delay coupled with temperature variation can be enough to determine the interface states and the emission time constants for the traps responsible of the V_{TH} Hysteresis.

Further studies, on devices whith known parameters are necessary to validate this methodology and put forward a new characterisation technique for the inerface of 4H-SiC MOSFETs.

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