

Hierarchical Approach in RNS Base Extension for Asymmetric Cryptography

Libey Djath¹, Karim Bigou¹, Arnaud Tisserand²

¹ Université de Bretagne Occidentale / Lab-STICC, UMR CNRS 6285
² CNRS / Lab-STICC, UMR 6285

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Asymmetric cryptography serves in:

- digital signature
- authentication
- secret key exchange

An example of asymmetric cryptosystem:

- Elliptic Curve Cryptography (ECC) [Mil85, Kob87]

For ECC, computations are performed in $GF(P)$ with P a 200 – 500 bits prime

1 ECC primitive requires a thousand of additions, subtractions and multiplications modulo P

Residue Number System (RNS)

RNS

- non-positional representation system
- Chinese Remainder Theorem (CRT)
- X is represented by its residues over a base
- representation with internal parallelism

RNS base

An RNS base \mathcal{A} is a tuple (a_1, a_2, \dots, a_n) of coprime integers named moduli

Representing the number X

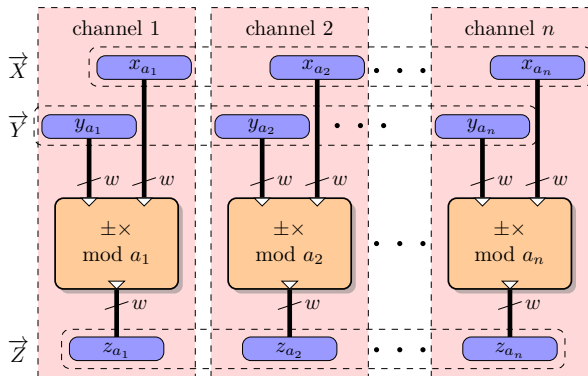
$$\vec{X} = (X \bmod a_1, X \bmod a_2, \dots, X \bmod a_n)$$
$$\vec{X} = (x_{a_1}, x_{a_2}, \dots, x_{a_n})$$

Converting back to positional representation

Compute the CRT over all the x_{a_i} s in base \mathcal{A}

In hardware implementations of asymmetric cryptosystems:

- **large integers** are splitted in **small residues** (typically 16-64 bits integers)
- computations on **large integers** are replaced by parallel computations on **small residues**



a_i are pseudo
Mersenne for
efficiency
purpose

Main advantages of RNS architectures:

- carry free operations among the channels
- fast parallel $+$, $-$, \times
- random order internal computations

Drawback:

- Comparison, division and $\text{mod } P$ reduction are difficult

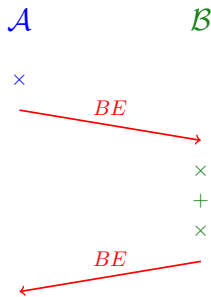
RNS Montgomery mod P Reduction [PP95]

Input: X_A, X_B

Precomp.: $P_A, P_B, (-P^{-1})_A, (A^{-1})_B$

Output: S_A and S_B with $S = (XA^{-1}) \bmod P + \delta P$
and $\delta \in \{0, 1, 2\}$

- 1 $Q_A \leftarrow X_A \times (-P^{-1})_A$
- 2 $Q_B \leftarrow BE(Q_A, \mathcal{A}, \mathcal{B})$
- 3 $R_B \leftarrow X_B + Q_B \times P_B$
- 4 $S_B \leftarrow R_B \times (A^{-1})_B$
- 5 $S_A \leftarrow BE(S_B, \mathcal{B}, \mathcal{A})$
- 6 **return** (S_A, S_B)



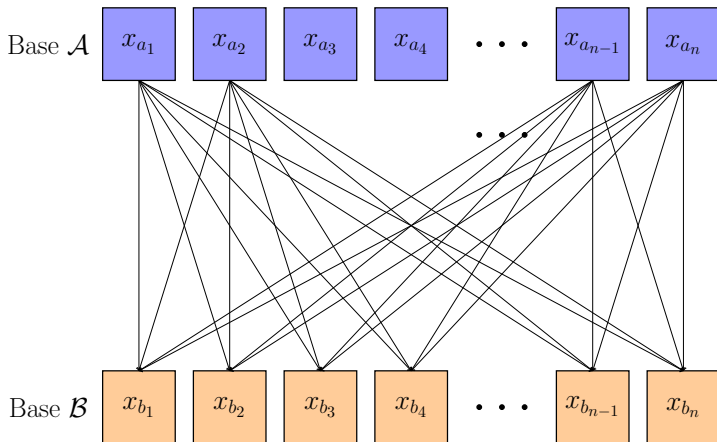
BE: base extension

Chinese Remainder Theorem (CRT) formula

$$X = \left| \sum_{i=1}^n |x_{a_i} \times \left(\frac{A}{a_i}\right)^{-1} |_{a_i} \times \frac{A}{a_i} \right|_A = \left(\sum_{i=1}^n |x_{a_i} \times \left(\frac{A}{a_i}\right)^{-1} |_{a_i} \times \frac{A}{a_i} \right) - hA$$

with $A = a_1 \times \dots \times a_n$

Base Extension (BE) [KKSS00]



BE converts X in base \mathcal{A} into X in base \mathcal{B}

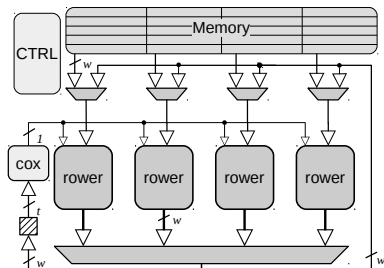
Base Extension [KKSS00]

BE algorithm from [KKSS00]

Input: X_A , $\sigma = 0$ or 0.5
Precomp.: $T_{a_i} \forall i \in [1, n]$
Output: X_B

- 1 for i from 1 to n parallel do
- 2 | $\hat{x}_{a_i} \leftarrow |x_{a_i} \times T_{a_i}|_{a_i}$
- 3 for i from 1 to n do
- 4 | $\sigma \leftarrow \sigma + \frac{\text{trunc}(\hat{x}_{a_i})}{2^w}$
- 5 | $h_i \leftarrow \lfloor \sigma \rfloor$
- 6 | $\sigma \leftarrow \sigma - h_i$
- 7 | for k from 1 to n parallel do
- 8 | | $x_{b_k} \leftarrow |x_{b_k} + \hat{x}_{a_i} \times \left| \frac{A}{a_i} \right|_{b_k} + | -h_i A |_{b_k} |_{b_k}$

Cox-rower architecture from [Gui10]



State of the art solution is usually called KBE

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Idea of Hierarchical Base Extension (HBE)

Changing the notation

$$\mathcal{A} = (a_1 \quad \cdots \quad a_n) \quad \mathcal{A} = \begin{pmatrix} a_{1,1} & \cdots & a_{1,c} \\ \vdots & \cdots & \vdots \\ a_{r,1} & \cdots & a_{r,c} \end{pmatrix}$$

with $n = r \times c$

Main Idea

- gather residues by row (c residues per row) into super-residues in base \mathcal{A} by computing their partial CRTs
- compute the CRT of the super-residues of base \mathcal{A} in base \mathcal{B}

Rewriting the KBE Algorithm

1D KBE

Input: X_A , $\sigma = 0$ or 0.5
Precomp.: $T_{a_i} \forall i \in [1, n]$
Output: X_B

```
1 for  $i$  from 1 to  $n$  parallel do
2    $\hat{x}_{a_i} \leftarrow |x_{a_i} \times T_{a_i}|_{a_i}$ 
3 for  $i$  from 1 to  $n$  do
4    $\sigma \leftarrow \sigma + \frac{\text{trunc}(\hat{x}_{a_i})}{2^w}$ 
5    $h_i \leftarrow \lfloor \sigma \rfloor$ 
6    $\sigma \leftarrow \sigma - h_i$ 
7   for  $k$  from 1 to  $n$  parallel do
8      $x_{b_k} \leftarrow |x_{b_k} + \hat{x}_{a_i} \times \frac{A}{a_i}|_{b_k} + | - h_i A |_{b_k}|_{b_k}$ 
```

Main cost: n^2 executions of line 8

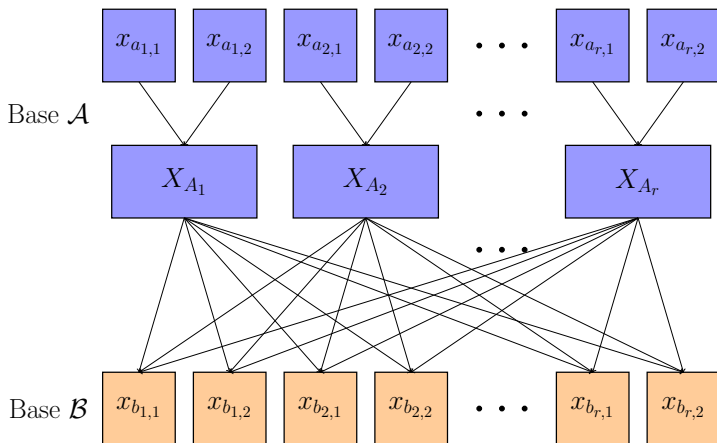
2D KBE

Input: X_A , $\sigma = 0$ or 0.5
Precomp.: $T_{a_{i,j}} \forall i \in [1, r]$ and $\forall j \in [1, c]$
Output: X_B

```
1 for  $i$  from 1 to  $r$  parallel do
2   for  $j$  from 1 to  $c$  parallel do
3      $\hat{x}_{a_{i,j}} \leftarrow |x_{a_{i,j}} \times T_{a_{i,j}}|_{a_{i,j}}$ 
4 for  $i$  from 1 to  $r$  do
5   for  $j$  from 1 to  $c$  do
6      $\sigma \leftarrow \sigma + \frac{\text{trunc}(\hat{x}_{a_{i,j}})}{2^w}$ 
7      $h_{i,j} \leftarrow \lfloor \sigma \rfloor$ 
8      $\sigma \leftarrow \sigma - h_{i,j}$ 
9     for  $k$  from 1 to  $r$  parallel do
10      for  $l$  from 1 to  $c$  parallel do
11         $x_{b_{k,l}} \leftarrow |x_{b_{k,l}} + \hat{x}_{a_{i,j}} \times \frac{A}{a_{i,j}}|_{b_{k,l}} + | - h_{i,j} A |_{b_{k,l}}|_{b_{k,l}}$ 
```

With $n = r \times c$, main cost:
 $r^2 c^2$ executions of line 11

HBE ($c = 2$)



Comparison between KBE and HBE

KBE

Input: X_A , $\sigma = 0$ or 0.5
Precomp.: $T_{a_i,j} \forall i \in [1, r]$ and $\forall j \in [1, c]$
Output: X_B

```
1 for i from 1 to r parallel do
2   for j from 1 to c parallel do
3      $\hat{x}_{a_i,j} \leftarrow |x_{a_i,j} \times T_{a_i,j}|_{a_i,j}$ 
4   for i from 1 to r do
5     for j from 1 to c do
6        $\sigma \leftarrow \sigma + \frac{\text{trunc}(\hat{x}_{a_i,j})}{2^w}$ 
7        $h_{i,j} \leftarrow \lfloor \sigma \rfloor$ 
8        $\sigma \leftarrow \sigma - h_{i,j}$ 
9       for k from 1 to r parallel do
10        for l from 1 to c parallel do
11           $x_{b_{k,l}} \leftarrow |x_{b_{k,l}} + \hat{x}_{a_i,j} \times \left| \frac{A}{a_{i,j}} \right|_{b_{k,l}} + | -h_{i,j} A |_{b_{k,l}}|_{b_{k,l}}$ 
```

Main cost: $r^2 c^2$ executions
of line 11

HBE

Input: X_A , $\sigma = 0$ or 0.5
Precomp.: $T_{a_i,j} \forall i \in [1, r]$ and $\forall j \in [1, c]$
Output: X_B

```
1 for i from 1 to r parallel do
2   for j from 1 to c parallel do
3      $\hat{x}_{a_i,j} \leftarrow |x_{a_i,j} \times T_{a_i,j}|_{a_i,j}$ 
4   for i from 1 to r parallel do
5      $\hat{X}_{A_i} \leftarrow 0$ 
6     for j from 1 to c do
7        $\hat{X}_{A_i} \leftarrow \hat{X}_{A_i} + \hat{x}_{a_i,j} \times \overline{a_{i,j}}$  (no reduction)
8   for i from 1 to r do
9      $\sigma \leftarrow \sigma + \frac{\text{trunc}(\hat{X}_{A_i})}{2^w \times c}$ 
10     $h_i \leftarrow \lfloor \sigma \rfloor$ 
11     $\sigma \leftarrow \sigma - h_i$ 
12    for k from 1 to r parallel do
13      for l from 1 to c parallel do
14         $\hat{x}_{b_{k,l},i} \leftarrow |\hat{X}_{A_i}|_{b_{k,l}}$ 
15         $x_{b_{k,l}} \leftarrow |x_{b_{k,l}} + \hat{x}_{b_{k,l},i} \times \overline{A_i} + | -h_i A |_{b_{k,l}}|_{b_{k,l}}$ 
```

Main cost: $r^2 c$ executions
of line 15

Theoretical Cost Comparison for $c = 2$

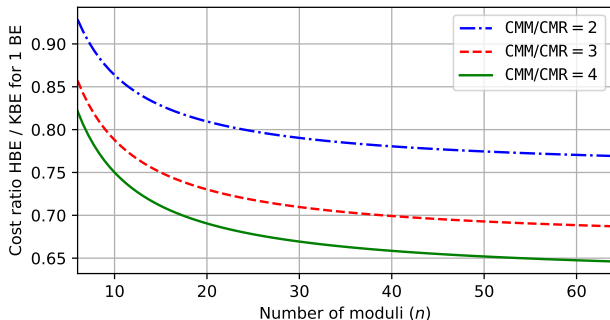
Notation:

- $CMM(w, w)$ for a $(w \times w \bmod w)$ -bit modular multiplication
- $CMR(w', w)$ for a $(w' \bmod w)$ -bit modular reduction

KBE cost: $n^2 CMM(w, w) + n CMM(w, w)$

HBE cost: $\frac{n^2}{2} CMM(w, w) + \frac{n^2}{2} CMR(2w + 1, w) + 2n CMM(w, w)$

Theoretical cost ratio for one BE for various base sizes (n)

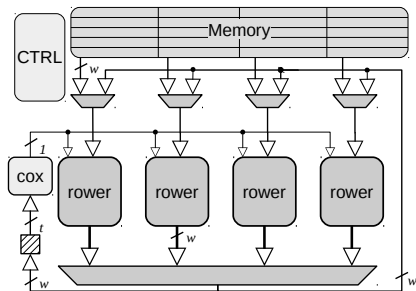


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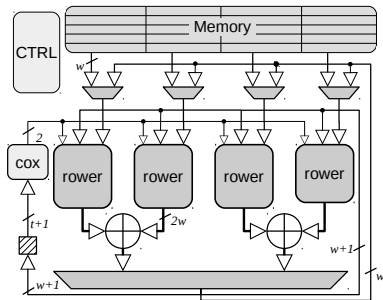
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Architecture Descriptions

Cox-rower architecture for KBE
[Gui10]



Proposed architecture for HBE
($c = 2$)



Hardware Implementation

Target FPGA

ZYNQ-7 ZC702 from Xilinx (ZedBoard xc7z020clg484-1)

Tool

Vivado HLS (version 2017.4) from Xilinx

Implementation

- P size = 256,384 bits
- $w = 17, 20, 24, 28$ bits

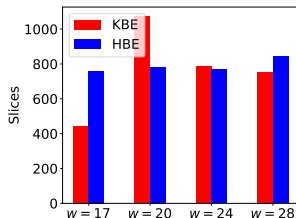
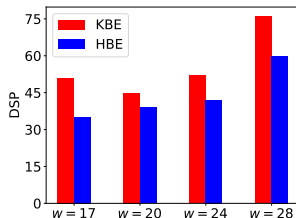
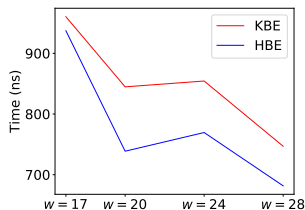
Optimization

Both algorithms, KBE and HBE ($\underline{c = 2}$) are implemented:

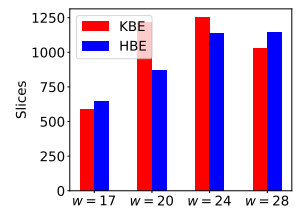
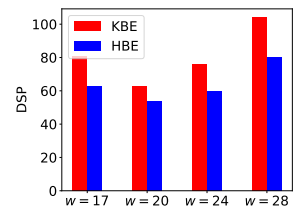
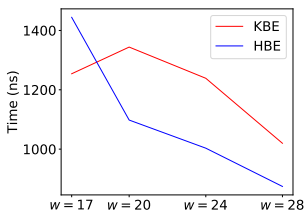
- same manner
- same optimization effort

Hardware Implementation Results

256-bit P :



384-bit P :



- most of the time, we have a faster AND smaller solution
- no impact on BRAMs and periods

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Conclusion

The proposed hierarchical approach BE:

- **improves** the main **cost** of the BE algorithm from $r^2 c^2$ to $r^2 c$
- preserves quite well the internal **parallelism** (for $c = 2$)
- on a XC7Z020 FPGA, it shows an improvement up to **18%** in total time and up to **31%** in DSPs

Future Work

- study the architecture for the cases $c = 3, 4$
- implement a full ECC crypto-processor

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Hardware Implementation Results

\mathbb{F}_p width (bits)	BE algo.	KBE	HBE	KBE	HBE	KBE	HBE	KBE	HBE
	w (bits)	17		20		24		28	
256	nb. slices	445	758	1073	784	785	769	753	843
	nb. DSP	51	35	45	39	52	42	76	60
	nb. BRAM	1	1	1	1	1	1	1	1
	period (ns)	9.8	10.3	9.6	8.9	9.6	9.5	9.7	9.6
	nb. cycles	98	91	88	83	89	81	77	71
	time (ns)	960.4	937.3	844.8	738.7	854.4	769.5	746.9	681.6
384	nb. slices	587	644	1215	869	1251	1134	1031	1145
	nb. DSP	81	63	63	54	76	60	104	80
	nb. BRAM	1	1	1	1	1	1	1	1
	period (ns)	7.6	10.1	9.6	9.0	7.6	7.6	9.9	9.4
	nb. cycles	165	143	140	122	163	132	103	93
	time (ns)	1254.0	1444.3	1344.0	1098.0	1238.8	1003.2	1019.7	874.2

HLS implementation results on a XC7Z020 FPGA for our HBE and the KBE (from [KKSS00]) algorithms for two widths of prime field elements and four RNS channel widths w .