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► **To cite this version:**

J. El Hussein, J. Gyani, Frédéric Martinez, M. Valenza, B Ramadout, et al.. DC and low frequency noise characterization of Multi gate N-MOSFET in a bulk technology by integrating polysilicon filled trenches. ULtimate Integration on Silicon 2010, 2010, Glasgow, United Kingdom. hal-02092983

**HAL Id: hal-02092983**

**<https://hal.science/hal-02092983>**

Submitted on 23 Jun 2020

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# DC and low frequency noise characterisation of Multi gate N-MOSFET in a bulk technology by integrating polysilicon-filled trenches

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**Abstract** — This paper presents a dc and low frequency noise characterization performed on multi gate N-MOSFET in a bulk technology by integrating polysilicon-filled trenches. This architecture provides a standard MOSFET controlled by the surface gate and multiple lateral sub-channels controlled by the lateral gate. A simple compact model predicting the current-voltage lateral transistor characteristics is proposed. Surface and lateral gate oxide interfaces are characterized. The slow oxide trap densities of the two interfaces have been extracted. The values obtained for the surface gate oxide are between  $N_t(E_{Fn}) = 1 \cdot 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$  and  $N_t(E_{Fn}) = 1 \cdot 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ . They are comparable to values for nitrated oxides on Si bulk. For the lateral oxide, we obtain trap densities between  $1 \cdot 10^{15}$  and  $1 \cdot 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ . According to these low values, these devices can be considered as a good candidate for analog applications.

## I. INTRODUCTION

Integrating trenches filled with doped polysilicon provides an alternative solution for electrical isolation of on-chip devices [1]. This contribution presents the study of a multi-gate N-MOSFET in a bulk CMOS technology by integrating lateral trench gate. Fabrication of this device is simple and needs just few extra steps for polysilicon-filled trenches [2]. Featured applications for these multi-gate MOSFET devices are mainly CMOS image sensors (CIS). In this paper we present DC and low frequency noise characterisation of the bulk and lateral transistors with special emphasis given to the lateral gate device. Low-frequency noise is well-known as being a very sensitive characterization tool for probing slow oxide traps. [3]. Noise is also a major concern in analog applications. Therefore, noise measurements have been carried out on the surface and lateral gate transistors in order to evaluate the oxide interfaces and so the potentiality of such devices in analog circuits.

## II. DEVICE STRUCTURE

This device contains three N-MOSFET transistors in parallel, consisting of three independent channels connected between Source and Drain. As shown in Fig 1 three separate gates can be differentiated, a surface gate ( $V_G$ ) and two lateral gates ( $V_{LTG}$ ). The lateral gates are connected together. We therefore have a surface channel and two side-wall channels. If the surface gate is biased and the lateral gates are grounded, the structure operates as a conventional MOSFET transistor; the channel is formed just below the surface gate and depends only on this gate. The operation of this channel can be changed if the lateral gate is biased with a positive voltage. When the lateral gate is turned on, the lateral MOSFET transistor is activated; this may shift the threshold voltage of the surface channel. The wider the device, the lesser the impact of the lateral channels on the surface channel. Therefore the threshold of the surface transistor depends on the bias applied to the lateral gate and on the effective width  $W$  of the device. This device can also work in a different way, by turning off the surface gate and activating just the lateral ones. This results in a side-wall current composed of several contributions. These contributions are strongly dependent on the doping profile of the pockets and the bulk. An activation of the surface transistor can affect one of the lateral channel's contributions. The study of the lateral transistor is developed in the next section.

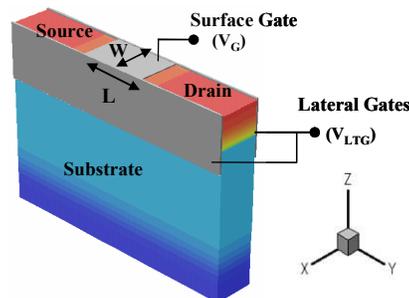


Fig. 1. Structure of the multi-gate MOSFET.

### III. CURRENT-VOLTAGE CHARACTERISATION

#### A. Surface and lateral channels

The surface transistor is studied by turning off the lateral transistor ( $V_{LTG}=0V$ ). The lateral transistor is studied by turning off the surface transistor ( $V_G=0V$ ). The device structure is symmetric, so that only one lateral gate needs to be considered.

To evaluate the operation of the device, TCAD simulations have been performed [4]. The simulated structure is shown in Fig 2. The surface gate area is  $0.2 \times 0.35 \mu m$ . The lateral oxide depth is  $0.3 \mu m$ . The Source/Drain junction depth is  $0.13 \mu m$ , and the extensions junction depth is  $0.02 \mu m$ . The doping concentration of the pockets and the bulk are  $1 \times 10^{18} cm^{-3}$  and  $1 \times 10^{15} cm^{-3}$  respectively.

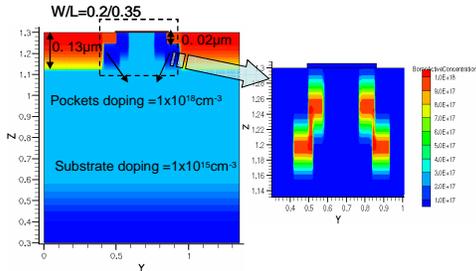


Fig. 2: TCAD simulated structure.

The surface transistor presents standard bulk MOSFET characteristics. Fig. 3 shows the simulated  $I_D(V_G)$  and  $g_m(V_G)$  characteristics of the lateral transistor.

In comparison to the surface transistor, Fig. 3 presents anomalous  $I_D(V_{LTG})$  and  $g_m(V_{LTG})$  characteristics related to lateral gate transistor. Three different sub-channels, (1), (2) and (3) forming the lateral current are identified on Fig. 3. In order to illustrate these different contributions, Figs. 4, 5 and 6 report three different lateral cross-sections at the  $SiO_2/Si$  lateral interface showing the current density in the structure.

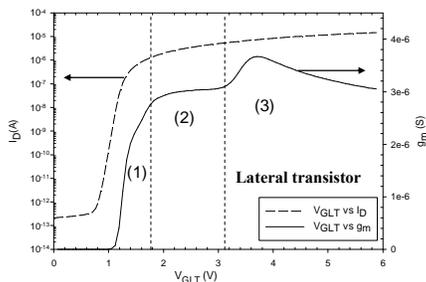


Fig. 3 Simulated  $I_D(V_{LTG})$  and  $g_m(V_{LTG})$  characteristics of the lateral transistor

A lateral cross-section of the simulated structure illustrating the current density of the sub-channel (1) is

shown in Fig. 4. The first current contribution is a deep channel created between Source and Drain, in the bulk of the transistor. The threshold voltage of this channel is strongly dependent on the doping concentration of the substrate ( $10^{15} cm^{-3}$ ) and its effective width  $W_{Lat1}$  is directly related to the depth of the lateral oxide trench.

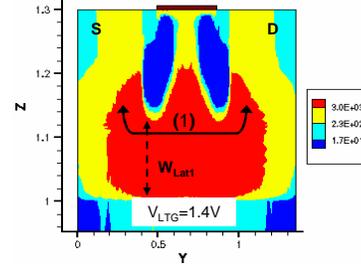


Fig. 4: TCAD simulation results of the multi-gate device for  $V_{LTG} = 1.4 V$  and  $V_G = 0 V$  showing the first lateral current

Fig. 5 and 6 show lateral cross-sections of the structure illustrating the current density in the sub-channels (2) and (3). Fig 5 shows that once the deep sub-channel is formed, a surface sub-channel (2) is created on the top side-wall of the device. This channel is located where the doping concentration of the pockets is the lowest. Fig. 6 shows the third sub-channel (3) contribution created through the pockets. The threshold of this current (3) is shifted as the doping concentration of the pockets increases. The effective widths  $W_{Lat2}$  and  $W_{Lat3}$  of these last two sub-channels are strongly dependent on the doping concentration profile of the pockets.

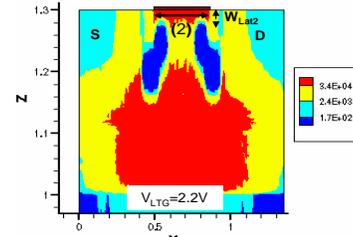


Fig. 5: TCAD-Simulation results of the multi-gate device for  $V_{LTG} = 2.2 V$  and  $V_G = 0 V$  showing the second lateral current.

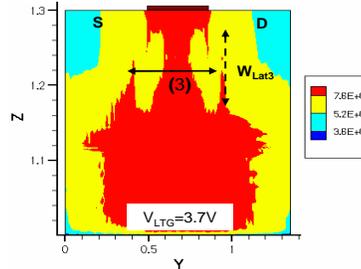


Fig. 6: TCAD-Simulation results of the multi-gate device for  $V_{LTG} = 3.7 V$  and  $V_G = 0 V$  showing the third lateral current.

### B. Compact model formulation

As TCAD simulations exhibit multi-channel contributions in the lateral gate transistor operation, we propose a simple compact model consisting of three parallel MOSFETs.

Each transistor model is based on the surface potential model [5]. The parameters involved for each transistor are the substrate doping concentration and the carrier mobility related to each region of the sub-channels. The width and length of each current contribution and the oxide thickness of the lateral gate are also model parameters. In the next section, we present a fit of experimental lateral transistor characteristics using this model.

## IV. EXPERIMENTAL RESULTS AND DISCUSSION

DC and low frequency noise characterizations were carried out on several devices for different geometries. In this section we present the DC and low frequency noise analysis performed on a device with a surface gate area of  $0.2 \mu\text{m} \times 0.35 \mu\text{m}$ . The oxide thickness of the surface and lateral gates are  $T_{\text{ox}} = 6 \text{ nm}$  and  $T_{\text{ox}} = 10.5 \text{ nm}$  respectively.

### A. Experimental Set-up

A complete current-voltage characterization using an Agilent 4156C semiconductor parameter analyzer was performed before noise measurements. Low-frequency noise measurements were performed using a HP89410A dynamic signal analyzer loaded by a high sensitivity programmable bias amplifier (PBA).

The drain voltage is set to  $V_D = 25 \text{ mV}$ , and the gate voltage ranges from weak to strong inversion. The surface transistor is measured by setting the lateral gate to zero ( $V_{\text{LTG}} = 0 \text{ V}$ ). The lateral transistor is measured by setting the surface gate to zero ( $V_G = 0 \text{ V}$ ).

### B. DC characterization

Typical DC drain current evolutions versus surface and lateral gate voltages are reported in Fig. 7. Experimental DC characteristics show the same behaviour reported by TCAD simulations for the surface transistor.

Concerning the lateral transistor,  $I_D(V_{\text{LTG}})$  characteristics illustrate the presence of four contributions forming the lateral current, while TCAD DC characteristics exhibit only three sub-channels. According to TCAD simulations the fourth sub-channel is related to a corner effect [6]. For simplicity's sake, this current contribution isn't illustrated.

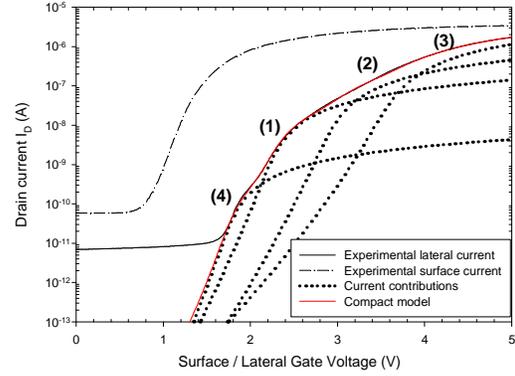


Fig. 7: Surface and Lateral measured characteristics of the device ( $W = 0.2 \mu\text{m}$ ,  $L = 0.35 \mu\text{m}$ ).  $I_D(V_{\text{LTG}})$  is measured with  $V_G = 0 \text{ V}$  and  $I_D(V_G)$  is measured with  $V_{\text{LTG}} = 0 \text{ V}$

### C. Low frequency noise results and discussion

Low-frequency noise measurements were performed on the drain current in both surface and lateral transistor modes. The power spectral densities show  $1/f$  dependence for the drain current. RTS (Random Telegraph Signal) noise was equally observed on this device but these results are not reported here. The low-frequency noise level at 1 Hz was reported for both surface and lateral transistors.

#### a. Surface transistor characterisation

Fig. 8 shows surface transistor's relative drain current noise at  $f = 1 \text{ Hz}$  versus drain current from weak to strong inversion. The magnitude of the  $1/f$  noise follows the carrier number fluctuation model ( $\Delta N$  model). The  $\Delta N$  model supposes that the number fluctuation of insulator charge may induce fluctuations in flat-band voltage. The relative drain current noise power spectral density is expressed as [7]:

$$\frac{S_{I_D}(f)}{I_D^2} = \left( \frac{g_m}{I_D} \right)^2 S_{V_{\text{FB}}} \quad (1)$$

with :

$$S_{V_{\text{FB}}} = \frac{q^2 k T N_T (E_{\text{Fn}})}{\lambda f W L C_{\text{OX}}^2} \quad (2)$$

where  $\lambda$  is the tunnelling constant and  $N_t(E_{\text{Fn}})$  the oxide trap density at electron quasi-Fermi level.

For all devices, the slow oxide trap densities are between  $N_t(E_{\text{Fn}}) = 10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$  and  $N_t(E_{\text{Fn}}) = 10^{17} \text{ cm}^{-3} \text{ eV}^{-1}$ . These values are in the range of those reported in literature for nitrided oxide with an oxide thickness of 6 nm [8-9].

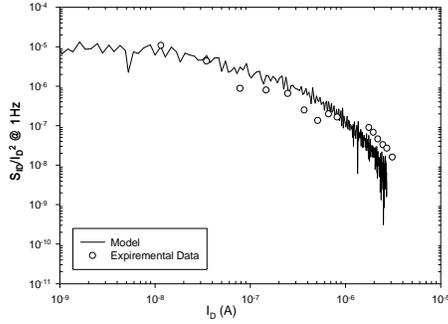


Fig. 8: Experimental relative spectral density at  $f=1$  Hz of the drain current noise of the surface transistor at  $V_D=25$  mV for  $0.2\mu\text{m} \times 0.35\mu\text{m}$ .

### b. Lateral transistor characterisation

Fig. 9 shows lateral transistor's relative drain current at  $f=1$  Hz versus drain current from weak to strong inversion. For every sub-channel, the  $1/f$  noise follows the variation of the corresponding  $g_m$ . This means that the lateral transistor's noise behaviour is equivalent to a conventional MOSFET transistor, following the carrier number fluctuation model ( $\Delta N$  model). Therefore the relative spectral densities can be modelled by the expression:

$$\frac{S_{I_D}(f)}{I_D^2} = \sum_i \left( \frac{g_{m_i}}{I_D} \right)^2 S_{V_{FB_i}} \quad (4)$$

The extracted value of the trap density at the  $\text{SiO}_2/\text{Si}$  lateral interface is different for every sub-channel. This is related to the non-homogenous doping concentration in the different sub-channels regions

For all measured devices, the extracted trap densities are ranging between  $N_t(E_{Fn})=10^{15}\text{cm}^{-3}\text{eV}^{-1}$  and  $N_t(E_{Fn})=10^{17}\text{cm}^{-3}\text{eV}^{-1}$ . These values are comparable to those extracted for other technologies [9].

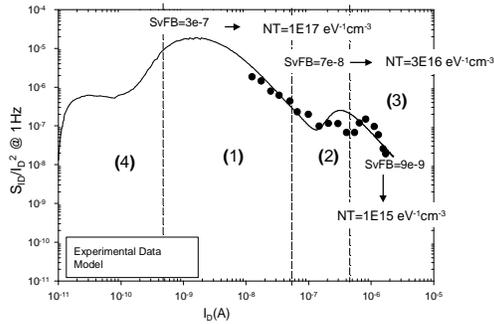


Fig. 9: Measured relative spectral densities at  $f=1$  Hz of the drain current noise at  $V_D=25$  mV

## V. CONCLUSION

We have presented DC and low frequency noise characterisation of a multi-gate N-MOSFET in a standard bulk technology with integration of polysilicon-

filled trenches. Lateral-gate and surface-gate transistors have been investigated. The surface gate transistor behaves like a conventional transistor with adjustable threshold by lateral-gate bias. TCAD simulations have been performed to evaluate the multiple sub-channels of the lateral gate transistor. These different contributions induce anomalous I-V lateral characteristics. Finally, a compact model of the lateral transistor has been proposed, and experimental data have been fitted with the model.

Low frequency noise measurements were carried out on both surface and lateral transistors. Slow oxide trap densities involved in low frequency noise have been extracted for both surface and lateral oxide. Trap densities of the surface oxide are between  $N_t(E_{Fn})=10^{16}\text{cm}^{-3}\text{eV}^{-1}$  and  $N_t(E_{Fn})=10^{17}\text{cm}^{-3}\text{eV}^{-1}$  whereas the lateral ones are ranging from  $N_t(E_{Fn})=10^{15}\text{cm}^{-3}\text{eV}^{-1}$  to  $N_t(E_{Fn})=10^{17}\text{cm}^{-3}\text{eV}^{-1}$ . The trap density values extracted for the surface and lateral transistors are comparable to those reported in the literature for equivalent oxide thickness. Consequently, these devices can be considered as a good candidate for analog applications.

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