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Analysis of the degradation mechanisms occurring in the topside interconnections of IGBT power devices during power cycling

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ABSTRACT

This paper presents an experimental technique to characterize the damage evolution of the topside interconnections of power semi-conductor devices during power cycling tests. DC power cycling tests are done on Semikron SKIM 63 power modules, a solder-free module with silver sintered chips, ensuring the degradations to appear in the top layers only. The cycled substrates are then extracted from the test bench at different steps of the aging for analysis. Four-probe measurements are implemented on the chips so that the evolution of physical parameters representative of the degradation in the metallization and the bond wire contacts can be obtained. Finally, optical microscopy analysis of cross-sections at the wire bond contact interface is carried out to corroborate the electrical measurements to the crack length growth after specific aging intervals.

1. Introduction

The topside interconnections in power semi-conductor devices, consisting of the metallization and the wire bonds, are subjected in operation to high functional stresses. This is the result of an important difference between the coefficients of thermal expansion (CTE) of the materials in contact: metallization and wire bonds (aluminum) and dies (silicon). The metallization layer (around 5 μm) deposited on the chips becomes a lot more distorted than the silicon with temperature, leading to high tensile and compressive stresses and thus to large inelastic strains [1].

It has been reported that two main types of degradation can take place in the topside of power chips under the effect of thermo-mechanical cycles: metallization reconstruction and degradation of bonding contacts [1–3]. The last one may itself be either heel-cracks or cracks propagation followed by lift-off [4]. Various works have been conducted to propose scenarios of degradation mechanisms using thermal and power cycling tests [5–7]. Although it is quite clear that the wire-bond lift-off contributes mainly to the module failure [8], this link is not obvious with the metallization degradation [6].

During power cycling tests, a classical aging indicator is the increase of forward drop voltage (V_{CE}). Usually, its monitoring indicates a slow and gradual increase before faster changes at the end of life [9]. The first period is classically associated with the reconstruction of the metallization and the degradation of the bonding contact. The end of life is rather characterized by bond-wire heel-cracks and lift-off [10].

This paper is a contribution to a better understanding of the effects

of power cycles, i.e. stress parameters, on the degradation mechanisms appearing in the first period mentioned above, by using specific characterizations. Namely, power cycling tests have been performed on dedicated power modules where only the degradation of top-side interconnections can occur. Specific measurements of metallization and bond-wire contact resistance were carried out along the aging in order to highlight the role of stress parameters on these degradations. The final objective is to assess the weight between both degradation types on the increase in the on-state voltage V_{CE} during power cycling tests.

2. Preliminary observations

2.1. Tested device

The tested modules are commercially available SKIM63 (1200 V-300A) (Ref. SKiM306GD12E4), produced by Semikron. These devices are six-pack modules with three individual phase legs on separated DBC substrates. These power modules were chosen for their solder-free die attach in order to concentrate the degradations only in the topside interconnections. The chips are all sintered with a nanoparticle silver paste, making the connections stronger than with classical solders. Hence, the degradations observed concern only the metallization and the bonds contacts.

The power cycling is carried out only on the central leg of tested modules which constitutes 2 DUTs, respectively high side and low side switches as visible in Fig. 1. Each DUT includes 4 IGBTs and 2 diodes on the DBC. All the IGBT chips in the substrate are aged.

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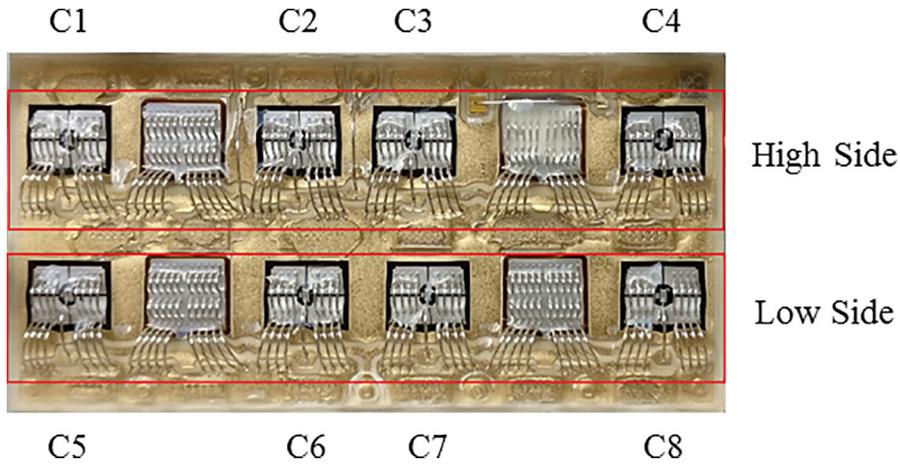


Fig. 1. Substrate of SKIM63 power module from Semikron.

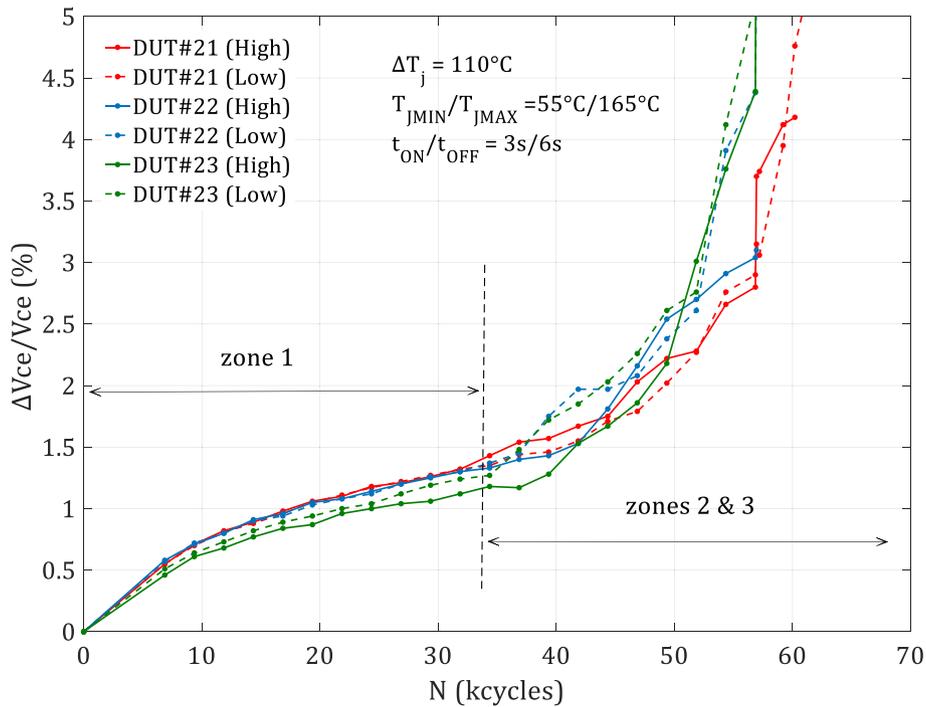


Fig. 2. Evolution of corrected collector-emitter voltage V_{CE} for $\Delta T_j = 110^\circ\text{C}$, $T_{j\min} = 55^\circ\text{C}$ and $t_{\text{on}}/t_{\text{off}} = 3\text{ s}/6\text{ s}$. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

Table 1
DC power cycling results.

DUT	$\Delta V_{CE}/V_{CE}$ (%)		N (cycles)
	High side	Low side	
M1	0.35	0.49	3000
M2	0.41	0.46	6000
M3	0.65	0.73	10,000
M4	0.76	0.69	14,000
M5	0.98	1.27	24,000
M6	1.15	1.35	30,000

2.2. DC power cycling

Two series of power cycling tests (PCTs) have been performed with constant ΔT_j strategy by controlling the gate voltage. The first one was done in order to get the general aging behaviour of the DUTs, and in the

second one were added specific measurements during aging. The constant ΔT_j strategy was chosen to control the stress and thus the damages in the top-side of the DUTs.

The first series of accelerated power cycling tests in DC-mode have been done on the modules presented in Section 2.1 with different tests conditions in junction temperature swing ($\Delta T_j = 70\text{ K}, 90\text{ K}, 110\text{ K}$) and heating time ($t_{\text{ON}} = 3\text{ s}, 20\text{ s}$). A dedicated methodology and instrumentation were implemented in order to monitor aging indicators with a high accuracy. One of the aging indicator, the on-state voltage (V_{CE}), is corrected from any possible increase in thermal resistance. However, no degradation in thermal resistance such as die-attach delamination has been detected.

As a typical result, the evolution of the on-state voltage V_{CE} , measured continuously during aging until reaching the failure criteria of the modules (corresponding to 5% increase in V_{CE}), is shown in Fig. 2. The test conditions in this case are $\Delta T_j = 110\text{ K}$, $t_{\text{ON}} = 3\text{ s}$, $t_{\text{OFF}} = 6\text{ s}$, $T_{j\min} = 55^\circ\text{C}$. The results show that the curves for all DUTs can be decomposed in three zones. The first zone corresponds to a progressive

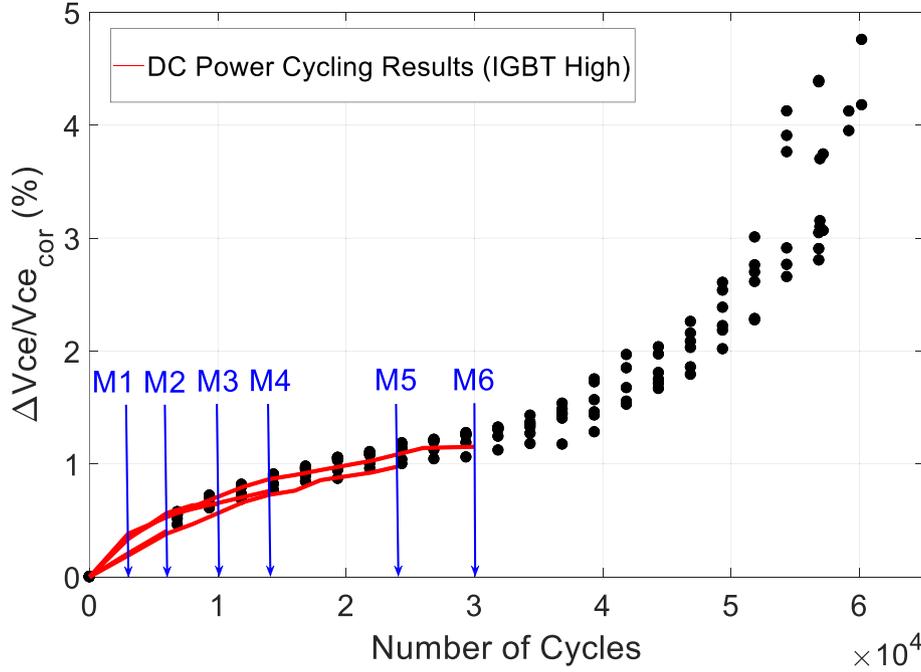


Fig. 3. Evolution of corrected collector-emitter voltage V_{CE} for $\Delta T_j = 110^\circ\text{C}$, $T_{j\min} = 55^\circ\text{C}$ and $t_{on}/t_{off} = 3\text{ s}/6\text{ s}$.

evolution of the V_{CE} until an apparent saturation around 1.3%. The second zone exhibits rather an exponential increase of V_{CE} and zone three a sharp and stepped increase, representative of the bond-wire lift-off. These observations have been also systematically observed for all others tests conditions (ΔT_j of 70°C and 90°C).

Considering that the SKIM63 are specific modules for which the damages are concentrated in the topside interconnections, only the wire bonds contacts and the metallization can affect the on-state voltage V_{CE} . As explained previously, the first zone is usually presented to be affected by the damages in the metallization and the bonding contacts, letting the bond-wire heel-cracks and lift-off be responsible for the exponential and stepped increase of zones 2 and 3.

To verify this assumption, additional power cycling is conducted with specific measurements on the top side of the power dies. For this purpose, the test bench is regularly stopped at different steps during the aging before reaching 5% of V_{CE} . Device samples are then extracted, i.e. completely removed from the test bench, in order to realize specific electrical characterizations in top-metallization and bond contacts. As this operation is destructive, the power cycling continues with new DUTs. The main hypothesis is considered that all DUTs are aging in the same way under the same stress conditions. This hypothesis is supported by the tests already carried out under different conditions mentioned above in Fig. 2, which show a fairly reproductive aging despite the inaccuracies related to PCT tests.

3. Specific power cycling tests

3.1. Methodology

The chosen test conditions for this specific power cycling are as follows: a ΔT_j of 110°C , a $T_{j\min}$ of 55°C and a t_{ON} of 3 s that should lead to the same results as those presented in Fig. 2. The PCT is interrupted as usual for aging indicator characterizations, but also sometimes as stated in Section 2.2 for the removal of a device from the test bench to analyse its degradation. The operation being destructive, the device cannot be cycled again. As already stated, the assumption is made that the degradations occur in the same way in all the tested devices.

In a first step, electrical characterizations of the metallization sheet-layer and the wire bonds contacts are done on all the IGBT dies of all the cycled substrates. These characterizations are performed by using a four-probe sensing as detailed in Section 5. Then, in order to quantify the degradations at the wire bond contacts and to corroborate the obtained electrical results, damage analyses on cross-sections are done on the four central chips of each substrate (C2, C3, C6 and C7 in Fig. 1) using optical microscope.

3.2. Results

The results in relative variation of V_{CE} during the DC power cycling are summarized on Table 1 and shown in Fig. 3. Six modules are aged at the same time on the test bench for the test conditions presented in Section 3. As these DUTs have been extracted at different steps of aging, their values in relative increase of V_{CE} differ.

As a result, different health states are obtained and thus an evolution of the degradations as a function of the aging. Only the zone 1 indicated in Fig. 2 is investigated here.

As shown in Fig. 3, the main assumption that all DUTs will age in the same way under the same stress conditions seems quite well verified. Indeed, a good consistency has been found between the aging curve tendency known from previous tests presented in Fig. 2 (black points) and this specific DC power cycling results (red curves).

The nature of degradations hidden behind this progressive evolution of the V_{CE} can be determined by having a precise evolution of the parameters representatives of the damage in this zone. For this purpose, specific electrical characterizations using four-probe instrumentation have been carried out and are presented in the next paragraph.

4. Specific electrical characterization results

The Fig. 4a shows the experimental set-up. Four-point instrumentation involving contact tips are used for electrical measurements. These tips are inserted into ceramic guides in pairs (see Fig. 4a). The four tips with their respective guide are then all assembled to ensure the rigidity of the measuring device and maintain constant the

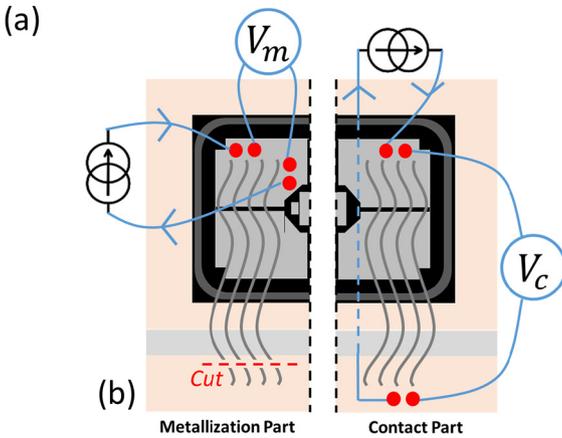
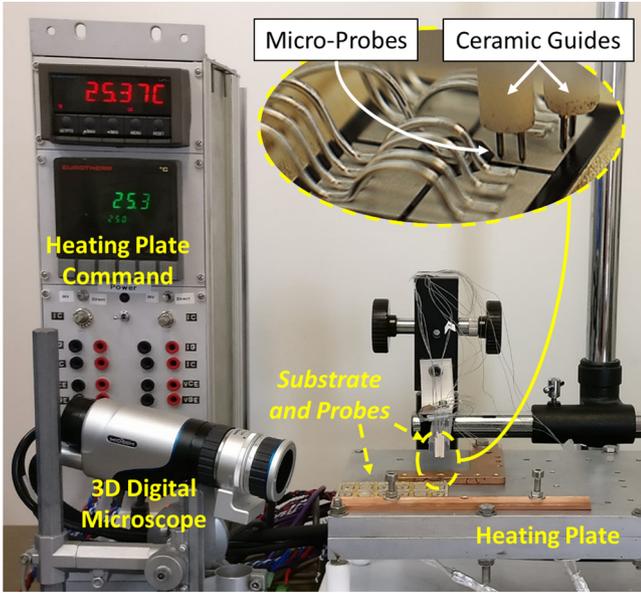


Fig. 4. (a) Experimental set-up for the measurement of V_m and V_C with a zoom view on the chip and the 4-probes, (b) schematic of the positions of the probes on the chip.

distances between the four probes. A 3D digital microscope is used to locate properly the good positioning of the probes on the metal pad (see Fig. 4a). The DUTs are fixed on a thermally regulated plate to ensure temperature stability and investigate temperature effects. Measurements are performed using a low injected current of 10 mA to avoid self-heating. Finally, all the measurements are done with a nanovoltmeter (Keithley 2182A) procuring an accuracy of $\pm 0.02 \mu\text{V}$ in the used range.

These electrical measurements were carried out on all the IGBT chips of the six aged substrates. A schematic of the micro-probes instrumentation is shown in Fig. 4b. To facilitate the measurements, each chip has been divided in two parts: the right part on which the change in the wire bonds contact resistance is measured via the contact voltage V_C , and the left part for the metallization resistance measurements (i.e. metallization voltage V_m). In addition, the connections between wire bonds and DCB on the left side are cut off for two reasons: to ensure no current leakage through the wires for V_m measurements, and to impose a current through the right side wire bonds only for V_C evaluation. This instrumentation presents some drawbacks: V_m is only measured on one pad and V_C , which represents only the first stitches of the four parallel bond-wires, includes a small metallization part to access the wire bonds.

4.1. Metallization results

The evolution of the metallization voltage V_m versus aging is presented in Fig. 5. Here, only the four IGBT chips data of the high side (C1, C2, C3 and C4 of Fig. 1) are plotted for illustration. The initial V_m has been measured on all the chips of a healthy substrate and the mean value $50.39 \mu\text{V}$ has been used as reference. Indeed, very little disparity was found in the measurements with a mean absolute difference calculated on all the eight IGBTs of $0.93 \mu\text{V}$.

The curve indicates that the damages in the metallization appear immediately at the beginning of the aging. In addition, a V_m increase of around 25% is visible for a V_{CE} increase of 1.15%, corresponding approximately to the end of the first zone of the aging curve (see Section 2.2). The results show that the evolution seems quite linear for this part of the aging. However, a slight decrease of the rate of rise seems to appear at the end. SEM images performed on the cycled modules M1, M3 and M5 presented in Fig. 6 support these observations. These images were taken in the same area of the metallization for all chips and with the same magnification. Indeed, a progressive reconstruction of the metallization layer is visible from 0 Cycle to 24 kCycles. Moreover, the Al reconstruction of the M5 module seems to be really advanced and underpins the idea of a decreasing rate of rise of V_m for a greater relative variation of V_{CE} . Some authors have already described this phenomenon and shown that the resistance evolution of the metallization tend to saturate after a certain amount of cycles [6]. Nevertheless, more tests need to be performed for modules aged after 30 kCycles to confirm this hypothesis.

The cause of this increase in metallization resistance can be either due to a change in the aluminum resistivity because of chemical reactions, or a modification of the geometry due to metal reconstruction. More measurements were done at different temperature levels for the modules M1, M3, M5, and a healthy module to identify the cause of this increase in resistance. The results presented in Fig. 7 show the temperature dependence of the metallization resistance (R_m) calculated using V_m and I_{sense} . A linear relation between R_m and the temperature is found for the healthy state, which is consistent. Moreover, this linear tendency seems to be unchanged with the aging, the difference of slope for M1 and M3 being probably due to inaccuracies of the measurements. However, a translation of the curves is visible with the aging. Change in the geometry of the metallization could be the reason of such a shift.

Studies focused on the metallization fatigue presented in [6, 11] showed indeed that micro-structural changes are occurring inside this material layer during aging. In both cases, cracks were observed in the metallization, starting from the surface and propagating through the layer. Moreover, oxidation of the aluminum has also been detected and it is shown that it participates in the crack propagation. However, the authors in [11] indicate that this oxidation might constrain the dislocations motion inside the metallization, leading to a reduced damaging. A focus on the changes occurring in the crystallographic structure of the metallization was then made in [12]. Grains reorientation and sub-grains formation were observed during the aging, giving information on the root of the damages occurring in the metallization.

4.2. Contacts results

The evolution of the “contacts voltage” V_C in function of the relative increase in V_{CE} is shown in Fig. 8. Like the metallization results, only the data of the four high side IGBTs are plotted. In this case, the mean absolute difference between chips for the “healthy” point is $1.05 \mu\text{V}$.

From the healthy state until around 0.6% increase in V_{CE} , the evolution of V_C is similar to the V_m one. But from DUT M3, V_C seems to increase faster than V_m until reaching almost 40% of its initial value for

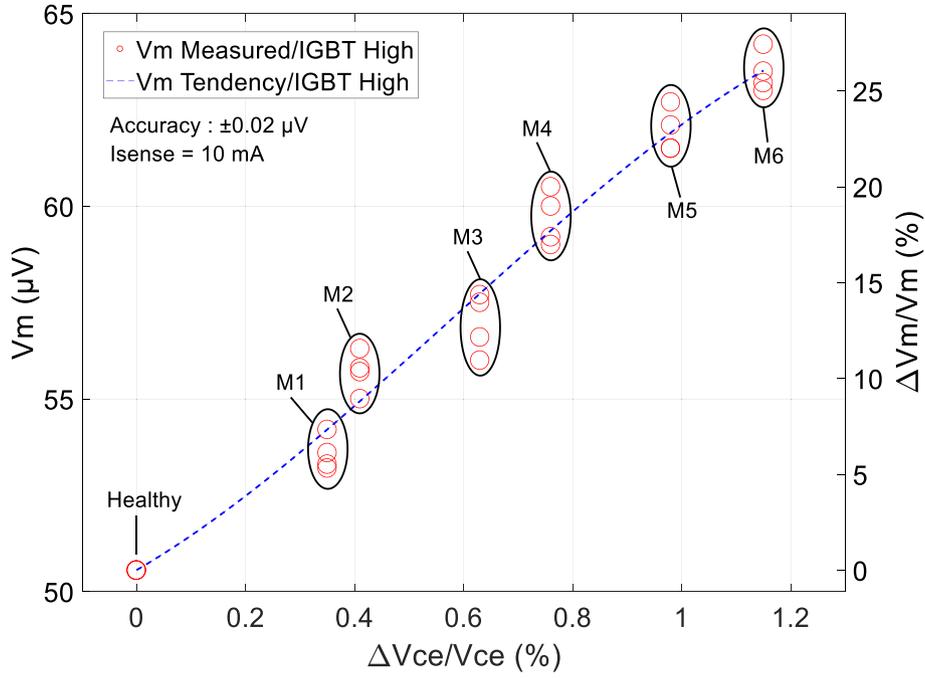


Fig. 5. Evolution of V_m as a dependence of the relative variation of V_{CE} for high side IGBTs at 25 °C.

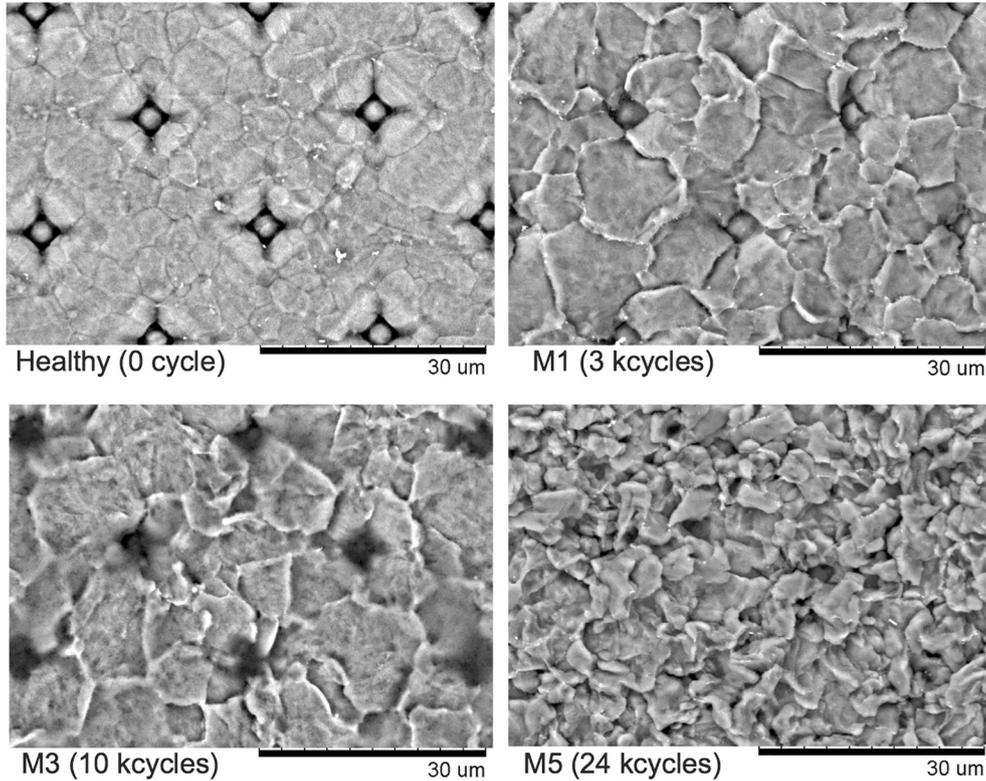


Fig. 6. SEM images of the Al Metallization for a healthy module and aged modules M1, M3 and M5.

a rise of 1.2% of V_{CE} . In comparison, the metallization voltage V_m had reached only 25% of its initial value for the same health state.

These results can be explained by the fact that a non-negligible metallization resistance is taken into account when measuring the contact voltage V_C . Considering that the metallization is very thin compared to the wire bonds (5 μm comparatively to 250 μm wire diameter), its impact on the voltage can be important. It is considered that from M2 or M3 aging stage, i.e. approximately 0.5% increase in V_{CE} , the

effect of degradations in the contacts begin to dominate compared to those in the metallization, leading to a faster increase of V_C . The optical microscopy observations on cross-sections presented in the next paragraph support this assumption.

5. Cross-sections observation results

Cross-sections were made on the aged modules M2, M4 and M6

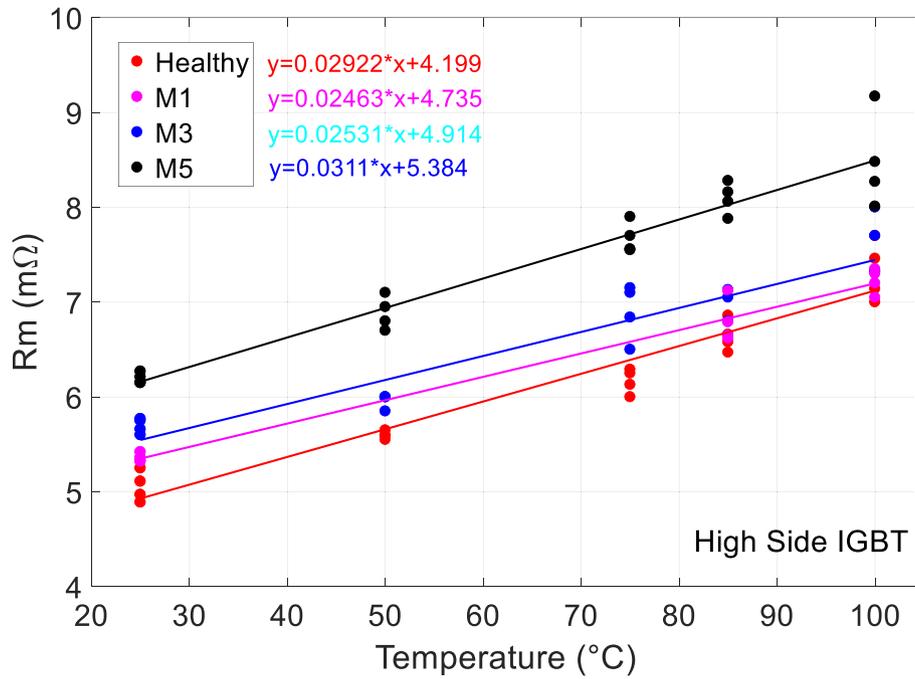


Fig. 7. Evolution of R_m in function of temperature for high side IGBTs.

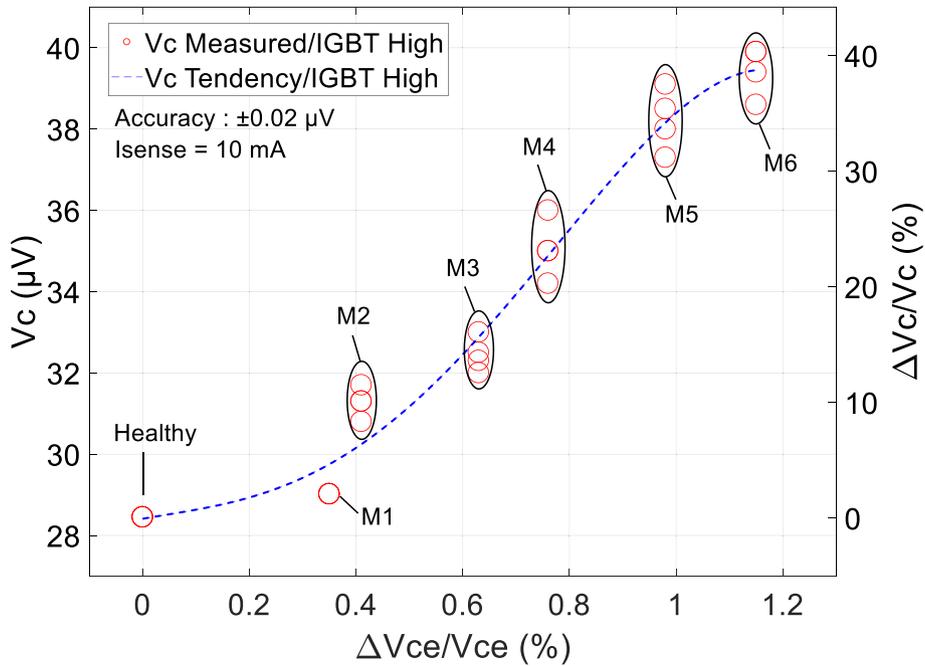


Fig. 8. Evolution of V_c in function of V_{CE} for high side IGBTs at 25 °C.

(respectively 6 kCycles, 14 kCycles and 30 kCycles) to obtain an evolution of the cracks propagation at the interface between the metallization and wire bonds. A healthy module was also analyzed for comparison. The images obtained are shown in Figs. 9 and 10.

The analysis of the healthy module shows that initial defects are visible in the interface. Pre-cracks are indeed detected at the contact edges. This weak zone corresponds with the initiation area where the

cracks appear and begin to propagate inside the wire bonds. These pre-cracks are the results of the ultrasonic bonding process when the wire bonds are welded to the metallization. Additionally, these results agree with previous studies [5, 13].

Fig. 10a presents the cross-section of a wire bond aged for only 6 kCycles, i.e. approximately 10% of the number of cycles to failure N_f . The initiation of the cracks at the edges of the interface has already

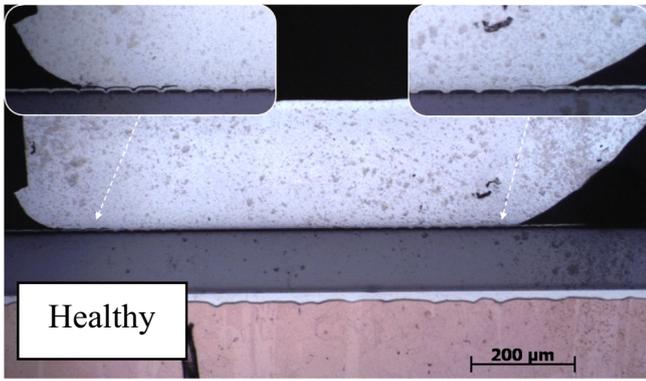


Fig. 9. Microscopic cross-sections of a healthy module.

begun. However, the decrease of the contact area is not important enough to have a significant impact on the contact voltage V_C compared to the damages in the metallization. On the other hand, in the cross-section shown in Fig. 10b, the cracks have propagated much further

into the center of the interface. The wire bond in this case has cycled for 30 kCycles ($\sim 50\%N_f$).

The Table 2 summarizes the results obtained from cross-sections analysis. The lengths data are all averaged on a complete module. The ratio between the initial ($L_{initial}$) and final (L_{final}) contact length at different steps of the aging seems to indicate that the crack propagation is linear, at least until 30 kCycles. Further analysis on modules aged beyond 30 kCycles need to be performed to obtain the tendency of the crack propagation speed near the failure.

6. Conclusion

Accelerated aging tests were performed on six Semikron Modules SKIM63 to relate the evolution of physical parameter with the damage. An electrical analysis was performed on the metallization and shows that the sheet resistance increases from the beginning of the aging. However, its rate of rise decreases at a certain point, potentially indicating a saturation in the metallization resistance after a certain amount of physical damage. SEM analysis of metallization of aged modules also supports this hypothesis. Additional electrical measurements were performed on the bond contacts. The results led to the

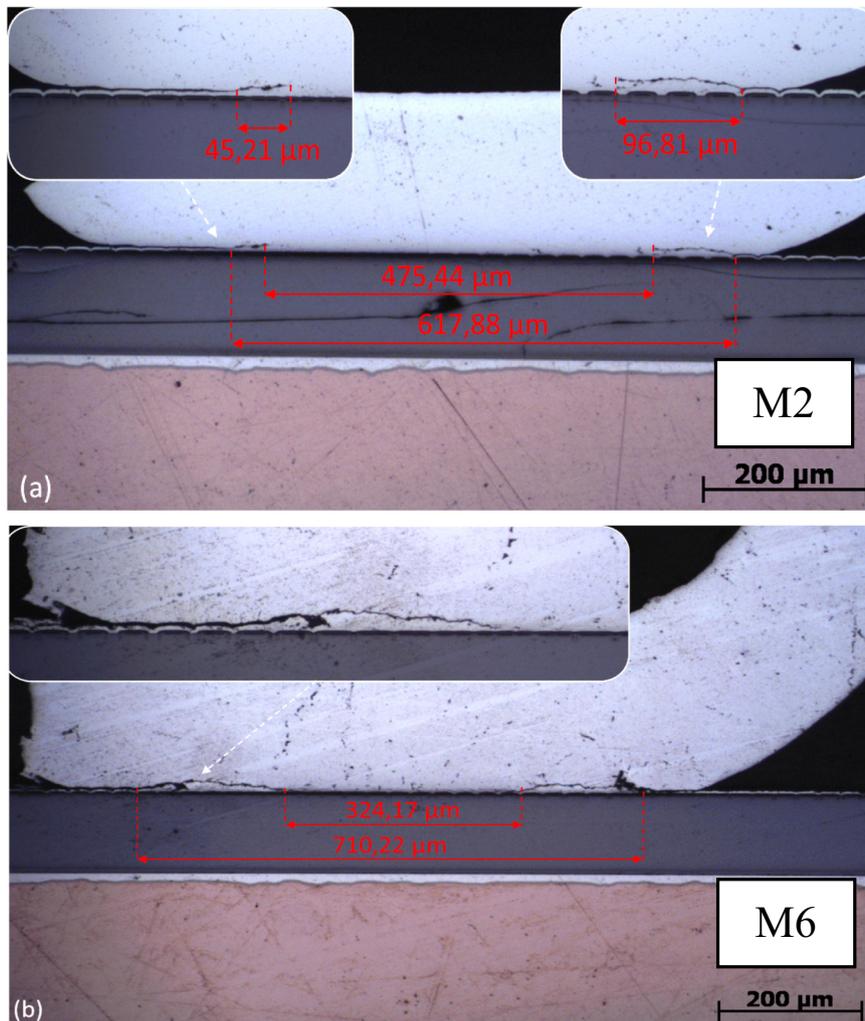


Fig. 10. Microscopic cross-sections (a) module M2 chip C2 (b) module M6 chip C2.

Table 2

Microscopic cross-sections results.

DUT	$L_{Final}/L_{Initial}$ (%)	N (Cycles)
M2	72.7	6000 (10% N_f)
M4	56.6	14,000 (23% N_f)
M6	25.1	30,000 (50% N_f)

conclusion that the damages in the metallization are prevailing on the contacts degradations in the early stages of the aging. However, after a certain amount of damages corresponding to around 20% of N_f , the damages in the bond contacts interface becomes dominating. This has been corroborated by crossed-sections analysis. These also showed that the crack propagation speed seemed to be constant. More analysis is required for the last zones of the aging curve to obtain the evolution of the parameters representatives of the damage near the device failure.

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