Secured Failure Analysis Methodology for Accurate Diagnostic of Defects in GaN HEMT Technologies

Jean-Guy Tartarin, Damien Saugnon, Laurent Bary, Jacques Graffeuil

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***Abstract*— III-V wide bandgap disruptive technology is positioned as a leader for high power segments operating at high frequency or under switching mode. Still, it is needed to investigate these transistors to push the maturity towards higher levels and to address elevated junction temperatures. Concerning analog RF applications, more than two decades of studies lay the main technological process basis. However, if failure signatures and their associated defects are now issues likely to be understood as individual problems, the global failure behavior in active high frequency analog devices still poses challenges to overcome. This paper is a contribution to the failure analysis studies on GaN technologies by providing a methodology for ensuring the validity of the stress analysis; this procedure is suitable even for a single stress test campaign, when usually several accelerated life tests are needed to separate concurrently proceeding effects. This methodology is based on the use of non-destructive and eventually destructive characterization techniques, as well as electrical TCAD modelling.**

***Index Terms*— Failure analysis methodology; GaN HEMT; Reliability; TCAD; Transient & frequency characterization;**

I. Introduction

RELIABILITY studies of solid state technologies have made possible the development of numerous useful tools and methods to identify degradation signatures and to correlate (cross)experiments. Revealed failure mode mechanisms have raised the mastering of technological processes, up to the critical Technology Readiness Level (main gate TRL 5 to 6) needed to secure the markets supplies (with specific requirements according to the targeted missions, as different as space technologies or generic off-the-shelf mainstream technologies). If silicon and gallium arsenide largely employed technologies are now well established, and their qualification procedures correctly classified (usually by the establishment of reliability standards), emergent wide bandgap nitride technologies Gallium Nitride (GaN) cannot be addressed in the same way.

High Electron Mobility Transistors (HEMT) active devices based on GaN technologies are now reaching a sufficiently high TRL to target various market segments; the major application for analog GaN devices concerns the segment of high-power and high-frequencies, used in wireless infrastructures (base stations and backhaul), defense and military systems (radar, jamming, counter-measures, guided weapons, etc.), broadcast and communication satellites (SatCom). From these different markets, it can be distinguished categories of applications that feature the same trend regarding the needed performances, the reliability requirements, the cost, the size/weight or also legacy considerations. For the foundries and brokers, winning the innovation race in terms of performance cannot be dissociated from providing the customers with highly reliable devices. More than twenty industrial laboratories are engaged in the market of GaN HEMT for Radio Frequency (RF) applications, and a summary of long-term accelerated tests on Nitride HEMT carried out by some of these technology brokers can be found in [1]. During the last decades, channel temperature junction has been improved as shown by G. David in its survey of the literature (improvement of MTTF by more than 10^6 factor from 2007 to 2014 @ 150°C, 175°C and 200°C [2]). These advances were achieved thanks to sustained efforts on technological improvement, accompanied by better understanding of the failure signature in GaN devices. But the complexity of the defects root causes in the devices is still to be understood to push these GaN technologies close to their theoretical limits. Parameters involved in the reliability of the devices are related to the design, the processing and the packaging steps. A large variation on the nature of devices is found in the literature (wafer or die level, small or large devices, packaged or naked die). According to the low or high value of TRL, the studies will more concern wafer level and naked die during process improvement phases, whereas packaged devices will be more representative for qualification steps. From the abundant literature concerning this challenging domain of study, a large variety of papers is dedicated to specific failure analysis studies in GaN devices, some of them propose new analysis tools, present a methodology for failure analysis [3][4][5][6][7] or propose a general overview concerning the reliability in GaN devices [8][9][10]. Usually, the identification of a complex failure signature is achieved by performing various stress campaigns under changing conditions to separate effects of

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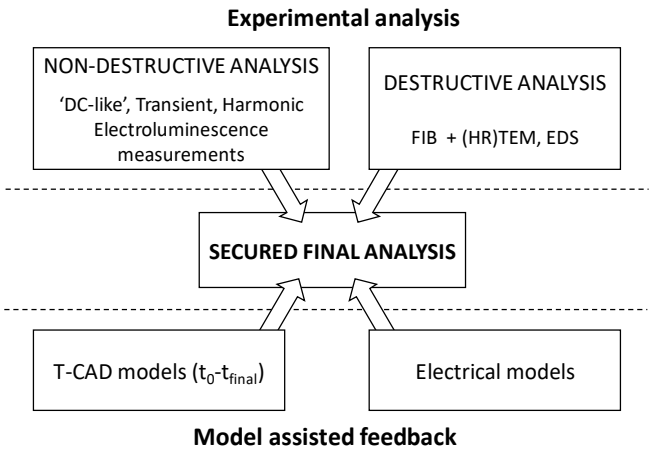


Fig. 1. cross analysis of non-destructive and destructive analysis with electrical models for secured stress analysis. Characterizations are performed on virgin (or initial measurement) and stressed (or final measurement) devices, with possible intermediate measurements. Physical origins of the defect can be assessed, and limits of operation can be defined closely related to the stress conditions.

mechanisms proceeding concurrently to a failure signature. This approach is time-consuming and is not always applicable for studies featuring only one batch of stressed samples. This last study case represents a situation where it is necessary to get numerous parameters from a unique equation – which is impossible if using a single analysis tool.

We propose in this paper a suitable methodology to identify various defects revealed under multi-factor stressing conditions, i.e. DC biasing with temperature and pulsed / Continuous Waves (CW) radiofrequency signal. As stated previously, a large set of experimental workbenches and dedicated models are needed to ensure a realistic and secured diagnostic concerning the failure mechanisms occurring in such technologies, and to establish their physical links. Lastly, a single stress experience will not allow the extraction of any activation energy, and at least three stress campaigns at different temperatures will be needed to extract such parameter from Arrhenius plot. It must be noticed that Arrhenius plots are not considered to accurately account for GaN technologies reliability predictions (even by using scaling factors [4]), and a better knowledge of the concurring defects is much prone to define security operating areas for circuit design.

The proposed methodology (and associated experimental tools or stress workbenches) has been attested and proven over several foundries, and over a large set of DC or RF stresses. Fig.1 summarizes the structure on which the methodology is based; it makes use of experimental analysis and of modelling techniques targeting the final diagnostic on failure root mechanisms.

The paper is divided in four main sections: after this introductive first section, the second one presents the largely accepted stress conditions and tests, the experimental stress workbench developed in our laboratory and RF stresses tests at different output power compression points. In the third section, the experimental diagnostic tools used for the reliability studies are presented, with a highlight on their complementarity (main measurements performed versus time, frequency or temperature). Then section four concerns the development of electrical models (dynamic large signal models for circuit design and reliability analysis, and TCAD models for physical acceptability of the diagnostic). The two last sections summarize the main achieved results and conclude about the need to use a robust methodology for reliability studies of III-N technologies.

II. Stress Conditions and Tests

A. *Main stress tests towards process improvement and process qualification*

According to the final objectives (electrical operating mode, harsh environment, …), reliability tests are needed to find out the first order degradation signature, and its related mechanism to be modeled or solved. Reliability studies aim to make the technology pass the lifetime requirements. When passing a critical lifetime requirement (usually 10 years of operation), then junction temperature requirement can be pushed towards higher limits. So thermal stresses are largely employed during life tests. Usually completed tests by GaN companies according to widely accepted standardized stresses are listed below:

-DC life tests (DCLT): HTRB (High Temperature Reverse Bias), HTOL (High Temperature Operating Life, Fig. 2) and I_{DQ}-I_{GQ} (variations of drain or gate quiescent current at ambient temperature under very deep AB or AB operation class) can be operated at different constant drain-source voltages (V_{DS}), or by step variation. Different parameters are tuned during the stress period (biasing drain current $I_{Dquiescent}$, saturation drain current

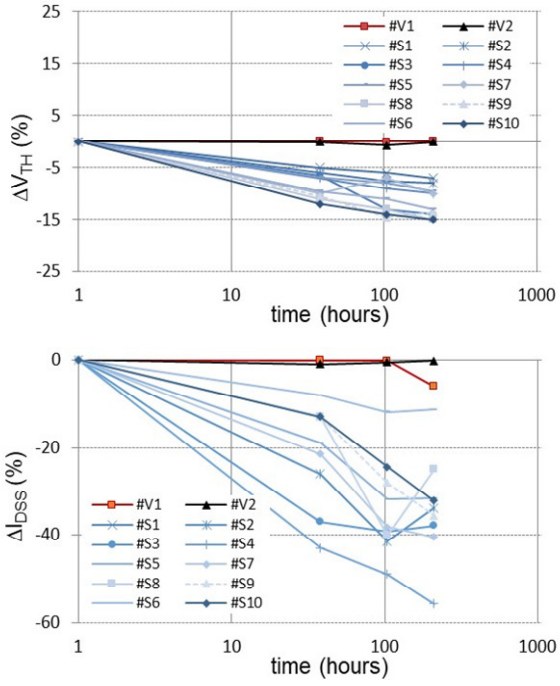


Fig. 2. Example of HTOL stress on a sample of ten 0.25x8x125µm² HEMT devices #S_i (the data for two virgin devices #V_j are also reprensented). Graphs report on the threshold voltage V_{TH} and on the saturation drain current I_{DSS} drifts during 210 hours of stress.

I_{DSS}, threshold voltage V_{th}, leakage currents $I_{G\text{-}leak}$-$I_{D\text{-}leak}$, static transconductance g_m, drain and gate voltages). Stopping condition of the stress is usually given at 10% variation of $I_{Dquiescent}$, or according to a limitation of leakage current before destruction of the gate.

-RF life tests (RFLT): CW at different output power (compression) is convenient to capitalize time variation of the dynamic and static parameters over long times. Step stresses are used to assess the aptitude of the devices to sustain critical RF levels for rugged applications.

-Additive stresses can also be achieved under given ambient conditions (moisture, radiation, mechanical vibration & acceleration, etc…), but generally concerns packaged devices rather than on-wafer transistors.

Each DC life test is time consuming, and several tests are needed to evidence one degradation (acceleration) parameter. RF tests are closer to the application context but more difficult to analyze because of possible conjugated effects; scaling factors are then used on the bases of DC tests, but at the expense of longer analysis period (if 1000 h per single test is performed, over three DC and one RF tests are needed at least, thus corresponding to half a year if cumulated).

B. RF-Thermal experimental stress workbench

For specific application purposes, it can be developed appropriate stress tests. For example, robustness of rugged low noise amplifiers (LNA) versus jamming signals for radar applications needs to study the behavior of the devices/circuits versus RF step stresses (different tests, recovering periods, removing charges procedures). RF stresses are one of the harshest tests as all the DC-thermal-RF swings make the puzzle more difficult with more parameters to consider together. More than ever, setting an appropriate experimental procedure to discriminate between some potentially correlated degrading parameters is needed.

An evolving RF stress workbench with programmable thermal pattern of the oven has been developed. It allows to track static quiescent conditions of the devices under test, dynamic powers at the input/output of the devices (@ RF stress frequency between 0.01 GHz and 40 GHz), and [S] parameters (removing RF-stress for [S] parameters measurement). It is a major issue during RF stresses to keep constant or to get feedback over stability of all the circuitry of the stress workbench, out of the DUTs. This is why temperatures of the oven and that of the ambient room are also monitored (±0.1°C measurement accuracy). More critical, as four different channels are available in our configuration, three channels are devoted to the DUTs, and a control channel is saved to secure the analysis with potential drifts from the driver module (synthesizer and driver power amplifier) (Fig.3). Then, the stability of the calibration is verified at room temperature over 500 hours, and for thermal cycling conditions between -40°C/+100°C over one week (168 hours). The experimental setup features drifts below ± 0.05 dB (resp. ± 1 °) at ambient, and below ± 0.04 dB (resp. +2 °) for - 40 °C/+ 100 °C thermal rectangular cycling, for the magnitude (resp. phase) of [S]

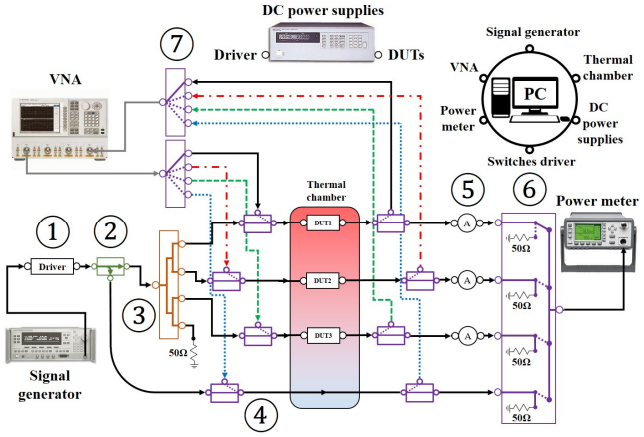


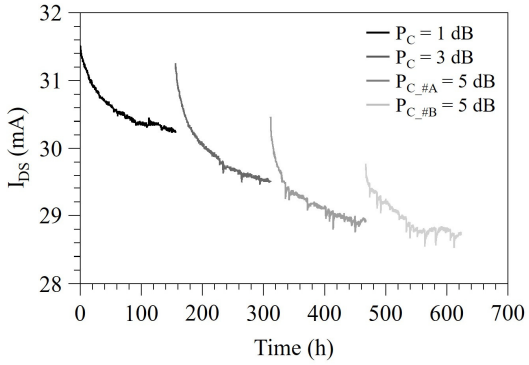
Fig. 3. Schematic of the fully-automated workbench used for RF/thermal stresses using step stresses or CW signals ranging from 0.1 GHz to 40 GHz. Thermal cycles rise and fall slopes are considered for temperature stabilization of the devices (from -40 °C to +150 °C). Vector Network Analyser collects [S] parameters with individual calibration set for each channel at intermediate times (very small variation of the calibration during hot/cold cycles and over a large period of use, less than 0.12dB insertion losses over two weeks). ① power amplifier, ② coupler, ③ four-way power divider, ④ SPDT, ⑤ attenuators, ⑥ SP4T 50Ω RF load terminations and ⑦ SP4T.

parameters. For the main stress paths, the total RF power fluctuations correspond to the drift of the power source HP 83650B (10 MHz to 50 GHz), coupled with the HP 8487A power sensor (50 MHz to 50 GHz) and to the Agilent E4418B power meter measurement uncertainties. The combined power drift at - 40 °C, + 25 °C and + 100 °C is respectively of + 0.01 dB, + 0.03 dB and ± 0.02 dB.

C. Illustration of RF-stresses at different RF compression level of the Device Under Test

CW RF stresses are carried out for a given technology in C-band and X-band. Fig. 4 presents an example of the variation of the drain current I_{DS} and output power P_{OUT} for a representative device under stress at three different output power compression points (1dB, 3dB and twice 5dB). Between each RF-stress, a positive DC voltage V_{GS} = 1 V (shorted drain) can be applied on the DUTs to recover initial electrical state for each device (due to a possible accumulation of charges during the stress). After each RF stress period (1 dB, 3 dB, 5 dB #A and 5 dB #B output power compression points), the drops of the drain-source current ΔI_{DS} are of 3.9%, 5.6%, 5% and 3.4% respectively. The drops for output power ΔP_{OUT} are 10.4%, 13.5%, 10.5% and 7.2% respectively. It is obvious that the change in the static and dynamic plots are more pronounced at elevated compression levels certainly due to higher non-linear effects, as will be discussed in paragraph IV.

Fig. 5 represents these variations of the RF signal versus those of the DC drain current. A linear trend globally results from DC and RF variations, and can be used to model the interdependence of the RF power with the carrier density in the 2DEG channel (i.e. static drain current I_{DS}). From the linear regression of the power versus DC drain current (red plots in Fig. 5), a model can be found using the stress level (in dB) as an acceleration factor of DC and RF degradation with time



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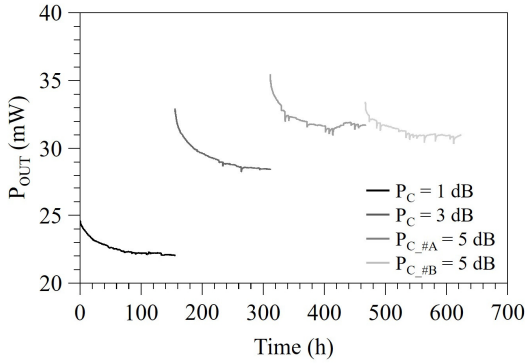
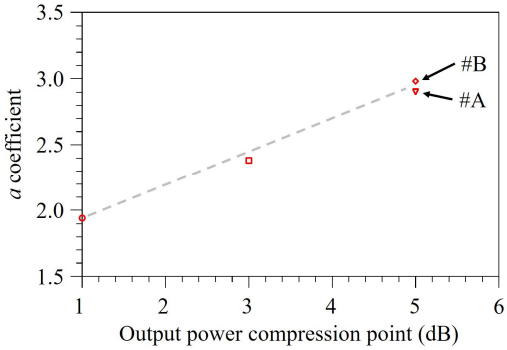


b)

Fig. 4. C-Band CW RF stress impact on a 0.25x2x75 µm² HEMT at chamber temperature of + 25 °C. P_{OUT} versus time at 1 dB, 3 dB and 5 dB (#A and #B) output power compression points for quiescent point at V_{DS} = 15 V and I_{DS} = 35 mA (each stress is applied for 1 week, i.e. 156h for a cumulated 624h of RF stress). a) DC drain current and b) RF output power vs time



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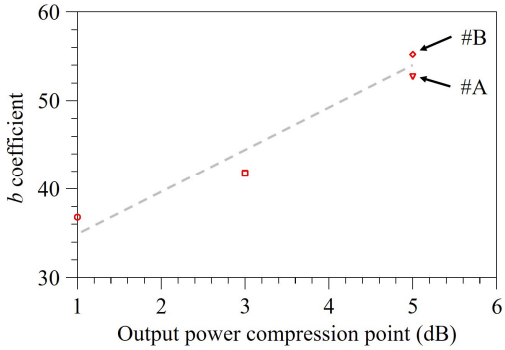


b)

Fig. 6. Affine function coefficients (P_{OUT}= *a* I_{DS} + *b*) for the device under test from Fig. 5, at 1 dB, 3 dB and 5 dB (#A and #B) output power compression point. (a) and (b) shows the relation between the activated degradation mechanism number during the stress (red linear regressions from Fig. 5).

(Fig. 6). Specific behaviors at the end of the 5dB compression RF stress (dotted rectangular area in Fig. 5) also give interesting inputs about the kinetic of recoverable or permanent degradation effects (#A and #B), and related information can be found in [11].

These data are used together with other characterization and simulation tools presented in the next sections to complete the map for understanding the underlying fine mechanisms of the stress. Here, accumulation of positive charges under the gate change the intrinsic bias of the 2DEG, and modulate the carriers

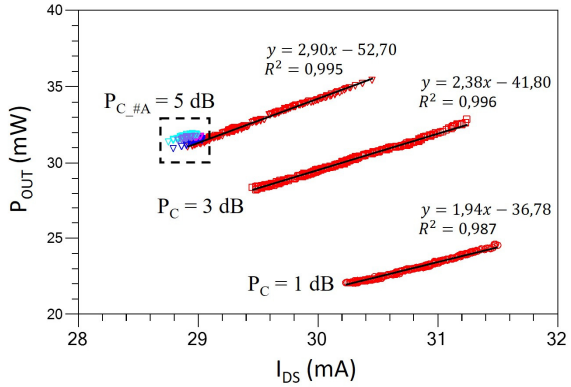


Fig. 5. Correlation between P_{OUT} and I_{DS} from Fig. 4 at 1 dB, 3 dB and 5 dB (#A) output power compression point. #B is not presented for improved clarity, due to the overlapping of the 5 dB #A and #B plots.

density n_i (thus I_{DS}). The dynamic gain S_{21} evolves (dBS_{21}) and the P_{1dB} compression point decreases as also revealed on the same sample of devices during X-band stresses [7]. From [S] parameters measurements (illustrated in Fig. 7 at 5dB compression), the input impedances (or S_{11} reflection coefficient) of the tested devices remain stable over time at each compression level; it can be stated that the electrical elements between gate and source pads are kept unchanged (access resistances on gate R_G and source R_S, intrinsic resistance R_i, and gate-source capacitance $C_{GS\text{-}i}$). Thus, time evolution on S_{21} correlates with change of the dynamic transconductance gain g_m, or to change of the intrinsic potential applied to the capacitance $C_{GS\text{-}i}$ (vertical stacking of charges at layers interfaces below the gate Schottky diode [10]). By using a fault tree method together with pertinent dedicated measurements or models, it is possible to guarantee the validity and the reliability of the interpretations.

To the three questions usually addressed by industrial founders for a process qualification (what happens? when does it happen? where does it take place?), two more questions must be discussed additionally (why and how do the defects reveal?). These last questions usually need specific experimental workbenches available in academic laboratories. The next section shows some experimental setups used for failure analysis studies, with objective to answer to the previous set of questions.

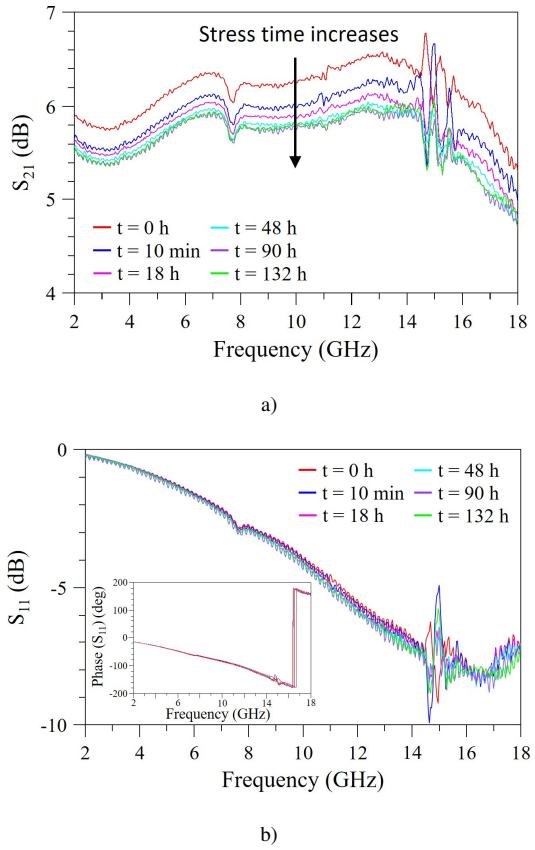


Fig. 7. [S] parameters evolution during 132 hours of stress at 5dB output power compression point. a) changes are noticed of the magnitude of the transmission gain S_{21}, whereas b) the magnitude and the phase of the input reflexion coefficient S_{11} remains stable.

III. Different Crossed Experimental Techniques

GaN HEMTs are obviously robust wide bandgap devices, but they are also sensitive to electrical charges, depending on local or global thermal states, on electrical fields and mechanical strains due to spontaneous and piezoelectrical charges at different interfaces of the layers. Related defects and resultant failure analysis can be revealed with experimental tools, directly by targeting the active area (destructive tools) or by deduction from external measurements (non-destructive tools).

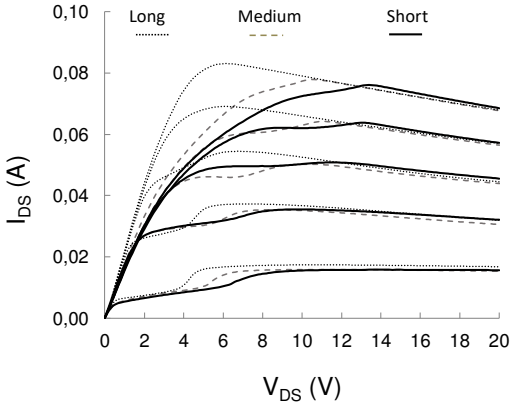


Fig. 8. Illustration of invasive DC-measurement on output characteristics of a 0.25x2x50 µm² HEMT (Measurement performed on a not yet mature InAlN/GaN HEMT process). I-V characteristics are given for different acquisition time configurations (acquisition time per data point - Short=640µs / Medium=20ms / Long=320ms) using 4156C Keysight Signal Analyser.

A. *Non-destructive techniques before/during/after stress*

Experimental tools allowing electrical (transient or harmonic) characterizations are attractive because the device under test is not supposed to evolve during the characterization. Then consequent sets of data can be compared at different stress times for fine analysis or modelling (versus electrical models or for TCAD model instruction). However, the measurement is mainly extrinsic to the invoked zone where the failure mechanism takes place, and a rigorous procedure associated to the experimental setup is needed to lower the speculative aspects of the resulting outcomes. First, it has to be considered seriously that non-destructive measurement technique does not necessarily mean non-invasive measurement. Test conditions can interact with some defects according to the setup of the workbench. Fig. 8 illustrates the sensitivity of a new generation InAlN/GaN HEMT device relatively to the acquisition time instructed for a signal analyzer during so-called 'static' or 'DC' output I_{DS}-V_{DS} (and transfer I_{DS}-V_{GS}) characteristics.

When such variation occurs in output 'static' characteristics, then electrical models using short or medium measurement configurations are erroneous due to those side effects, considered as the manifestation of memory effects. Even during [S] parameters measurement, frequency dispersion can appear at frequencies well below the starting frequency conditions (usually set at 40 MHz) [12]. In the case of DC or [S] parameters variation according to measurement conditions, resultant models will be inappropriate for analysis before, during or after the application of a stress (and of course inappropriate for circuit design).

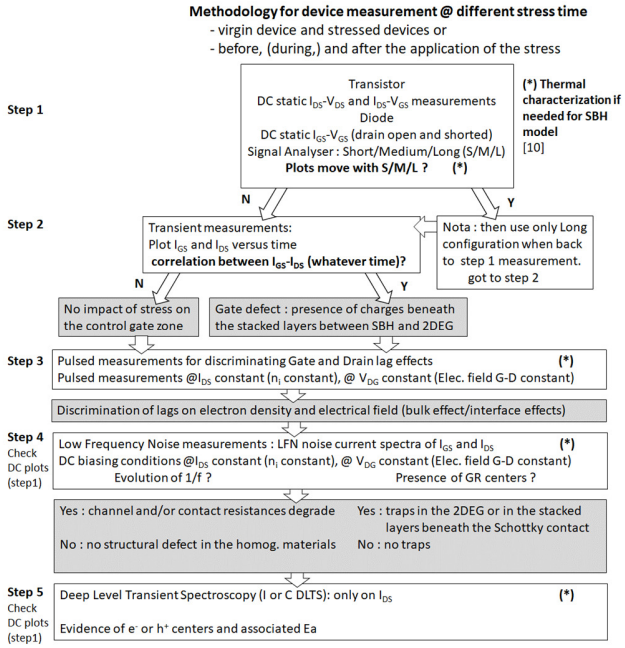


Fig. 9. Measurement methodology using transient and harmonic measurements to reveal defects in the HEMT. Comparison between initial/final measurements defines the location and the origin of the defects.

The methodology used for each characterization before and after the application of the stress is depicted in Fig. 9; the experimental setup complementarity is associated to the different sweep conditions (time, frequency or temperature). In this procedure, data from the stress file (i.e. P_{out}, DC currents and [S] parameters versus time) are analyzed together with initial and final set of measurements as proposed in Fig. 9. It is also possible to partition the stress campaign to have more intermediate results.

- DC measurements stand as reference measurement to ensure the integrity of the electrical signatures of the DUTs during the procedure of Fig. 9. If these characteristics change, then fine analysis between step 1 and step 5 is nonsense (step 1, step 4, step 5).
- Transient measurements give a first insight about short, medium or long memory effects or trap related effects. Moreover, the possible correlation between I_{GS}(time) and I_{DS}(time) gives a first order information about the common nature of the defect charges under the gate [10], as depicted in Fig. 10 (step 2). This is the evidence of time-varying charges under the gate, which effect is to de-biais the intrinsic V_{GS}-i control voltage, and then affects I_{DS} and I_{GS} simultaneously (with a first order linear dependence for I_{DS} and an exponential law for I_{GS}, as stated by the neperian logarithmic relationship from Fig. 10 b). A procedure is proposed in [13] for lag analysis on gate and drain currents using pulsed measurements (step 3).
- Low Frequency Noise spectra (LFN) spectra (from 1 Hz to 1 MHz) are known to be very sensitive to the quality of the material and to the presence on defects on the path where the current flows (gate S_{IG} and drain S_{ID} noise current spectral densities). Measurements under different biasing conditions permit the identification of DC voltage or current sensitivity

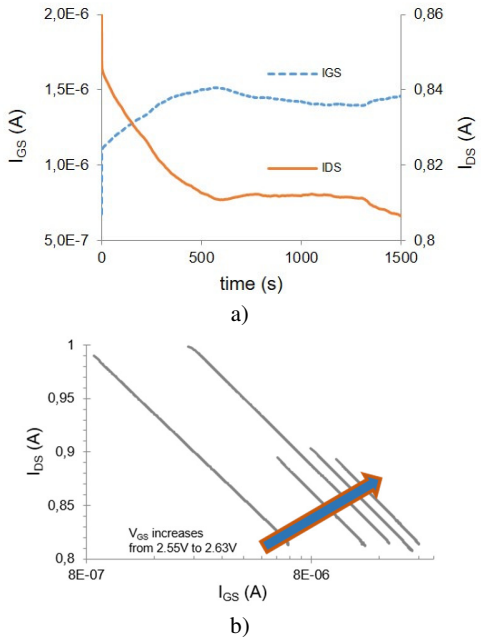


Fig. 10. DC leakage current I_{GS} and drain current I_{DS} variation for a 1 mm equivalent width GaN device. a) Evolution versus time over 1500 seconds for a given quiescent point V_{GS}-V_{DS}, and b) neperian logarithmic correlation according to I_{DS}=ln(I_{GS}) for different quiescent points on the overall transient screen.

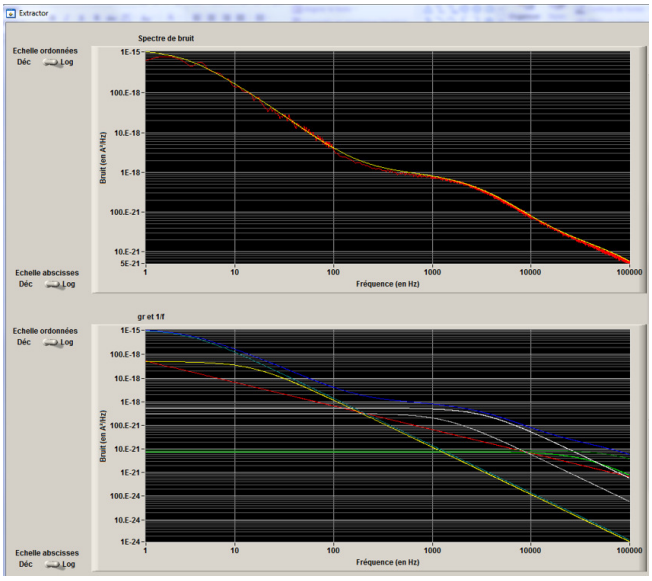


Fig. 11. Low Frequency Noise measurement (red) and resulting model (yellow) on gate current spectral density versus frequency (top picture), with automatic extraction of noise contributors (second screen below); here six different lorentzians (four generation-recombination and two RTN contributors) and 1/f flicker noise are evidenced to compose the blue plot model (yellow in the upper screen). Screenshot from proprietary software; for distinction of colors, please refer to the electronic version.

of traps (Generation-Recombination centers if present in the measured spectra) (step 4). From the literature, it is often illustrated that S_{ID} remains constant before and after the application of a stress, despite numerous GR distributed over the low frequency range; this means that defects are present (and can vary with bias), but are not necessarily impacted by stress. On the contrary, S_{IG} is very sensitive to charge or trap evolutions and can stand as a great marker of defects under the Schottky command [13][14].

- Capacitance or current Deep Level Transient Spectroscopy (C- or I-DLTS) measurements are performed over a temperature range of 90 K -450 K (step 5). Activation energy and section of the traps are extracted and compared with the GR centers from LFN measurements in step 4 [15].

Fig. 11 plots the measured Low Frequency Noise current spectral density S_{IG} on the gate, with the extracted contributors; 1/f flicker noise, Lorentzian noise from Generation-Recombination centers (GR) or Random Telegraph Noise (RTN). RTN contributors are sort out by performing transient measurement, and by using a routine for corner frequency and current variations (Fig. 12); the contribution of RTN can be plotted in the frequency domain by using equation (1), and compared to LFN spectra as illustrated in Fig. 11. A dedicated software developed in the laboratory allows the extraction of noise contributors from LFN spectra. Then, the GR centers are tracked and plotted versus biasing or versus temperature. This allows to extract activation energies [15], and to identify the related bond-vacancy or other activation mechanism from literature, or by crossing experiments with Energy-Dispersive X-ray (EDX) spectroscopy or Raman spectroscopy analysis for example. The same procedure has been develop for the noise spectra on the drain current, under different constant voltage V_{DG}, V_{DS}, V_{GS} biasing conditions to appreciate the first order

parametric law versus the electrical field, or versus the carrier density [13].

$$S(f) = \frac{2(\Delta I)^2\bar{\tau}}{4+(2\pi f\bar{\tau})^2} \text{ with } \frac{1}{\bar{\tau}} = \frac{1}{\overline{\tau_e}} + \frac{1}{\overline{\tau_c}} \quad (1)$$

τ_e and τ_c are respectively related to the lower and higher states of the noise level. Many levels are accounted for, as illustrated in Fig. 12, in the statistic extraction of random telegraph signals.

Other characterization tools have been used successfully (not identified in Fig. 9), to give evidence and to characterize defects in the devices under test. For instance, photo Emission Microscopy (EMMI), Optical Beam Induced Resistance Change (OBIRCH) technique [16], electroluminescence, or other athermal A-DCTS techniques [17] and Capacitance-Voltage (C-V) measurements are providing the users with key complementary clues.

B. Destructive techniques (before/) after stress

Non-destructive techniques can also be considered as speculative, because of the indirect proof given of a failure mechanism (especially when different defect mechanisms are engaged). Destructive technique focus on the active part of the defect (according to the difficulty to find out the related location). If the manifestation of defects can be proved by direct location of structural/chemical degradation in a stressed device (compared to a virgin device), a question still rises from such an approach: does this defect play a role in the electrical signature of the device? Statistic approach also strengthens the conclusions from these studies, but definitely it will not be easy to check intermediate steps during stress periods; this would imply a large number of (homogeneous) samples for each stress, removing few devices at given moment of the stress. Then the correlation of studies as proposed in Fig. 1 reduces the risk of speculative answers by crossing independent issues.

Very sensitive characterization tools such as High-Angle Annular Dark-Field Scanning Transmission Electron Microscopy (HAADF STEM) with atomic number contrast in the stacked layers, Transmission Electron Microscopy (TEM) lamella after gate foot removing, EDX spectroscopy analysis have been used in [18] with TCAD models and electrical measurements to differentiate defects origins responsible of various failure signatures.

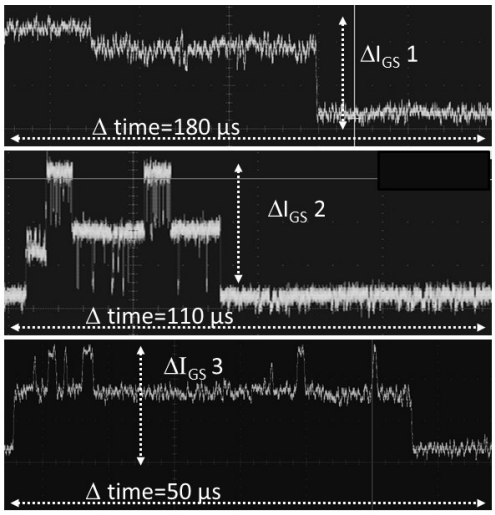
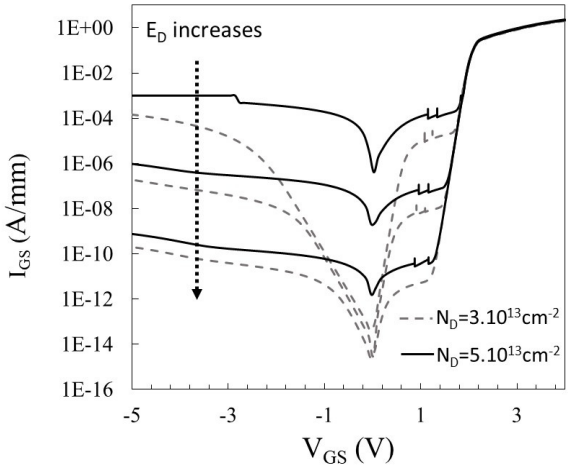
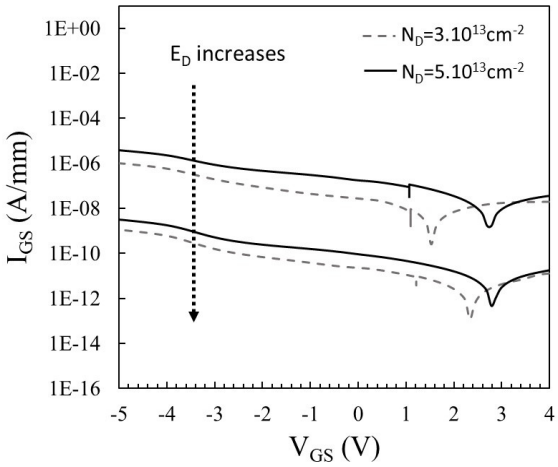


Fig. 12. Random Telegraph Noise transient measurements can be modeled and their contribution can be distinguished from GR Lorentzian in Fig. 11.



a)



b)

Fig. 13. Simulated leakage I_{GS}-V_{GS} characteristic (V_{DS}=0 V for figure a, and V_{DS}=8 V for figure b), versus different donor activation energies and concentrations. Energies E_D are situated at (0.1eV figure a), 0.3 eV and 0.5 eV below the conduction band, with donor concentration n_D at 3.10^{13} cm^{-2} and 5.10^{13} cm^{-2}.

IV. MODELS FOR FAILURE ANALYSIS

From electrical (large signal) measurements, it is possible to develop non-linear models; the availability of such a model with failure signatures associated is useful for circuit design [18]. Design of a circuit at initial t_0 and also considering parametric shifts at final t_{stress} can help the designer for topology optimization.

Here, TCAD models (using Sentaurus-Synopsys) are more under concern as the paper deals with failure analysis. Physical modeling of degradation mechanisms thanks to 2D simulations

of the active device helps to understand III-N HEMT failure modes; the instruction of physical parameters in a specific region of the model gives helpful feedback on experimental results.

Effects of charges and traps in terms of nature, location, energy level, density, section, (bulk, interface, under the gated or ungated zones G-S and G-D) can be evaluated on the output I_{DS}-V_{DS} and transfer characteristics I_{DS}-V_{GS} (G_m-V_{GS}) [19], and on leakage currents I_{GS}-V_{GS} (diode and transistor mode).

After an exhaustive study concerning the way to instruct the defects and to simulate the parameters, the impact of donors or acceptors in the bulk and at the different interfaces, one can dispose of a large variety of parameters, each associated to a failure signature. Then, regarding the experimental plots, it is possible to tune such TCAD model to match the measurement in a realistic way.

Donor-like centers in the bulk account for I_{GS}-V_{GS} magnitude variation as revealed by some HTRB or HTOL stresses. It is likely to suppose that, for a fixed activation energy of the donor-like centers, only the concentration increases with the application of the stress, as reported in Fig. 13 a) (donor located at the SiN/GaN cap layer interface); the rapid increase of the leakage current from part of this inversion voltage, featuring a plateau, is reported in many papers [20][21], and even concerns GaN-based LEDs [22]. Furthermore, Fig. 13 b) illustrates how the inversion voltage shifts largely considering different donor concentrations, and for activation energies situated 0.3 eV below the conduction band E_C, in transistor mode (no variation of V_{th} versus n_D is revealed for 'deep centers' as reported for E_D=0.5 eV below E_C). The closer the activation energy to the conduction band, the more pronounced the variation shift of the inversion voltage. Depending on the epitaxial and passivation process, the simulation can fit to account for specific electrical signatures.

Other electrical modelling of HEMT devices can be used to account for fine charge effects, or defects influence in the active zones or in the command definition. The accuracy of such a model, and its aptitude to translate the physical behaviour when embedded in a circuit context, is mandatory to enable power devices working close to their maximum safe operating conditions. The other point is to provide confidence to the circuit designer concerning the mean time to failure, and so to integrate models of the device at t_0 (initial performances) and t_{max} when dynamic or static criteria are 10% degraded for example. As the command, or at least the vertical stack under the command, seems to play a crucial role in the degradation processes of I_{DS} (and P_{OUT}), the specific model of the Schottky Barrier Height (SBH) must be accurately instructed in the electrical models. From the literature, the extraction of the SBH value is usually over-evaluated with ϕ_B ranging between 1.1eV and 1.6eV, while the theory states a value for ϕ_B around 0.9eV. We have developed a method for the accurate mean SBH extraction, using leakage currents from low to high levels, and for a large range of temperature [19][23]. Then, after processing the mean SBH for different inhomogeneity of the barrier, it is possible to extract the ideal SBH on the σ_s=0 eV intercept (i.e. with no inhomogeneity or defect). From Fig. 14, 2 virgin and 4 stressed devices are processed, all featuring an ideal SBH around 1eV at zero dispersion σ. The impact of the stress is noticeable, with virgin devices featuring lower SBH and with stressed devices featuring higher SBH. Thus, the need of stability for the gated control zone, and its correlation with the degradation of the devices, is clearly highlighted.

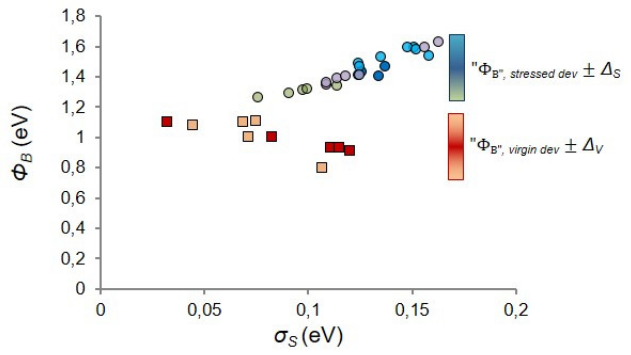


Fig. 14. Variations of $\overline{\Phi_{Bx}}$ versus σ_{Sx} at temperature between 200K-400K), under different gate current ranges (2 decades sliding gate current window), for 2 virgin samples (squares) and 4 stressed samples (circles).

V. Global Overview Concerning Failure Analysis Results From Previous Studies on GaN HEMTs

From the proposed set of experimental and simulation tools, we are able to reduce the number of speculative assumptions concerning the possibly involved mechanisms from a given file of stress. The detection and the location of charges at different interfaces under the gate and between gate-source and gate-drain regions, the possible transient correlation between gate and drain currents related to time-varying charges under the gate, and the analysis of the gate leakage current behaviors versus temperature are some of the outcomes from such previous works. As one of the dominant failure mode of GaN HEMT devices relates to a gradual RF output power degradation (wear-out), generally correlated with the (recoverable) decrease in the drain current (current collapse), studies have been focused on the impact of RF power stresses. The role of RF-activated traps and charges has been evidenced on the degradation mechanism for different compression levels. Moreover, the leakage current is an efficient marker of the degradation mechanisms [24], and a direct link can be established between the current level I_{GS} and the MTTF as shown by [25]. Then its study is considered as the most relevant part for nitride technology improvement. From some studies summed up in this paper, we are able to discriminate between defects in the channel (usually not stress-dependent) and defects activated by stress in the outer zones of the main electron flow (from source to drain), featuring recoverable or permanent effects. These techniques have made it possible to improve different academic and industrial GaN processes.

VI. CONCLUSION

The optimization of a GaN technological process concerns the understanding and the mastering of failure mechanisms, still considering a roadmap towards increased frequency and power added efficiency. Failure analysis for RF stresses are among the more difficult to achieve as many parameters are involved in the different RF and DC electrical signatures before and after application of a stress. A set of DC/thermal/RF stresses is usually needed for the identification of such degradation processes, which represent long study times. In this paper are identified a set of (non) destructive measurement techniques that can be confronted with TCAD simulations to secure the failure analysis as presented in Fig. 1. It is then possible to identify root physical degradation defects involved in many different (RF or DC) electrical signatures from a single RF life test. Obviously, this methodology does not allow the extraction of activation energies needed to get the mean time to failure; it can however be easily reached if used with three different temperature life tests.

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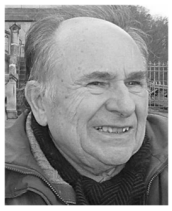

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