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► **To cite this version:**

E Baghaz, A Naamane, N. M'Sirdi. The use of Carbide Silicon transistors in a switch-mode power supply. IRSEC IEEE 6th Int Renewable and Sustainable Energy Conference, Dec 2018, Rabat, Morocco. hal-02078037

HAL Id: hal-02078037

<https://hal.science/hal-02078037>

Submitted on 25 Mar 2019

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The use of Carbide Silicon transistors in a switch-mode power supply

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Abstract—In this paper, we propose a switch mode power supply using carbide silicon transistors in a Full Bridge DC/DC converter structure controlled by an analog control, designed during this work. This solution shows several advantages: simple implementation, compactness with satisfactory performance. The simulation results achieved are compared with those obtained by using a Texas Instrument digital controller UCC28950. It is shown that the designed power supply with an analog control shows an efficiency of more than 90%.

Keywords: Full Bridge DC/DC converter, analog control, UCC28950 controller, power supply, output

I. INTRODUCTION

The choice of DC/DC converters in the field of power electronics, depends on the load specification of the desired application. Classical DC/DC converters (Boost, Buck, ...) are easy to design, they require only one PWM signal to control the power switch. But this type of converters are only used for limited current and voltage applications, they suffer from a low-yield problem [1-4] because of the use of hard switching controls, resulting in very significant output power loss during the switching of the transistor [1-4]. To address this problem, there are several other structures of power DC/DC converters for power applications [5,12]. In this context, we propose a high power full bridge DC/DC converter [11] using A carbide silicon MOSFET's. this structure is controlled by an analog circuit, which has several advantages: Simple to implement, compact and it allows a soft switching. And as a result, it improves the overall efficiency of the converter. The simulation results obtained are compared with those of converter designed and controlled by Texas Instrument components. [11] This comparison shows that the system developed in this work has similar results to that of Texas Instrument ones.

II. STRUCTURE AND OPERATION OF A FULL BRIDGE DC/DC CONVERTER CONTROLLED BY AN ANALOG CONTROL

Figure 1A represents the synoptic diagram of the Full Bridge DC/DC converter, with its analog control high controlled power an analog. Figure 1B, represents a full bridge DC/DC converter. With four transistors (T_A , T_B , T_C , and T_D) in the primary side of the transformer. T_E , and T_F represent the

transistors on the secondary side of the T_2 transformer. While L_{Out} and V_{Out} form the output filter. The T_r inductance is designed to assist the T_2 transformer leakage inductance when operating in resonance with the internal capacity of the MOSFET and facilitates zero voltage switching (ZVT). We have used silicon carbide-based transistors (C2M0025120D).

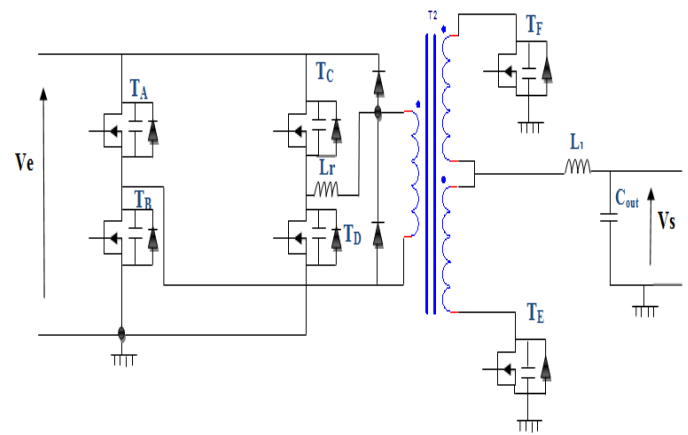


Figure1. DC/DC Full Bridge converter scheme

To monitor their operation, we conducted an electro-thermal study of this kind of transistor (Figure 2a) in order to evaluate the evolution of the junction temperature during its operation. Figure 2b shows the simulation results and with datasheet ones [12], the variation of the Drain-Source resistance ($R_{ds(on)}$) as a function of temperature, for a current value of 50A.. It appears that the electro-thermal model developed during this work shows a good precision close to the optimum operating conditions given by the datasheets even in the case of very high temperatures ($>150^\circ\text{C}$), which confirms the high temperature operations of SIC transistors.

The design of an analog control with soft switching

In order to design a simple analog control suitable for high power applications, we have studied and designed a simple analog control, it is based on the acquisition of the current image generated by the input generator and the output voltage we have also generated 6 PWM synchronized signals to ensure the switching of the 4 Transistors (T_A , T_B , T_C , T_D) on the primary side of the transformer and those on the secondary side (T_E , T_F) (Figure 1).

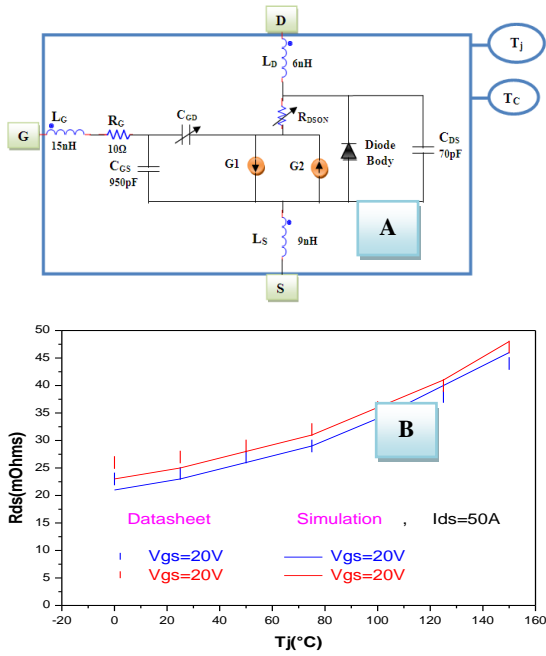


Figure 2: A: Electrical model of SiC (C2M0080120D).
B: Rds(on) variation Vs junction temperature

The operating principle of this control is as follows:

- ❖ **A proportional and integral PI** : which regulates the output voltage in order to correspond to a given reference. As shown in Figure 3, using a particular bridge circuit The two voltages V1 and Vref are connected respectively to the non-inverting and inverting input of the proportional and integral amplifier PI.
- ❖ **A progressive start circuit** (Figure 3):.This circuit allows to generate a voltage that increases slowly until it reaches the maximum value. The purpose of adding this circuit to the PI controller is to generate a progressive cyclic ratio in transient mode.
- ❖ The Acquisition of the current was carried out on the basis of the circuit shown in Figure 4A, the transformer used for this application has a transformation ratio (m) of 100 and the maximum voltage applied to the CS pin is $V_p = 2V$.
- ❖ From this data, we calculate the values of the resistances (R_1 and R_{cs}) in Figure 3A:

$$I_{p1} = \left(\frac{P_s}{V_s * \eta} + \frac{\Delta I_{L1}}{2} \right) * \frac{1}{m} + \frac{V_{INMIN} * D_{MAX}}{L_{MAG} * 2 * F_{SW}} = 6.88A$$

$$R_{CS} = \frac{(V_p - 0.3)}{\left(\frac{I_{p1}}{n} * 1.1 \right)} = 20.89\Omega \quad (1) \quad R_7 = n * R_{CS} = 800\Omega \quad (2)$$

- ❖ The signal that represents the current image at the input of the Full Bridge DC/DC converter is added to a saw-tooth signal (VRAMP) (Figure 4B), using a summer Opamp circuit. Next, the resulting signal is compared with the VS1 signal generated by the circuit in Figure 3. And as a result, this comparison results in a PWM signal. The simulation results are shown in Figure 4.

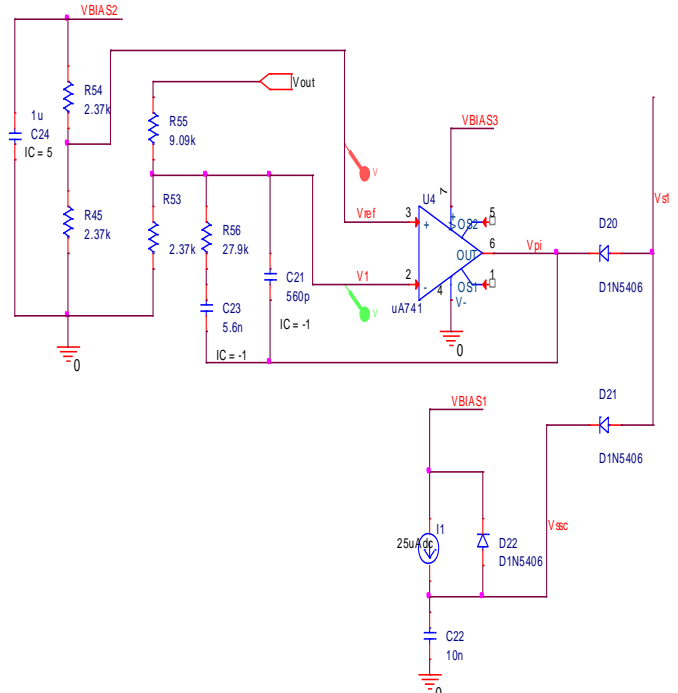


Figure.3. PI Corrector

The PWM signal obtained above is connected with a flip flop JK toggle (Figure 6). The Q output of this toggle will only change the state if the PWM signal connected to its CLK input is in the rising front. The signal Q and \bar{q} at the output of the JK are two PWM signals (QC and QD) that will control an arm of the transistors of the DC/DC converter Full Bridge.

Then, we applied a delay of 360ns to the front amount of two signals Q and (\bar{q}), which ensures a switching to zero voltage SVA (soft switching), avoiding the switching losses that usually occur during a Operation and a classical PWM delay.

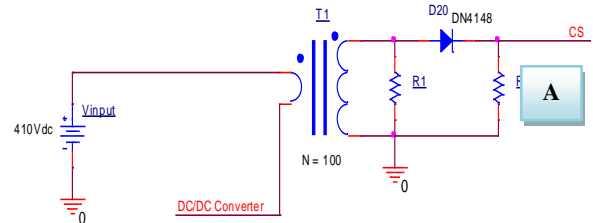


Figure.4 A : Input current acquisition

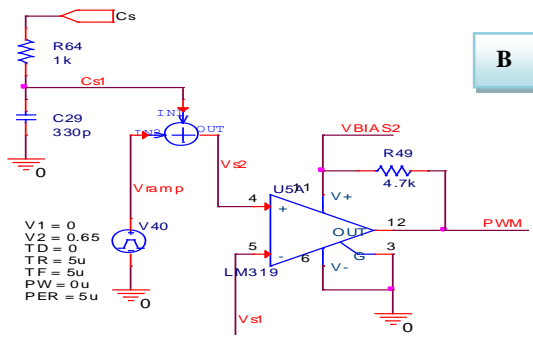


Figure.4 B: Input Current comparison with comparison Vs

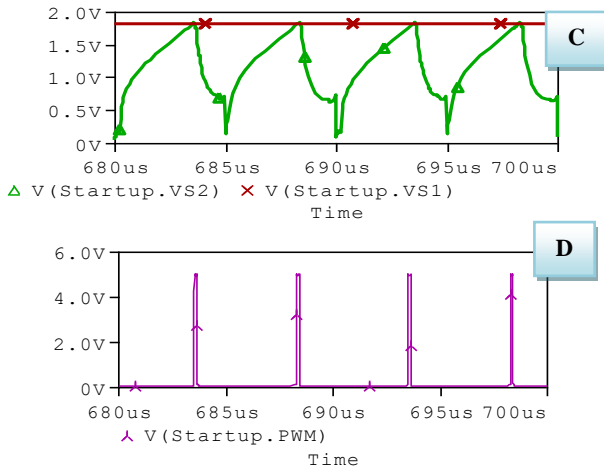


Figure.5 Generated signals by Circuits of figures 2 & 3

C: Signals comparison Vs of figure 2 and Vs1 of figure 3;
D: PWM signal at comparator output of figure 3B.

The simulation results are shown in Figure 7, by connecting the PWM signal obtained to a JK flip flop, we obtain the signal from Figure 6 in green. One notices the JK has a rising edge behavior for its state changes. The outputs Q and Q-, at the output of the JK flip flop, are shifted at each front up to 60ns. (7 F and G).

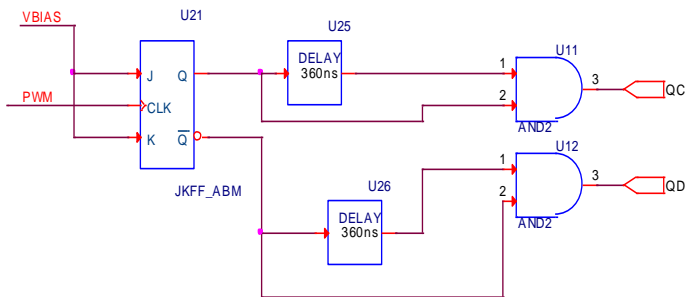


Figure.6 PWM signals connected to transistors T_C et T_D.

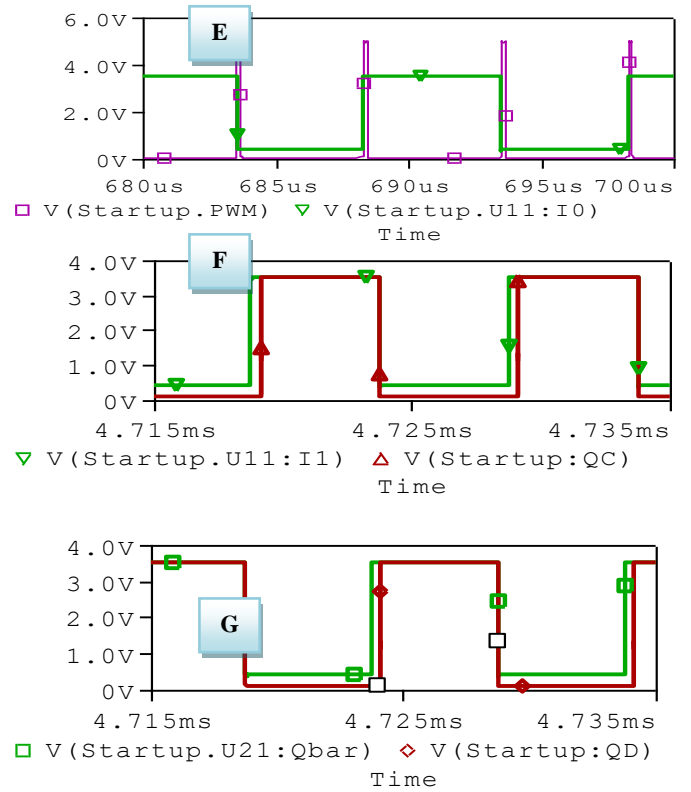


Figure 7. Signals generated by the circuit in Figure 5: E: PWM signal connected to the flip flop JK input (pink) and the one at its output (green); F: PWM signal QC (in red) of the JK flip flop (in green); G: QD PWM signal (in red).the output (Qbar) of the JK flip flop (in green).

Following the same principle, we generated the other two second-arm PWM signals from the Full Bridge DC/DC converter (Figure 8). Such as, by connecting a CLK signal of cyclic ratio of 0.05 to the CLK input of the Flip Flop JK, resulting in two output Q and (Qbar). By imposing in the same way a delay of 360ns on the front amount of each output, we deduct the other two PWM signals (QA and QB) of the primary part. Figure 9 shows the simulation results of the signals generated by the circuit in Figure 8.

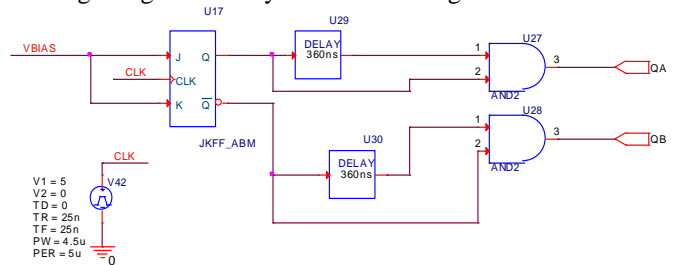


Figure.8 PWM signals connected to transistors T_A et T_B

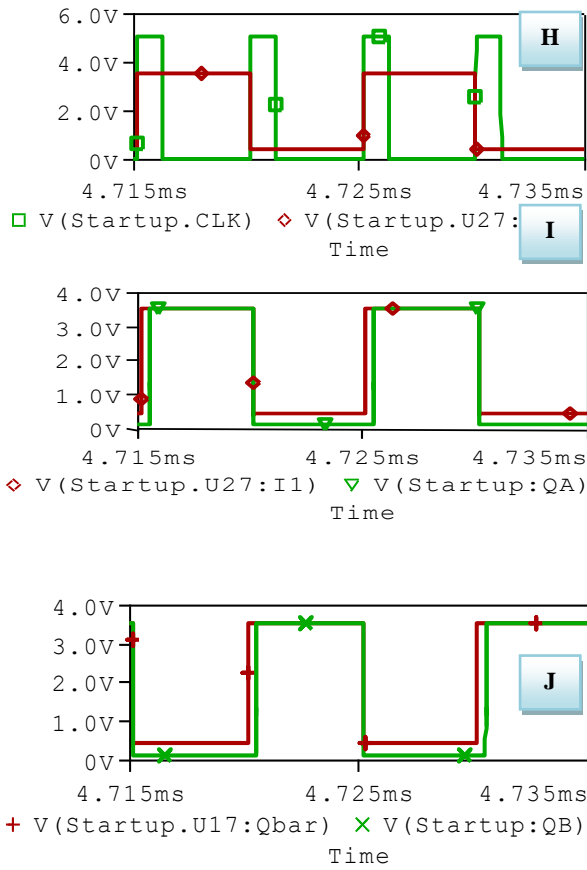


Figure.9 H: Clock signal (in green) connected to the flip flop JK input and the one to its output (red);
I: QA (green) PWM signal at the output of the JK flip flop (in red)

III. SIMULATION RESULTS AND INTERPRETATION

Fig 10, represents the complete circuit of the switching mode power supply, implanted in the PSPICE simulator. We represent in the following the different simulation results obtained.

III.2 Performance comparison of the designed control and the UCC28950 controller

In order to show the performance of the analog control designed during this work, we compared the different signals of the Full Bridge converter in Figure 1b, controlled by the designed control and the UCC28950 controller. The different results obtained are shown in Figure 11. It is to note that the results of the system controlled by the analog control designed are shown in Figure 11 on the left and those of system controlled by UCC28950 [11] are shown on the right. Based on the results obtained:

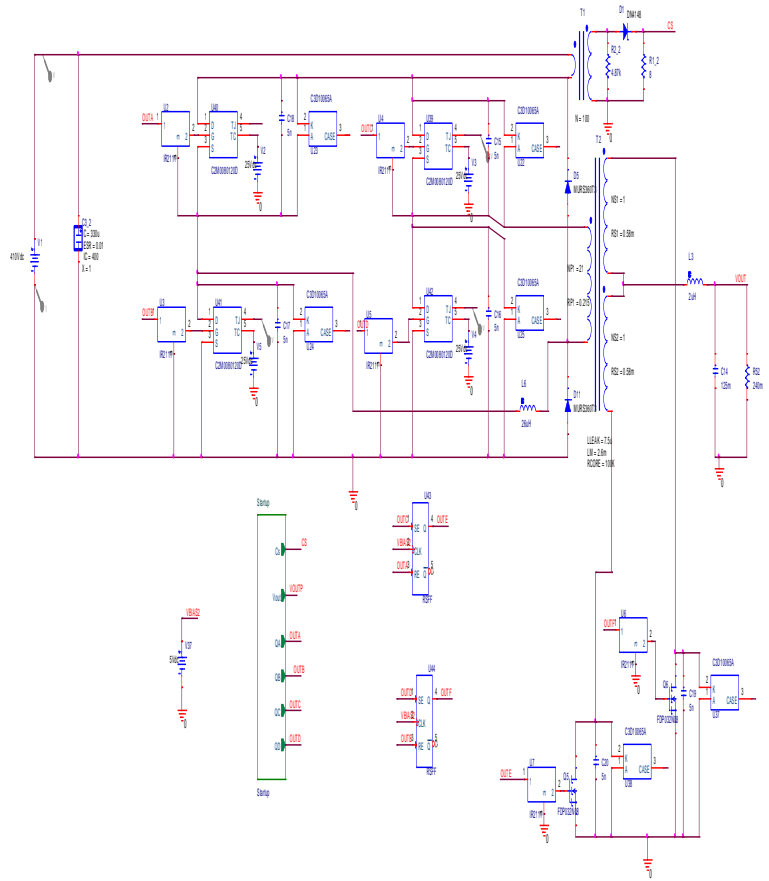


Figure. 10 Complete circuit of the Supply switch mode

- The comparison of the OUTA PWM signal generated by the two controls shows that they have the same cyclic ratio of 0.47, the same frequency of 100kHz.

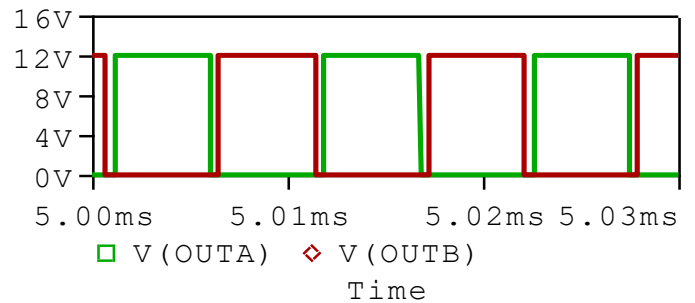
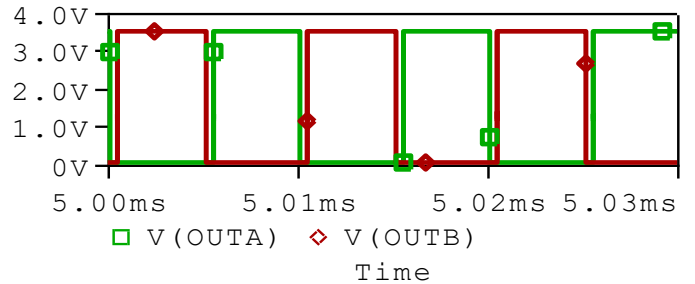


Figure 11. OUT A PWM signal,

- The currents (Figure 12A and B), which flow in the transistor TF of the second part, generated by the two commands are identical

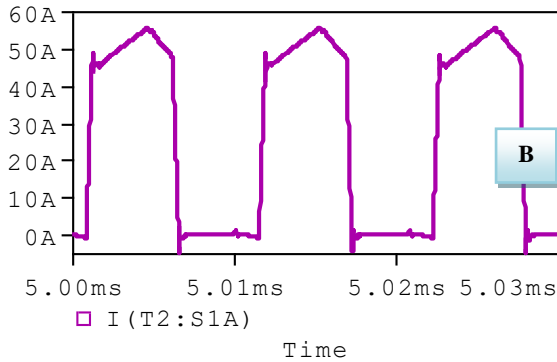
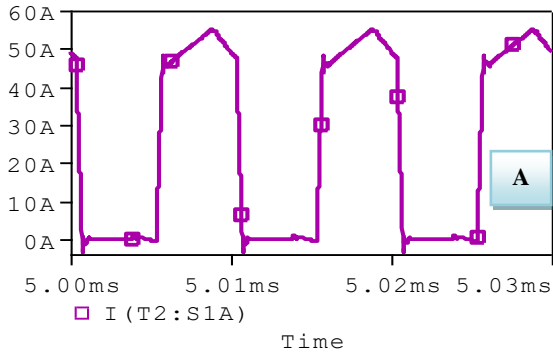
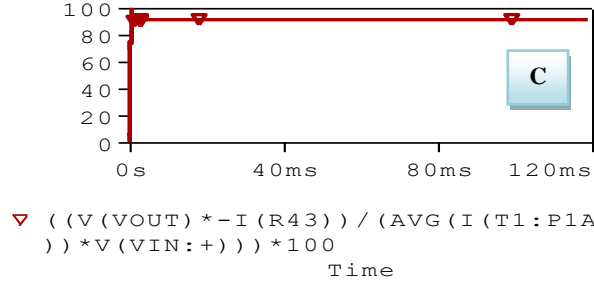
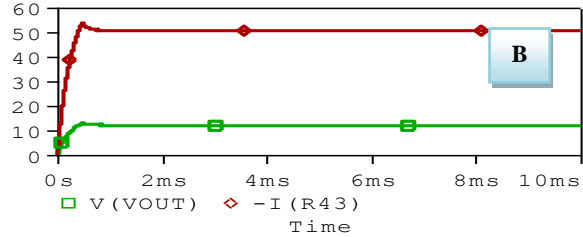
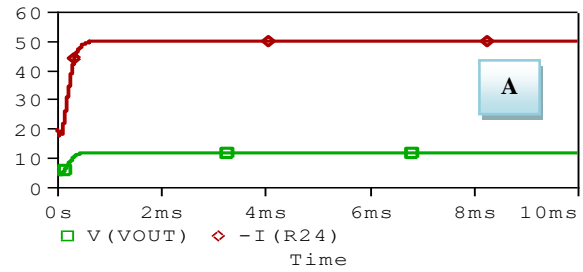
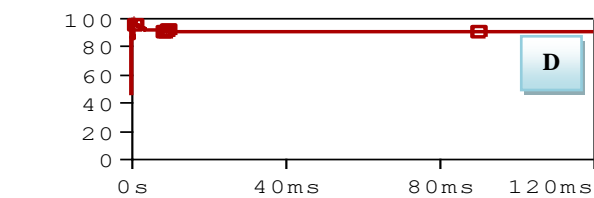


Figure .12 Output transformer current generated

- The electrical quantities at the output (voltage, current) generated by the analog control designed (Figure 13 A) are identical with those generated by the UCC28950 (Figure 13 B). Then, the electrical quantities generated by the controls respond well to the defined load specification: a voltage, a current and a power output of 12V, 50A and 600W respectively
- The analog control designed in this work has a satisfactory performance, it is higher than 90% (figure 13C). It is identical to that generated by the UCC28950 controller (figure 13D).
- The analog control designed during this work generates well-synchronised PWM signals, which ensures smooth switching to the transistors of the DC/DC converter. In order to clearly show these advantages, we have shown in Figure 12 and F, the power losses and the junction temperature of the four transistors, of the Full Bridge DC/DC converter (Figure 1), during the transistor switching. It appears that, the power losses in each transistor is low, they do not exceed 0.5W. Then the junction temperature of each transistor is about 50 °C. The results obtained clearly show the advantage of the control designed during this work



$$\triangleright \left(\frac{V(VOUT) * -I(R43)}{AVG(I(T1:P1A)) * V(VIN:+) } \right) * 100$$



$$\square \left(\frac{-I(R24) * V(VOUT)}{AVG(I(T1:P1A)) * V(T1:P1A)} \right) * 100$$

Figure. 13 Electrical quantities at the output of the DC/DC converter generated by the two controls:

A (B): Voltage and current generated by analog control (UCC28950)
C (D): Overall output of the converter controlled by the digital control (UCC28950).

III.2 Power losses study of the DC/DC converter

The analog control designed during this work generates well-synchronised PWM signals, which ensures soft switching of the transistors of the DC/DC converter. In order to clearly show these advantages, we have shown in Figure 14, the drain current I_D and the V_{DS} voltage of the DC/DC converter. It should be noted that the current is multiplied by 100 in order to clearly notice the power losses during the transistor switching. It appears that:

- At the opening of the T_A transistor (Figure 14 A), it is noted that the V_{DS} voltage toggles from 0 to 400V in few nanoseconds time and the current I_D changes from the max to 0 gradually, leading to a very small power loss. While

at the closing (Figure 14 B), the V_{DS} voltage diverges directly to 0. On the other hand, the current I_D is delayed (1.5 μs) so that it toggles from 0 to its maximum value giving also a very small power loss (Figure 14 C) Then the junction temperature of each transistor is about 50 $^{\circ}C$ (figure D). The results obtained show clearly the advantage of the control designed during this work

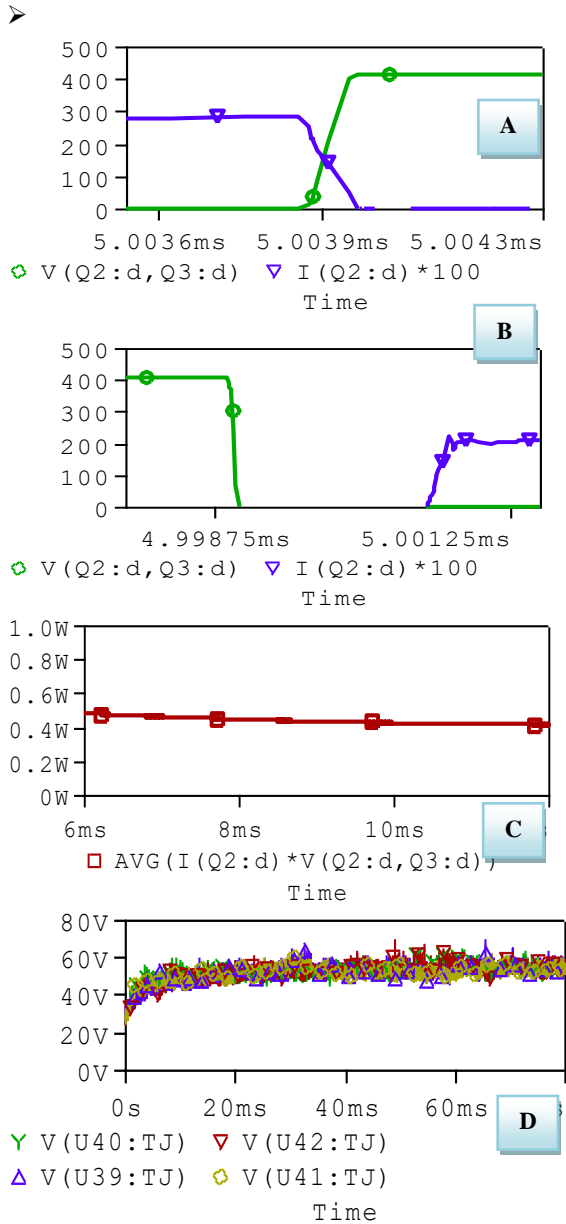


Figure 14 : Voltage V_{DS} and current I_D of the DC/DC converter T_A in Figure 1:
A and B: Voltage V_{DS} and current I_D at the opening and closing of the transistor.
C: Dissipated losses in the T_A transistor.
D: Temperature junction (1V=1 $^{\circ}C$)

IV. CONCLUSION

The development of a power supply with a relatively high current is presented. It allows to generate a voltage of 12v and a current of 50A, (600kW). It operates at a switching frequency of 100 kHz. The used structure is a Full Bridge DC/DC converter controlled by an analog control, developed and designed during this work. The challenge was to show that the analog control could advantageously be used instead of a digital one as the one commercialized by the Texas Instrument (UCC28950. The different results obtained show that the proposed control has relevant results similar to those obtained by the digital control.

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