

Packaging Solution for SiC Power Modules with a Fail-to-Short Capability

APEC, Anaheim, USA



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Outline

Introduction

Power Module Design & Manufacturing

Test of the Failure Mode

Conclusions



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Introduction

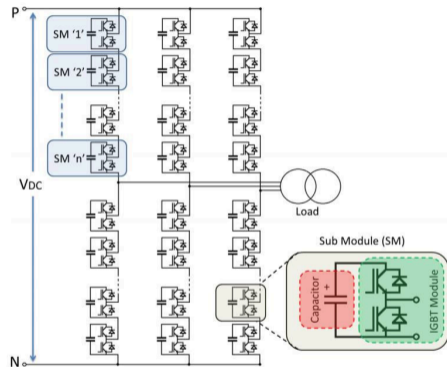
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Fail-to-Short Packaging for HVDC Applications

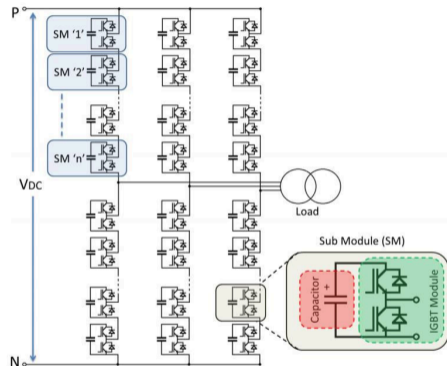


Source: I. Yaqub PhD thesis, 2015 [1]

HVDC Converters

- ▶ Rated at 100s kV
(ex 320 kV for France-Spain link)
 - ▶ Series of 100s of transistors
(800 for same converter)
 - ▶ Transistors fail randomly
 - ▶ Should not stop converter
 - ▶ Failed device turned to short circuit
- Need for Fail-To-Short Packaging

Fail-to-Short Packaging for HVDC Applications

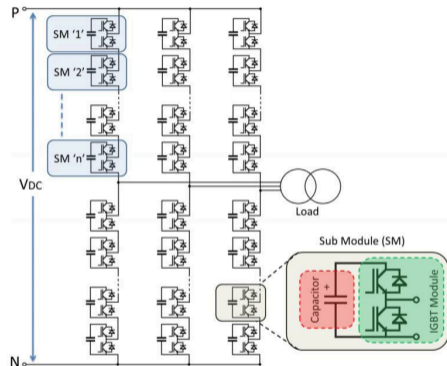


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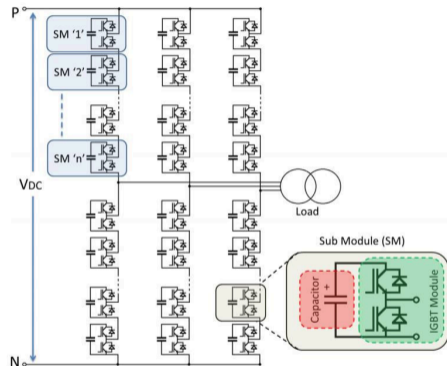
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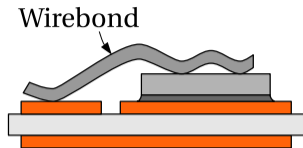
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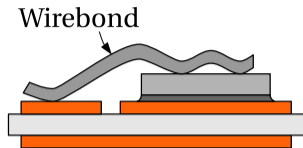
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- ▶ Standard packaging: Fail-to-Open
- ▶ Wirebonds act as fuses or blown away
- ➔ Need for massive contacts

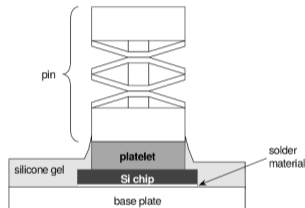
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- ▶ Initially for single die, now for multichip
- ▶ When failure occurs:
 - ▶ Temperature rises
 - ▶ Die and surrounding metal melt
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 - ▶ Strong package contains explosion

Fail-to-Short Packaging



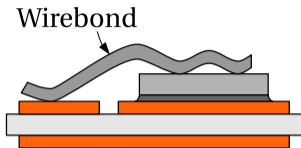
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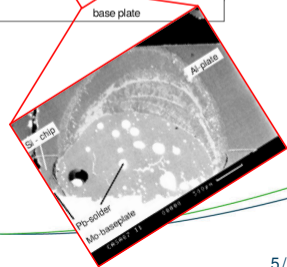
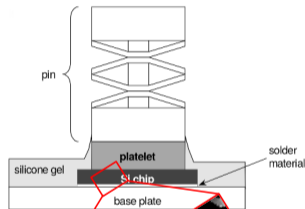
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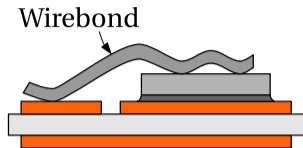
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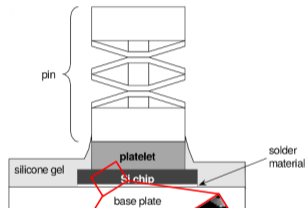
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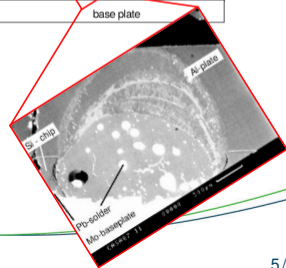
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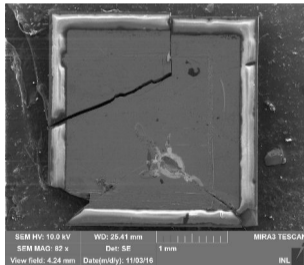


Is a FTS package Possible for SiC?

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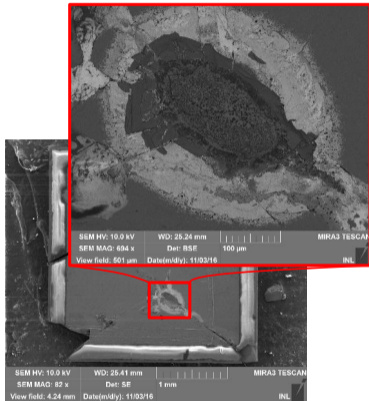


Previous investigations [3]



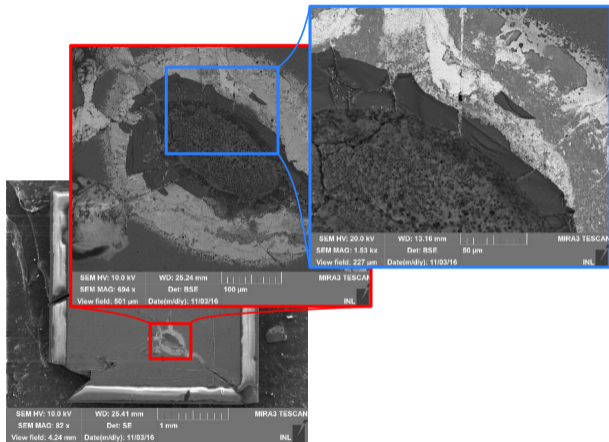
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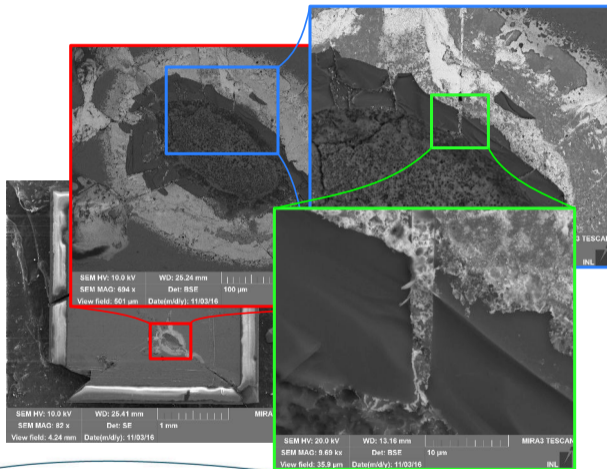
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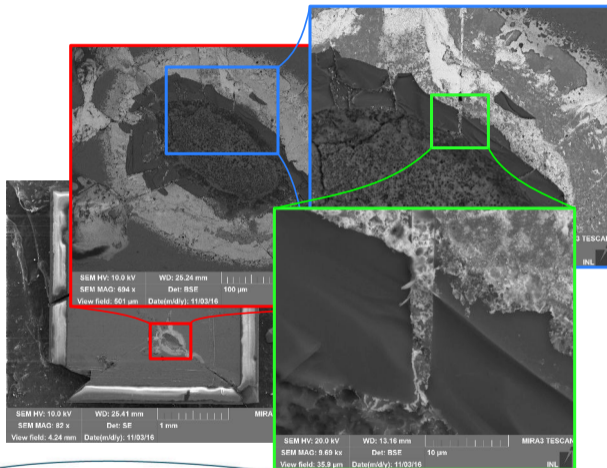
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→ Fail-to-short behaviour possible with SiC

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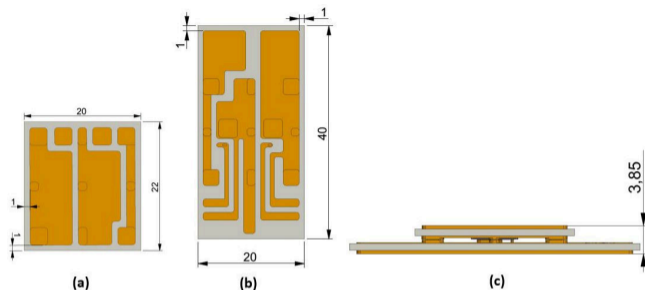
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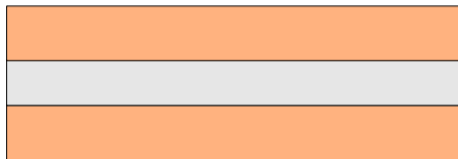


Module Structure



- ▶ **“Sandwich structure”**: massive interconnects
- ▶ **Silver sintering**: high temperature bonding
- ▶ **Salient features**: for topside contact with dies
- ▶ **Two SiC MOSFETs**: multi-chip module (half-bridge config.)

Preparation of the Substrates [4]



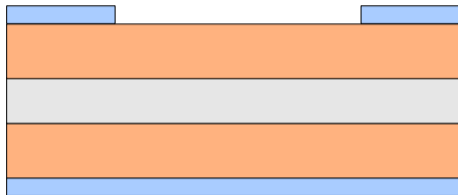
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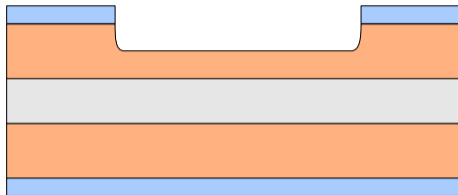
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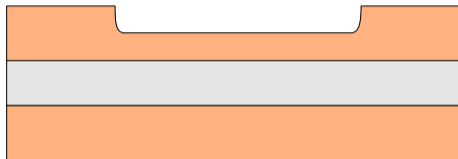
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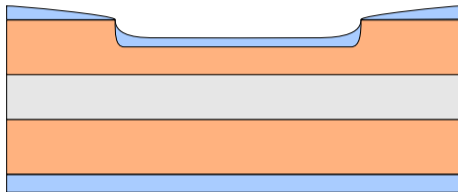
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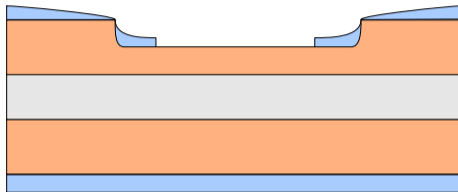


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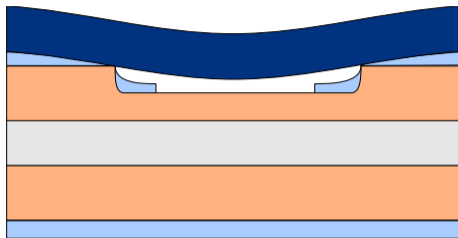
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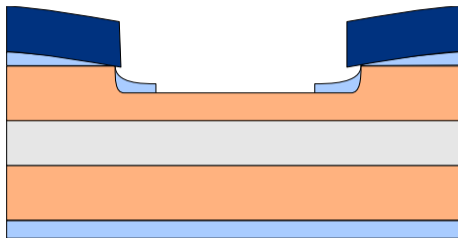
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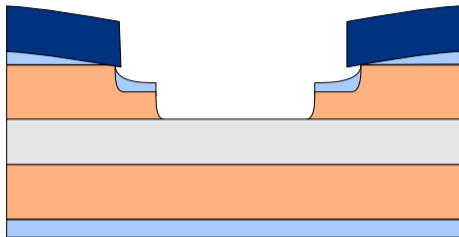
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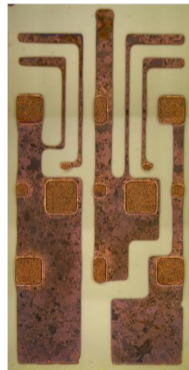


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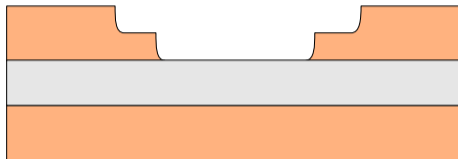
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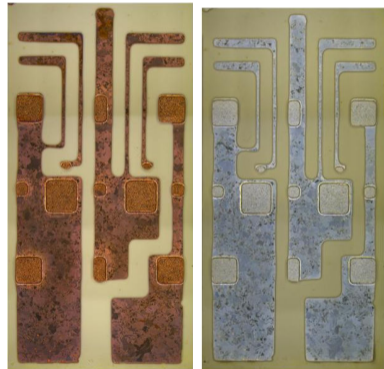
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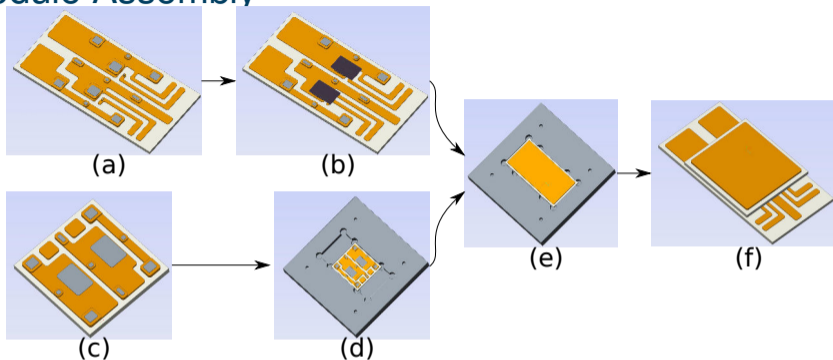
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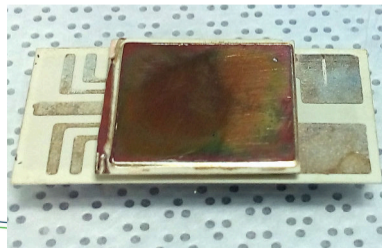
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Power Module Assembly

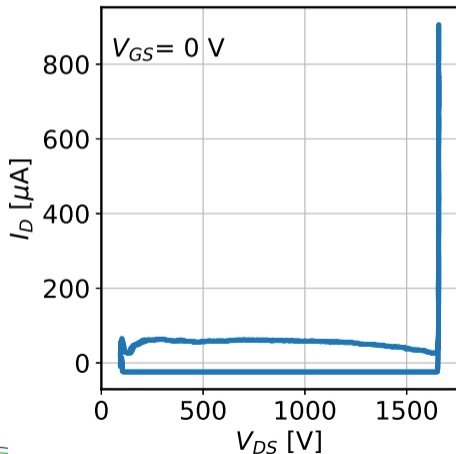
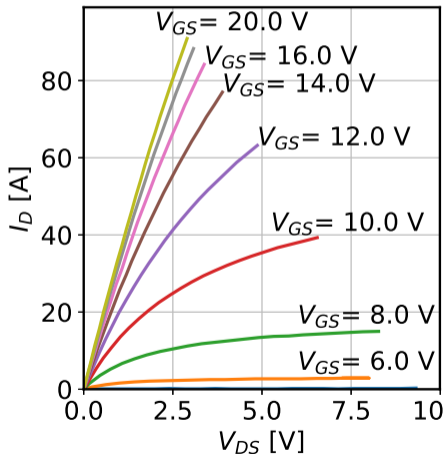


- ▶ Two sintering steps
- ▶ More details in paper and [4].



Electrical Validation

- ▶ 4 modules made (7 dies fonctionnal)
- ▶ 3 encapsulation schemes: none/Silicone gel/epoxy



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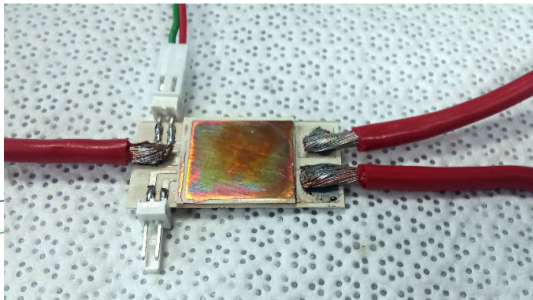
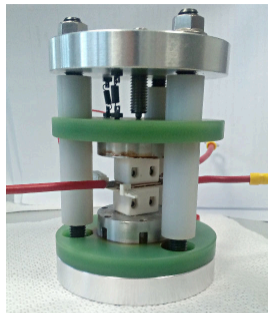
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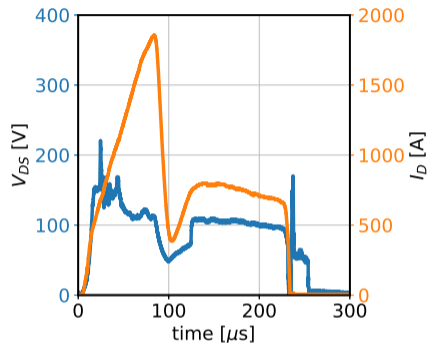
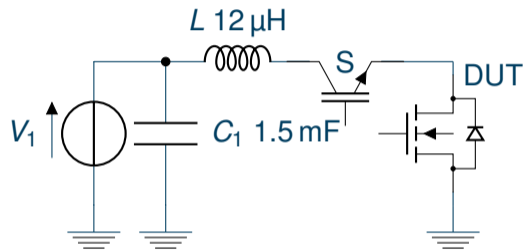
Test Setup – 1

Sample	Encapsulant	Clamp	Switch
Module A	None	Yes	MOS 1
			MOS 2
Module B	Silicone	Yes	MOS 1
			MOS 2
Module C	Epoxy	No	MOS 1
			MOS 2
Module D	Silicone	Yes	MOS 1
			–



- ▶ Dies tested individually
- ▶ “Clamp” used for modules A, B and D
- ▶ MOS 2 of module D not connected

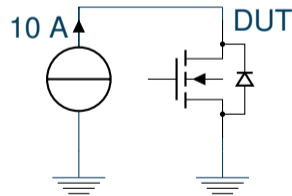
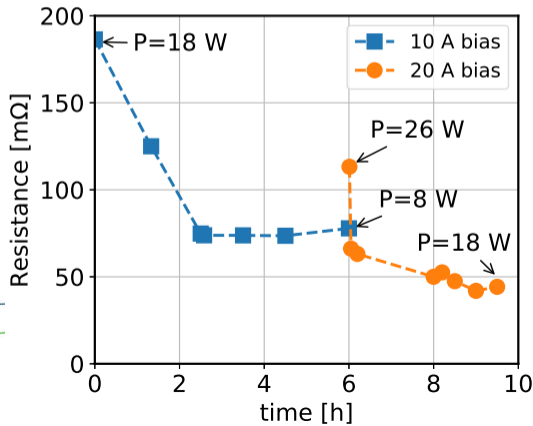
Test Setup – 2



- ▶ Short circuit test for various energy levels (1 to 20 J)
- ▶ Inductance consequence of tester wiring
- ▶ Activation of protection switch S causes complex waveforms

Test Setup – 3

- ▶ After failure, modules are biased for 6 h at 10 A
- ▶ Short-circuit failure mode considered stable if $R_{final} < R_{init}$
- ▶ In some cases longer test, with 20 A

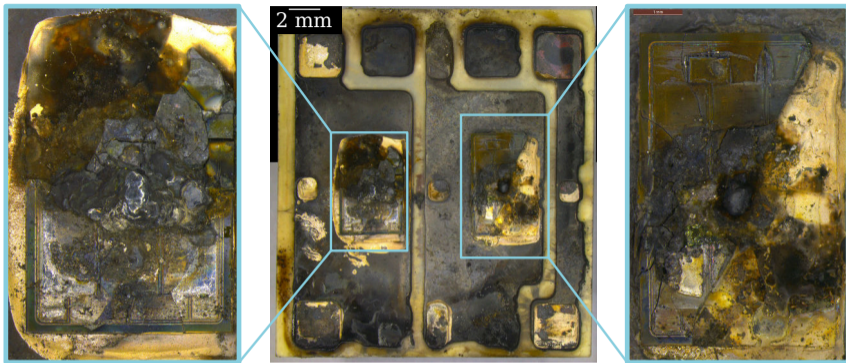


Results

	Encapsulant	Clamp	Switch	E [J]	R_{init} [mΩ]	R_{final} [mΩ]	Failure mode
A	None	Yes	MOS 1	–	186	77	SC
			MOS 2	8.8	201	128	SC
B	Silicone	Yes	MOS 1	20	165	120	SC
			MOS 2	1	188	167	SC
C	Epoxy	No	MOS 1	9.7	–	–	OC
			MOS 2	–	–	–	–
D	Silicone	Yes	MOS 1	2.24	180	158	SC
			–	–	–	–	–

- ▶ Module C separated during first test, causing open circuit
- ▶ All other modules exhibited stable short circuit

Analysis



- ▶ Dies largely broken because of short circuit
- ▶ Change in color, oxydation of module
 - ▶ caused by high temperature during stability test
- ▶ Metal infiltrated in SiC cracks

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Conclusions – 1

- ▶ Sandwich module proposed for fail-to-short behaviour
 - ▶ Relatively simple manufacturing process
 - ▶ Silver sintering as single bonding material
 - ▶ No degradation of SiC dies performance observed
 - ▶ Allows for dual-side cooling
- ▶ Short-circuit test up to 2000 A
 - ▶ “Clamped” modules were found to fail in short-circuit
 - ▶ Stable short-circuits observed after 6h
 - ▶ Final resistances 3-7 times higher than $R_{DS(on)}$ of SiC MOSFETs

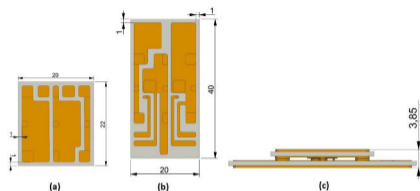


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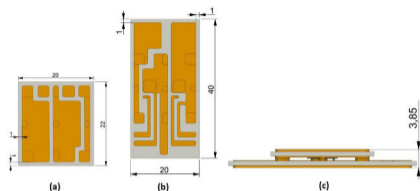


Conclusions – 2







- ▶ Fail-to-Short behaviour with SiC dies requires:
 - ▶ To prevent the Ceramic tiles from separating
 - Need for strong mechanical clamp/frame
 - Soft encapsulant probably better for gases to escape
- ▶ To provide massive interconnects:
 - ▶ Wirebonds would act as fuses
 - ▶ Need to supply metal to fill the cracks in the dies
 - ▶ Heat dissipation at failure points help reducing the resistance

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-  I. Dchar, C. Buttay, and H. Morel, "SiC power devices packaging with a short-circuit failure mode capability," *Microelectronics Reliability*, 2017.
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Thank you for your attention

<https://www.supergrid-institute.com>

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