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# Thorough investigation of Si-nanocrystal memories with high-k interpoly dielectrics for sub-45nm node Flash NAND applications

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## Abstract

In this paper we show for the 1<sup>st</sup> time that Silicon nanocrystal (Si-ncs) memories with high-k (HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> and HfAlO) interpoly dielectrics (IPD) can offer excellent behaviour in the Fowler-Nordheim regime, with great relevance for future sub-45nm NAND memory generations. We significantly advance the state-of-the-art by showing a strict correlation between the different IPD properties (high-k dielectric constants, leakage currents) and the performance obtained on memory transistors down to 90nm gate lengths. In particular the results demonstrate that HfAlO IPDs combine the fast p/e and good 10<sup>5</sup> cycles endurance behaviour of HfO<sub>2</sub> and the long retention of Al<sub>2</sub>O<sub>3</sub> with no activation up to 125°C. Then, in order to boost the memory window, we also integrated a hybrid Si-nc/SiN layer floating gate, with a HfAlO based IPD. It is shown that a 6V  $\Delta V_{th}$  can be achieved, with good retention and cycling behaviours. Finally, a physical model of Si-nc memories is introduced which explains the impacts of IPD characteristics on memory performance.

## Introduction

The large success of mobile equipment is leading to a dramatic increase of the market for NAND Flash, key devices for mass data storage [1]. Discrete trap memories, such as TANOS [2] and Si-nc memories [3,4] are one of the most suitable candidates to push integration density further beyond the 45nm node, because of their good scalability, robustness against SILC and low floating gate (FG) to floating gate coupling. In particular, Si-nc memories offer the potential of better data-retention at high temperature (the stored electrons being trapped in the Si-nc energy conduction band, rather than in temperature-activated deep traps of nitride), as well as mitigated lateral charge migration (the Si-ncs being isolated from one to the other by silicon dioxide rather than nitride). However, up to now, Si-nc memories have always shown poor FN program/erase characteristics, due to the small Si-nc/control gate coupling. In order to overcome this issue, engineering of the tunnel dielectric and/or IPD [5, 6] is necessary. In particular, in this paper, we present for the 1<sup>st</sup> time to our knowledge an exhaustive experimental and theoretical study of Si-nc memories where the conventional HTO or oxide/nitride/oxide (ONO) interpoly dielectric is replaced by HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> or HfAlO based IPD. Excellent performance and clear correlations between the device electrical results and the IPD material properties are shown. We also suggest how to solve another issue of Si-nc devices, which makes them poorly interesting for multi-level NAND applications, i.e. the relatively small programming window. As a possible solution we propose the addition of a thin SiN layer over the Si-ncs, which allows for a significant increase of the memory window. Our approach is widely validated through in-depth analysis of Si-nc memories with HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> or HfAlO IPD, based on several material results, electrical data on memory transistors, physical modelling and TCAD three-dimensional simulations.

## I. Device fabrication

*Si-nc memories (samples S1 to S4)* – Si-ncs were deposited by CVD ( $\Phi \sim 6\text{nm}$ ,  $d \sim 9\text{E}11\text{cm}^{-2}$ ) on a 4nm thick thermally grown tunnel oxide. Si-ncs were passivated by a 750°C NH<sub>3</sub> nitridation. Then different IPD stacks were deposited, composed of an 8nm high-k layer (HfO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub> or HfAlO with  $\sim 30\%$  of Hf) sandwiched between two 4nm-thick HTOs (S1 to S3, Fig.1). Their respective EOT are 10nm, 10.5nm and 11.2nm. Poly-Si was used as a control gate. On some wafers, the interpoly HTO top oxide was skipped to reduce the EOT of the stack (S4, Fig.1). In this case, a TiN control gate was deposited. The gate length was defined by electron beam lithography, down to 90nm.

*Si-nc/ SiN memories (sample S5 and S6)* – In this case, Si-ncs were deposited by CVD ( $\Phi \sim 8\text{nm}$ ,  $d \sim 9\text{E}11\text{cm}^{-2}$ ) and capped in-situ by a 2nm SiN layer. HfAlO based 3-layer (S5) and 2-layer (S6) IPD were integrated.

Fig.1 presents Si-ncs SEM plan views and TEM cross sections of the memory devices. Fig.2 shows the infrared spectra of HfAlO layers, demonstrating the progressive shift of the AlO binding energy as %Hf increases. The optical bandgap of HfAlO layers (Fig.2) increases linearly with %Al.

## II. Results and discussion

**1. IPD comparison** - Fig.3 shows the IV characteristics of high-k based 3-layer IPD capacitors. One can observe that at high fields, the insulation capabilities increase with the Hf content of the high-k [7]. Moreover, lower leakage currents are measured at high voltages on high-k based stacks with respect to HTO. **Program erase** (p/e) characteristics in FN-FN regime of the 3-layer IPD Si-nc memories are presented in Figs.4-5. These results demonstrate the feasibility of NAND applications for Si-nc memories with high-k IPD thanks to the improved coupling ratio and low IPD leakage current at high voltages (Fig.3). It also appears that the memory window is the largest with an HfO<sub>2</sub> based IPD (fig.6). Indeed, as the IPD EOT decreases, the coupling ratio increases, leading to higher

$\Delta V_{th}$ . In fig.7 is plotted the required program voltage  $V_p$  for a 2.5V  $\Delta V_{th}$  in 1ms for the different IPD stacks, and it appears that  $V_p$  is reduced as the IPD EOT decreases, confirming our former hypothesis.

**Cycling** characteristics are presented in Fig.8. With HfO<sub>2</sub> IPD, a constant memory window of  $\sim 3\text{V}$  is maintained even after 10<sup>5</sup> cycles, with a  $\sim 500\text{mV}$   $V_{th}$  drift. The higher  $V_{th}$  drift of Al<sub>2</sub>O<sub>3</sub> based IPD devices may be explained by the higher electric field in the Al<sub>2</sub>O<sub>3</sub> layer (due to higher dielectric constant) for a given p/e condition. HfAlO offers a good compromise between HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> in terms of memory window and low  $V_{th}$  drift.

**Retention** characteristics of the different memory devices at RT and 125°C are plotted in Figs.9-10. Since the tunnel oxide thickness was the same for the different samples, we can conclude that the retention time is governed by the leakage current through the IPD stack. We observe that the charge loss is the highest for the HfO<sub>2</sub> IPD memory while the Al<sub>2</sub>O<sub>3</sub> IPD exhibits the best retention time and the slowest charge decay rate. This is consistent with the more elevated barrier height of Al<sub>2</sub>O<sub>3</sub>, which is relevant especially at low applied electric fields. Finally, the charge life time was extracted from retention measurements (Fig.11), showing no temperature activation up to 125°C, and thus demonstrating the good high temperature behaviour of Si-nc memories.

## 2. Si-nc/SiN floating gate memories

Fig.12 plots the program erase characteristics of Si-ncs/SiN double layer floating gate memories. With HfAlO three-layer IPDs, large memory windows of nearly 6V for 1ms programming time can be achieved. A reduction of p/e voltages by 2V is possible by using a 2-layer IPD rather than a three-layer one. Fig.13.a shows the feasibility of 2-bits/cell operation in HC programming mode. The 2-bits are clearly distinguished, with a 25%  $\Delta V_{th}$  separation between both of them, demonstrating the discrete character of the Si-nc/SiN floating gate. Retention characteristics at room temperature (fig.13.b) show the same charge decay than Si-nc memories. However, a stronger activation is measured at 125°C compared to Si-nc memories due to the contribution of SiN traps. Good endurance performance (fig.14) is also achieved. The memory window narrowing (not observed in Si-nc memories), can be explained by charges trapped in the SiN layer, which are more difficult to remove.

## III. Modelling and numerical simulations

The physical model of Si-nc devices with high-k IPDs is illustrated in Fig.15. The writing current through the tunnel oxide was calculated using the WKB formalism. Leakage currents through the IPD are given by experimental data (Fig.3) [7]. The trapped charge in Si-ncs is calculated by the balance of the filling and emptying currents through the tunnel and interpoly dielectrics [8], respectively  $J_{tun}$  and  $J_{IPD}$ . With a HTO IPD,  $J_{IPD} \sim J_{tun}$  and FN programming is not efficient. On the other hand with high-k IPD  $J_{IPD} \ll J_{tun}$ , and the memory window is essentially governed by  $J_{tun}$ , controlled by the memory coupling ratio. Indeed as the IPD EOT decreases, the injected charge in the FG increases (due to higher coupling ratio) leading to a wider  $\Delta V_{th}$ , which is in agreement with our experimental results.

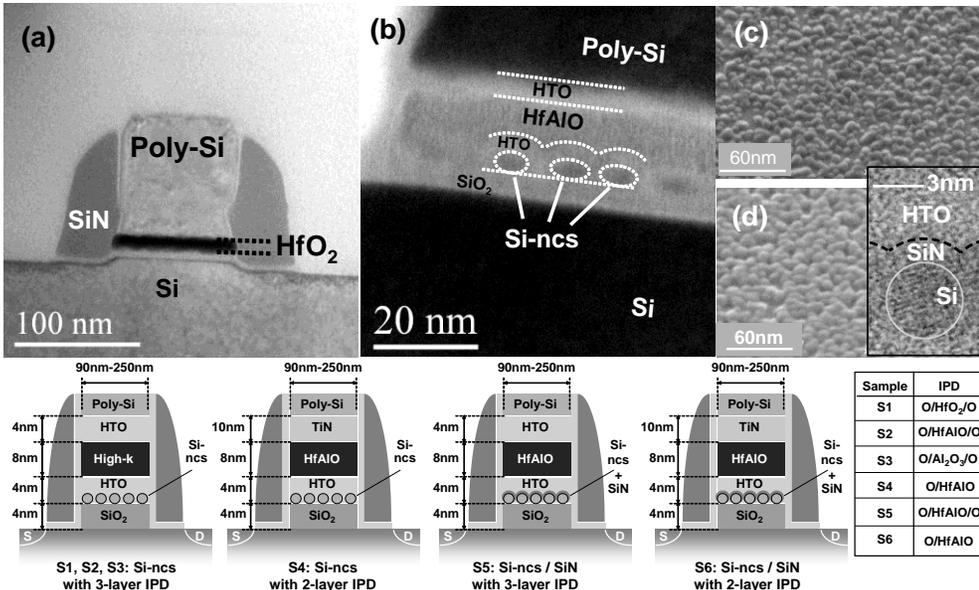
The endurance measurements (Fig.8) show that the IPD has a strong influence, meaning that trapping in the high-k layer rather than in the tunnel dielectric (as usually considered for cycling [9]) should be involved. We have therefore developed a cycling model (Fig.16) that takes this trapping into account and have arbitrarily assumed it as happening along a plane in the middle of the high-k film. We show here the result of the cycling model in the case of S1 (IPD with HfO<sub>2</sub>). The trapping in the HfO<sub>2</sub> is considered by using an empirical power law (used in [10] for silica; see modelling details in Fig.16) that leads to good correspondence with the experimental results.

TCAD 3D simulations (Fig.17) using Synopsys tools were performed to evaluate the FG to FG coupling for future generations of ultra dense NAND memories [1]. A strong reduction ( $\sim 2$  decades) of the FG cross coupling in the 32nm node with Si-ncs is obtained compared to the case of a poly-Si FG, due to reduced coupling areas. This leads to a lower parasitic  $\Delta V_{th}$  of the disturbed cell for a given FG charge in the master cell. Note that for such scaled Si-nc memory devices where a very small number of Si-ncs per cell is involved, the use of self assembled FGs [11] will reduce the dispersion of the memory characteristics.

## Conclusions

We successfully demonstrated the FN operation of Si-nc memories by integrating high-k IPDs, due to the improved coupling ratio and reduced IPD leakage currents. HfAlO based IPD combines the good quality of HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> dielectrics, allowing 1ms programming, good endurance and long retention. Moreover  $\Delta V_{th}$  was enhanced to 6V by using a double Si-ncs/SiN FG with an HfAlO IPD. Finally physical modelling and TCAD simulation allow to explain the advantages of Si-ncs and high-k IPD on the memory characteristics.

## I - Material device



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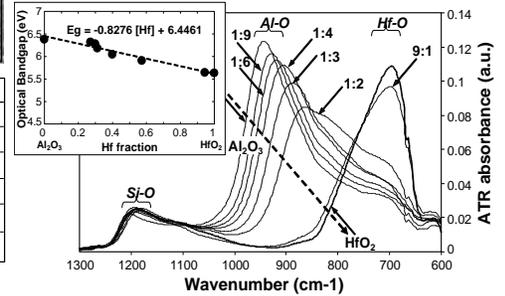


Fig.1 (a-b) TEM cross sections of 3-layers IPD memories. (c-d) SEM plan views of deposited Si-ncs (c) and Si-ncs/SiN (d) layers. Inset: TEM cross section of the double Si-nc/SiN layer. Bottom: schematics of the 3-layer and 2-layer IPD Si-nc and Si-nc/SiN memory devices studied in this work.

Fig.2 Infrared spectra of 6nm ALD deposited HfAlO films of various Hf:Al compositions. Inset: measured optical bandgap (ellipsometry) vs the Hf fraction of HfAlO alloys.

## II.1 - High-k interpoly comparison

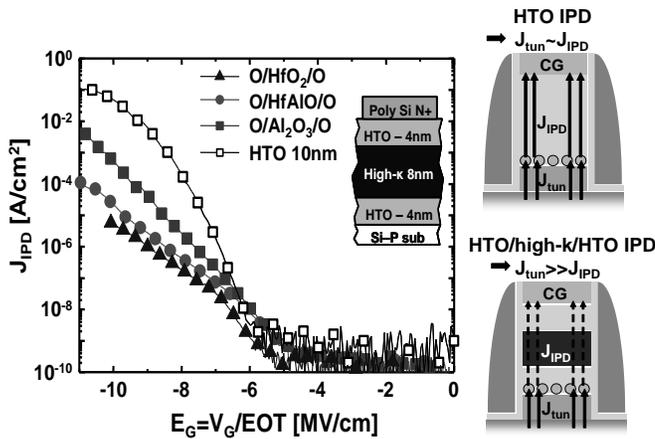


Fig.3 Leakage currents of 3-layer interpoly capacitors. Different O/high-k/O stacks are measured, HTO reference is also represented. On the right: schematics of the filling and emptying currents during writing.

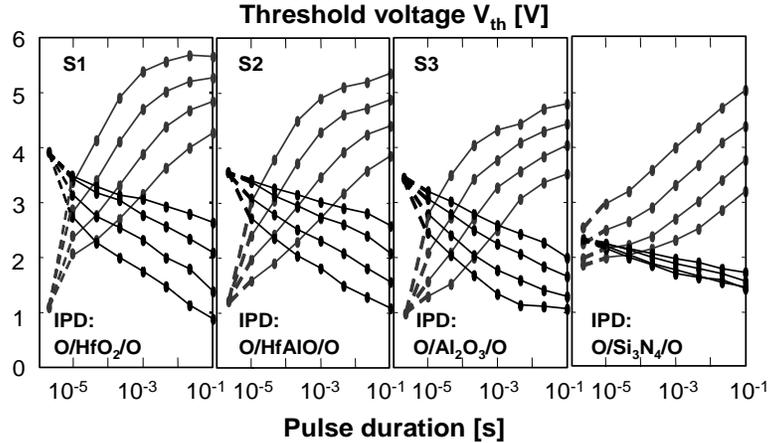


Fig.4 Program erase characteristics of Si-nc memories with various O/high-k/O IPD stacks ( $W \times L = 0.5 \mu\text{m} \times 0.25 \mu\text{m}$ ).  $V_P$ : 14V to 17V.  $V_E$ : -12V to -15V.

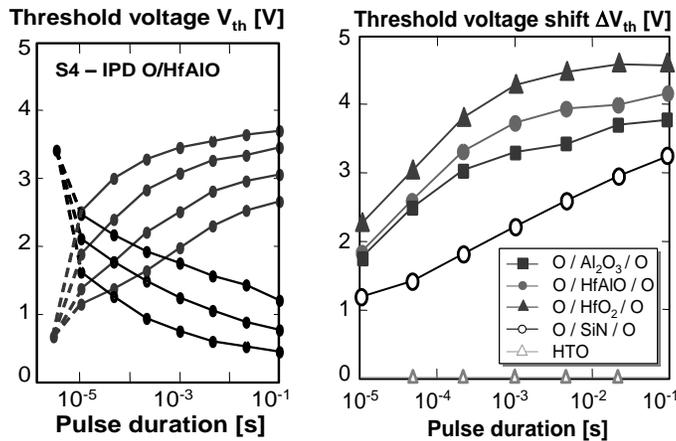


Fig.5 Program erase characteristics of sample S4.  $V_P$ : 10V to 13V.  $V_E$ : -11V to -13V.

Fig.6 Comparison of  $\Delta V_{th}$  for a program voltage of 18V for memory devices with various 3-layer IPDs. Control devices with ONO and HTO IPD are also shown

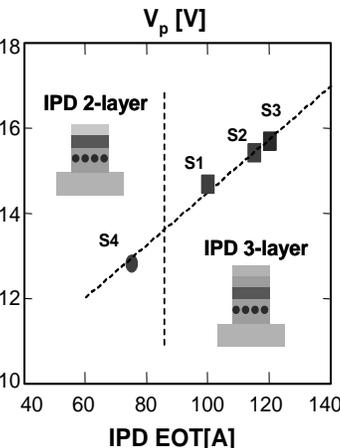


Fig.7 Program voltage required for a  $\Delta V_{th}$  of 2.5V with 1ms pulses, vs IPDs EOT. Different 3-layer and 2-layer IPD are shown.

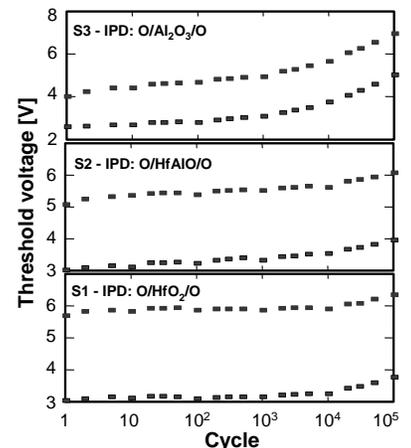


Fig.8 Endurance characteristics of 3-layer IPD memories (S1 to S3), with various O/high-k/O IPDs. Program:  $V_P = 18\text{V}/1\text{ms}$ , erase:  $V_E = -15\text{V}/1\text{ms}$ .

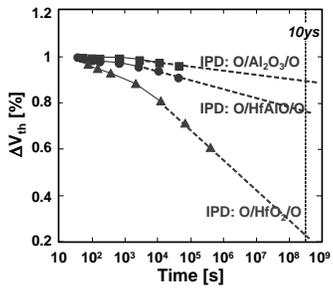


Fig.9 Normalized retention curves at RT of the programmed state ( $\Delta V_{th0}=2.5V$ ) for devices S1 to S3.

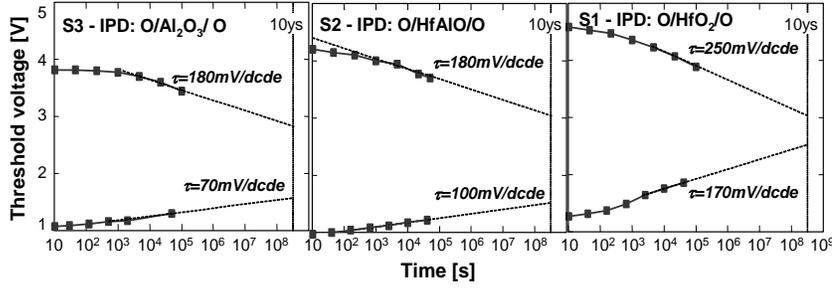


Fig.10 Retention characteristics at 125°C of 3-layer IPD memories (S1 to S3), with various O/high-k/O IPD stacks (S1 to S3).

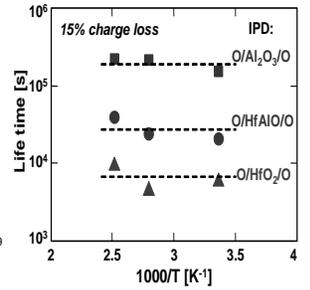


Fig.11 Life time vs measurement temperature for samples S1 to S3.

## II.2 - Si-nc/SiN floating gate memories

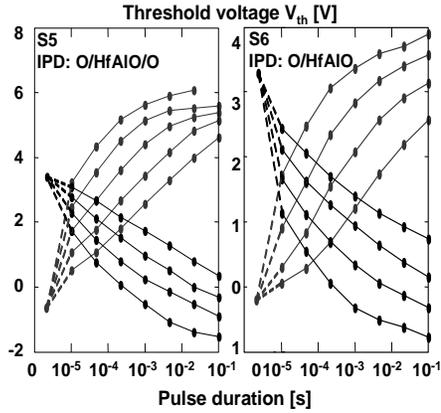


Fig.12 Program erase characteristics of Si-nc/SiN memories (S5 and S6). S5:  $V_p=14V$  to  $18V$ ,  $V_e=-12V$  to  $-15V$ . S6:  $V_p=10V$  to  $13V$ ,  $V_e=-10V$  to  $-13V$ .  $W \times L=0.5\mu m \times 0.25\mu m$ .

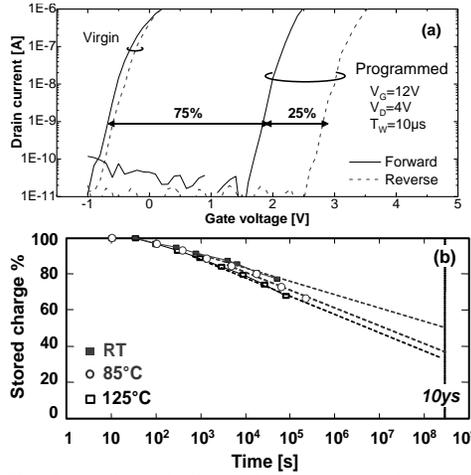


Fig.13 (a)  $I_d(V_g)$  in forward ( $V_d=1.5V$ ) and reverse ( $V_d=-1.5V$ ) modes for S5. (b) Normalized retention curves of the programmed states of S5 ( $\Delta V_{th}=3.5V$ ).

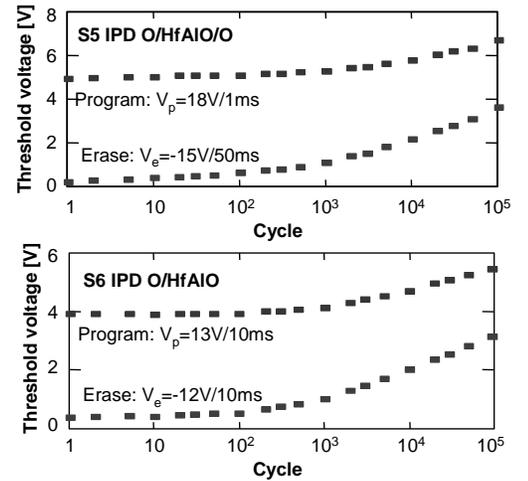


Fig.14 Endurance characteristics of Si-nc/SiN memories with 3-layer (S5) and 2-layer (S6) IPDs.

## III - Modeling and simulations

$$\bullet J_{tun}(V_{FG}) = \frac{4\pi q^3 m_{Si} k_B T}{h^3} \int_0^\Phi \Theta_{sub}(E, V_{FG}) \ln \left[ 1 + \exp\left(\frac{E_{Fsub} - E}{k_B T}\right) \right] dE$$

$$\bullet \Theta_{sub}(E, V_{FG}): \text{transparency with WKB approximation}$$

$$\bullet V_{FG} = \frac{C_{IPD} V_G}{C_{tun} + C_{IPD}} + \frac{Q_{FG}}{C_{tun} + C_{IPD}}$$

$$\bullet \frac{dQ_{FG}}{dt} = J_{tun}(V_{FG}) - J_{IPD}(V_G - V_{FG})$$

$$\bullet \Delta V_{th} = \frac{-Q_{FG}}{C_{IPD}} R_{dot}$$

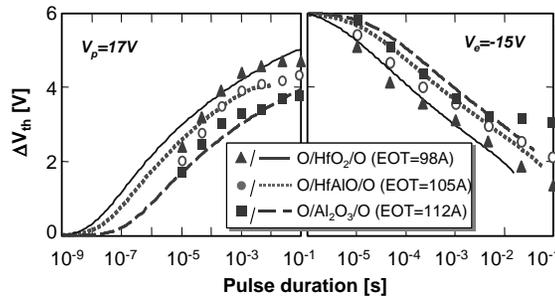


Fig.15 Simulated program/erase characteristics. Lines: simulations (Si-ncs area coverage [8];  $R_{dot}=50\%$ ), symbols: data. In high-k IPD memories, as  $J_{IPD} \ll J_{tun}$ , the memory window is essentially controlled by the IPD EOT.

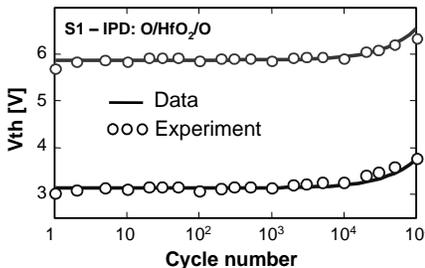


Fig.16 Simulated endurance characteristics for S1, assuming a progressive trapping in the middle of the IPD stack during cycling, modelled by an empirical law [9].  $\nu=-0.2$ ,  $K=6.35 \cdot 10^{-7}$ .

$$V_{th} = \frac{-Q_{FG}}{C_{IPD}} R_{dot} + \frac{-Q_{IPD}}{2C_{IPD}} + V_{th0}$$

$$Q_{IPD}(Q_{inj}) = \frac{-K}{\nu+1} |Q_{inj}|^{\nu+1}$$

$$V_{th0}: \text{neutral } V_{th} \quad Q_{IPD}: \text{charge trapped in IPD} \quad \nu = -0.2 \quad K = 6.35 \cdot 10^{-7}$$

During one w/e cycle (w/e: write/erase time):

$$Q_{inj} = \int_0^{t_w} |J_2 [V_{GW} - V_{FG}(t)]| dt + \int_0^{t_e} |J_2 [V_{GE} - V_{FG}(t)]| dt$$

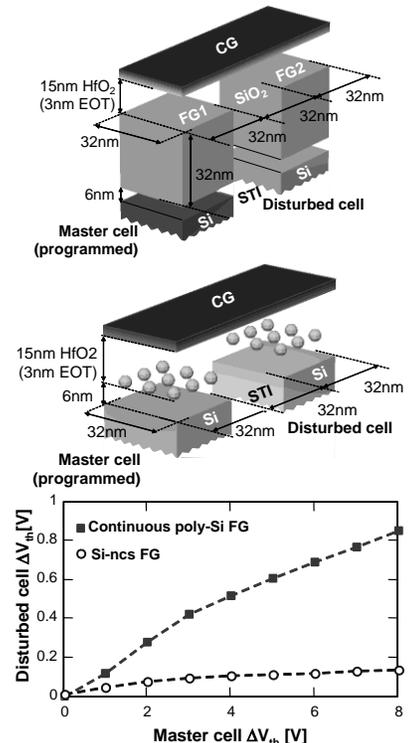


Fig.17 TCAD 3D simulation of the FG/FG cross coupling in a poly-Si FG memory and in a Si-nc memory.  $\Delta V_{th}$  is analytically calculated from the simulated FG potentials.