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# Flexible organic/inorganic hybrid field-effect transistors with high performance and operational stability

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## Abstract

The production of high quality semiconducting nanostructures with optimized electrical, optical and electromechanical properties is important for the advancement of next-generation technologies. In this context, we herein report on highly obliquely aligned single-crystalline zinc oxide nanosheets (ZnO NSs) grown *via* the vapor-liquid-solid approach using r-plane (01-12) sapphire as the template surface. The high structural and optical quality of as-grown ZnO NSs has been confirmed using high resolution transmission electron microscopy and temperature-dependent photoluminescence, respectively. To assess the potential of our NSs as effective building materials in high performance flexible electronics, we fabricate organic (parylene C) / inorganic (ZnO NS) hybrid field-effect transistor (FET) devices on flexible substrates using room temperature assembly processes. Extraction of key FET performance parameters suggest that as-grown ZnO NSs can successfully function as excellent n-type semiconducting modules. Such devices are found to consistently show very high on-state currents ( $I_{on}$ )  $> 40 \mu\text{A}$ , high field-effect mobility ( $\mu_{eff}$ )  $> 200 \text{ cm}^2/\text{Vs}$ , exceptionally high on/off current modulation ratio ( $I_{on/off}$ ) of around  $10^9$ , steep sub-threshold swing (s-s)  $< 200 \text{ mV/decade}$ , very low hysteresis and negligible threshold voltage shifts with prolonged electrical stressing (up to 340 min). The present study delivers a concept of integrating high quality ZnO NS as active semiconducting elements in flexible electronic circuits.

**Keywords:** Zinc oxide, nanosheets, organic / inorganic hybrid, field-effect transistors, flexible substrates

## 1. Introduction

There exist burgeoning interest in autonomous smart systems that can be manufactured on mechanically flexible substrates for the internet-of-things (IoT), biomedical sensor nodes, military and/or civil surveillance and consumer electronics. In this regard, low-temperature processable organic / inorganic hybrid based electronic devices, such as field-effect transistors (FETs),<sup>1-7</sup> micro/nano generators,<sup>8,9</sup> light emitting diodes,<sup>10,11</sup> photodetectors<sup>12</sup> and solar cells<sup>13</sup> offer practical solutions towards realizing low-cost, flexible self-powered autonomous systems.<sup>14</sup> The FET represents the basic building block for complex electronic circuits facilitating the development and evolution of the Internet, mobile electronics, computers and many other technologies. Progressively, enormous efforts have been made to develop new materials with enhanced functionalities as fundamental elements for future FET devices. As a one potential candidate,  $\pi$ -conjugated organic semiconductors offer several advantages over traditional FET modules, these include: (i) low elastic modulus (flexibility), (ii) high transparency and (iii) allowed formulations in most organic solvents and subsequent room temperature processing over large area flexible substrates in roll-to-roll fashion, makes them suitable for next-generation of large area flexible thin-film electronics.<sup>1,3,15</sup> However, the wide spread use of organic semiconductors as an active semiconducting channel element in high performance electronics is severely compromised due to poor charge carrier mobility,<sup>16</sup> sensitivity to process conditions and stability over time.<sup>17</sup>

Single-crystalline semiconducting inorganic nanomaterials have been proposed as alternative advanced materials for the development of next generation ultra-efficient low-cost electronics, due to their enhanced mechanical flexibility, single-crystalline nature and excellent electrical transport characteristics. Moreover, the possibility to suspend them in solutions, like inks,

allowed to use inexpensive printing techniques for large area device fabrication.<sup>6</sup> Significant developments in the synthesis of functional semiconducting nanomaterials *via* self-assembly from the bottom-up approach are now offering high quality materials.<sup>18</sup> From the plethora of single-crystalline semiconducting nanostructures under active research studies, notable FET device applications have been demonstrated in the past.<sup>19–25</sup> One of the key challenges associated to the scalability of nanomaterial based FETs is the exquisite control over the nanostructure's morphology, location and orientation during the growth process, while keeping their high crystalline quality intact. Vapor-liquid-solid (VLS) method<sup>26</sup> is routinely employed to produce a wide range of nanostructure morphologies with unparalleled material's quality for electronics, optoelectronics, and energy harvesting applications. Since the first demonstration of the VLS growth by Wagner et al., continuous refinement of the process has resulted in the growth of different varieties of semiconducting nanostructures.<sup>27,28</sup> However, the growth of orientation controlled assembly of nanostructures is still challenging.

Among various inorganic semiconductors, nanomaterials of metal oxides, such as indium oxide, tin oxide and zinc oxide (ZnO) have been intensively studied for the development of low-power transparent electronics.<sup>29</sup> As a semiconductor, ZnO exhibits a number of unique electrical and optical properties such as wide band-gap ( $\sim 3.37$  eV at room temperature), high exciton binding energy (60 meV), excellent thermal stability, and high channel mobility ( $\sim 200$  cm<sup>2</sup>V<sup>-1</sup>s<sup>-1</sup>). Moreover, ZnO nanostructure's diverse morphological compositions are finding widespread applications in next-generation nanoscale devices. During the last decade, many efforts have been made to study the growth of well-ordered ZnO nanostructures such as nanowires (NWs)<sup>26,28</sup> and nanowalls<sup>27,30</sup>. Such aligned structures have proved to be advantageous, in both vertical<sup>30</sup> and horizontal integration<sup>31</sup>, for device fabrication over large areas. Recently, few nanometer

thick two-dimensional (2D) ZnO nanosheets (NSs)<sup>32-34</sup> and/or nanomembranes (NMs)<sup>35</sup> have gained much attention because of their high surface to volume ratio, reduced flexure rigidity and superior electrical properties. Moreover, it was proposed that the surface of such 2D nanomaterial sufficiently favors contacts that resemble those from conventional thin-film technologies, where the classical metal-semiconductor theory of planar contacts may be applied.<sup>23</sup> Consequently, such 2D semiconducting nanomaterials have been employed for the realization of a number of exciting device applications such as field-effect transistors<sup>23</sup> photovoltaics<sup>36,37</sup> and piezoelectric nanogenerators<sup>38,39</sup>. Despite these several reports on the growth of NSs on sapphire substrates,<sup>32-34</sup> the exact mechanism responsible for the evolution of this type of nanostructure is still not well understood. In the present work, we have not only demonstrated exquisite growth of highly obliquely oriented single-crystalline ZnO NSs on r-plane sapphire surface, but also decoded the growth mechanism behind the growth of such aligned nanostructures using characterization techniques such as x-ray diffraction (XRD) and cross-sectional high resolution transmission electron microscopy (HRTEM). The presented growth mechanism may be applied to the growth of other nanostructures with similar hexagonal wurtzite structure such as GaN NWs on r-sapphire substrate. Moreover, we will show that such ZnO nanostructure can be used for the fabrication of next-generation semiconductor technologies such as FETs on flexible substrate which can potentially revolutionize the increasingly ubiquitous thin-film electronic technologies. The optimized fabrication process is new and can be applied to other semiconductor nanostructures. Further, the reported mobility values from the NS-FET devices (both on rigid Si/SiO<sub>2</sub> and flexible PET) are superior than most of the reported value for ZnO thin films and nanostructures such as NWs.<sup>40</sup>

## 2. Results and Discussion

### 2.1 Structural and morphological characterizations

Figure 1 show representative scanning electron microscope (SEM), x-ray diffraction (XRD) and Raman spectrum data from as-grown ZnO NSs. It can be seen from the SEM images that the ZnO NSs are obliquely aligned at approximately  $\pm 30^\circ$  tilt with respect to the sapphire surface. From the XRD pattern, the peak appearing at  $2\theta$   $56.5^\circ$  was successfully assigned to hexagonal (11-20) ZnO in the wurtzite phase. It is worth noting that no other ZnO diffraction peaks were observed within the measured range ( $2\theta = 20$  to  $80^\circ$ ), consistent with the heteroepitaxial growth of a preferential a-axis [11-20] oriented ZnO thin-film on the r-plane substrate.<sup>41</sup> The crystalline quality of as-grown ZnO NSs was confirmed by micro-Raman measurements, as shown in Figure 1d. From this data, the two dominant peaks centered at 98.6 and 437.4  $\text{cm}^{-1}$  were successfully assigned to the two non-polar first-order Raman active  $E_2$  (low) and  $E_2$  (high) modes, described by the Raman selection rules for wurtzite ZnO (with  $C_6v$  point group symmetry). Moreover, the peaks were found to show very low values with a full width half maximum (FWHM) of 2 and 5  $\text{cm}^{-1}$ , respectively. The Raman spectra suggest the production of high crystal quality ZnO. Another important observation to note from the experimental data, shown in Figure 1d, is the appearance of two smaller peaks at 330 and 574  $\text{cm}^{-1}$ . While the former can be ascribed to the second-order Raman processes, the latter suggests that the c-axis of wurtzite ZnO is oriented parallel to the r-plane substrate. To confirm this hypothesis, HRTEM characterizations, carried on the as-prepared lamellas using FIB (focused ion beam), are discussed in the next section.

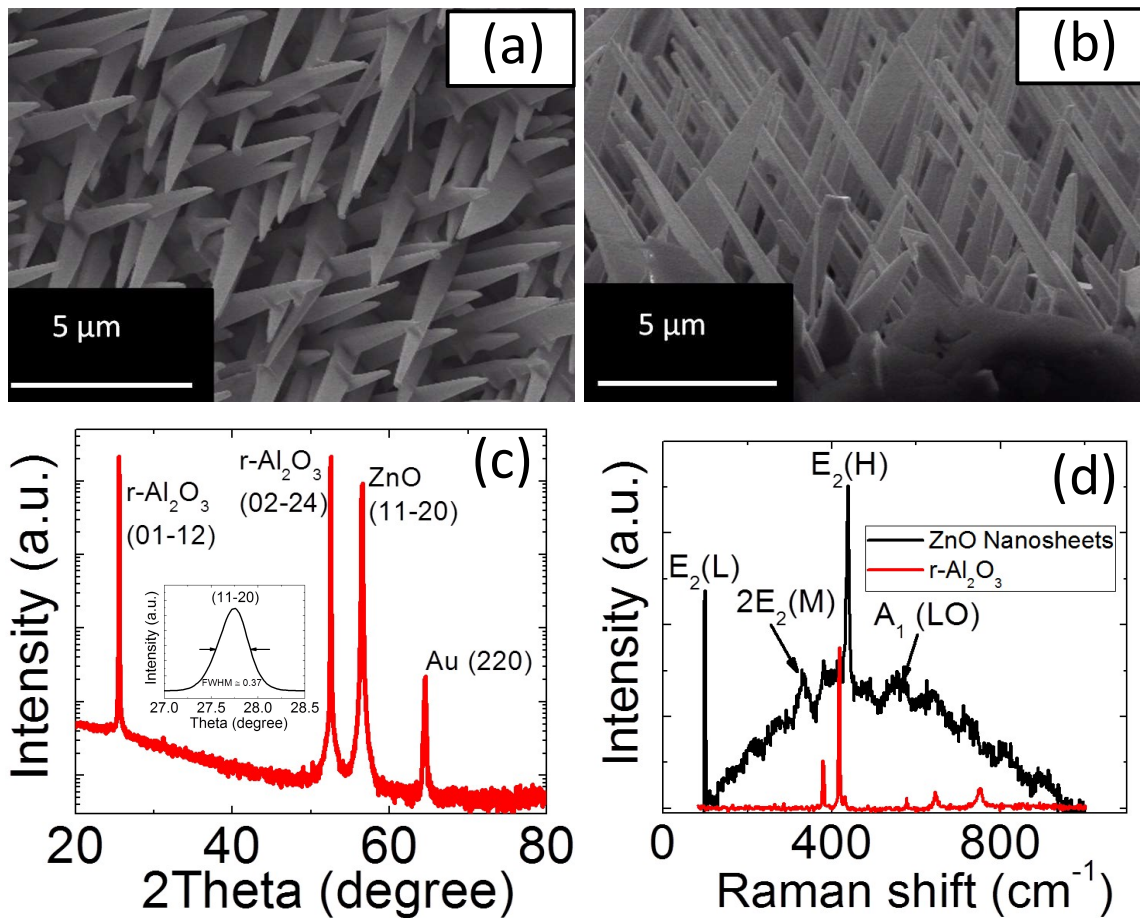


Figure 1. (a) and (b) are the top view and cross-sectional SEM images of the as grown-ZnO NSs. (c) typical XRD pattern of ZnO NSs, and (d) Raman spectra measured from the forest of ZnO NSs on r-plane Sapphire substrates.

## 2.2 Proposed Growth mechanism

In order to propose the growth mechanism of the present obliquely aligned ZnO NSs, we used HRTEM analysis. Prior to initiating the VLS growth procedure, surface morphology of as-received and annealed ( $\sim 800$  °C) r-plane sapphire substrates, were examined by AFM (atomic force microscopy) technique. This pre-conditioning step sufficiently sharpened the surface topography of as-received r-plane substrates due to re-arrangement of adatoms because of the increase in thermal energy<sup>42,43</sup> (Figure S1, AFM images of r-sapphire surface (a) pristine, (b)

annealed at 800 °C). After the thermal annealing step, sapphire substrates were coated with ~2 nm thick Au films by e-beam evaporation. To understand the growth mechanism, standard photolithography was also used to selectively pattern Au rectangular stripes. During the ramping process, the dewetting of the 2 nm thick Au film, created nanoparticles (NPs) droplets on the substrate surface that served as catalyst sites during growth. At the dwell temperature (~ 900 °C), the Zn vapor source was supplied from the carbothermal reduction of ZnO powder which was mixed with carbon powder at a 1:1 weight ratio. The growth plateau was held for 180 min. After VLS growth, the bulk of the catalyst patterns were covered with a dense forest of ZnO NSs that are obliquely aligned around  $\pm 30^\circ$  on substrate surfaces (Figure 1a-b). On the other hand, guided growth of horizontal ZnO nanonecklaces (NNs) on r-plane sapphire (Figure S2, SEM images (at various magnification) of ZnO NNs: (a) at 180x, (b) 2000x, (c) 35000x, and (d) 130k magnification) were found to protrude from edges of the patterned Au, similar to previous reports<sup>44</sup>. According to the authors, NNs grew along the c-axis [0001] direction of wurtzite ZnO on the sapphire substrate in the [10-11] direction, yielding a RT lattice mismatch of around 1.5 %.

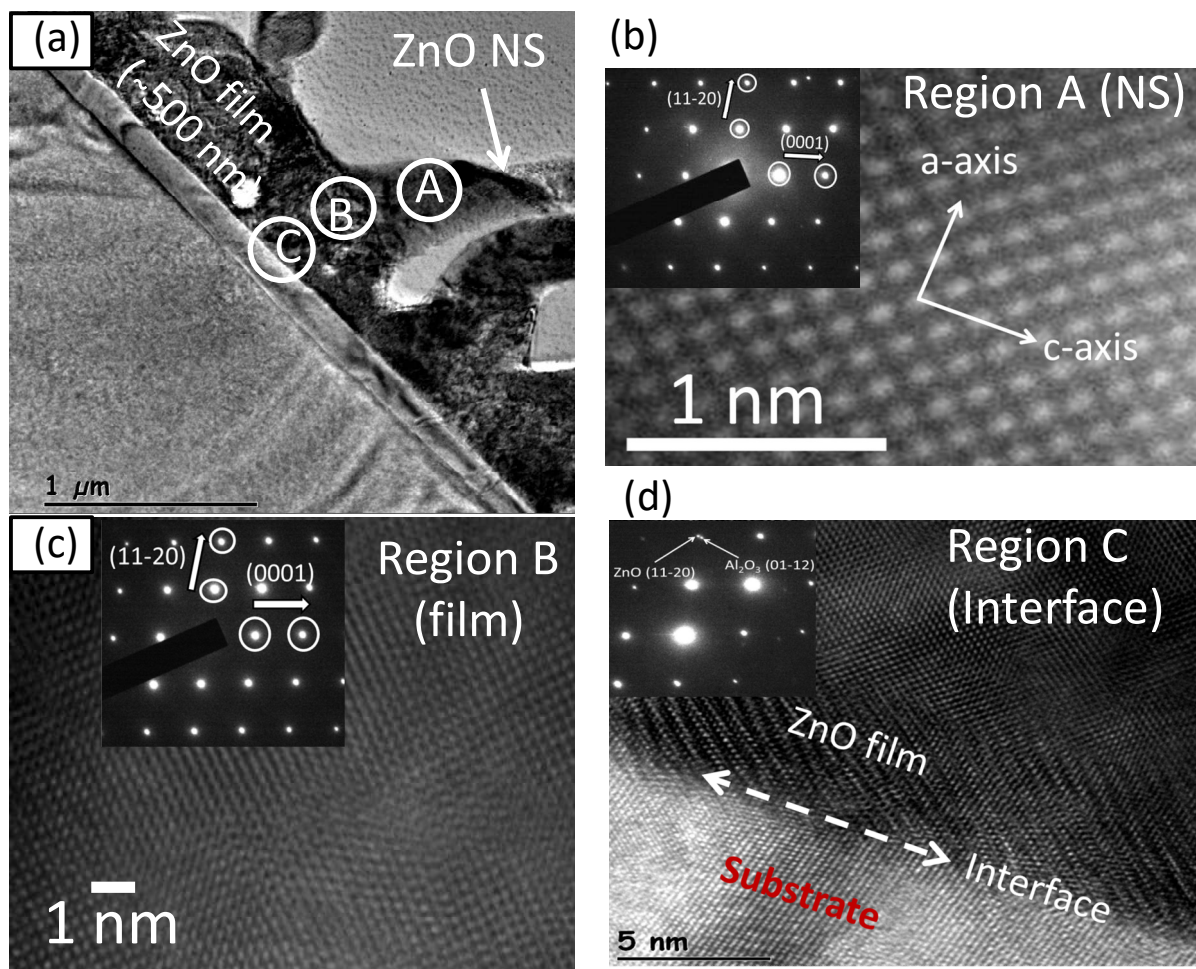


Figure 2. (a) TEM image of the prepared lamella and region marked for HRTEM characterizations. HRTEM characterizations and SAED pattern (b) ZnO NS, (c) ZnO film, and (d) interface between ZnO film and *r*-sapphire surface.

Figure 2 show HRTEM images performed on ZnO NS lamellas. From Figure 2a, it can be clearly seen that a ~500 nm thick ZnO film is present at the base. Based on this observation, we can conclude the following: (i) prior to the ZnO NS formation, a heteroepitaxial ZnO film initially form, on the sapphire surface. It has been shown that epitaxial (11-20) ZnO thin-film grows on *r*-plane sapphire substrates,<sup>41</sup> identical to the ones used in this work. However, unlike to ref. [41], we followed the VLS growth mechanism for the growth of ZnO NSs with Au NPs as a catalyst.

In the VLS growth process, the presence of a similar film, at the base of nanostructure, is commonly reported in the literature.<sup>45</sup> Kuykendall et al. observed a similar GaN film at the base of GaN NWs.<sup>45</sup> They believe that the film is the result of frustrated nanowire growth along and at shallow angles to the substrate. Kuykendall et al. hypothesize that during the lateral growth NWs likely underwent many collisions before branching off and growing into non-sterically hindered free space. Following these reports, we also assume that the formation of this ZnO film, at the base of NSs, can be related to lateral growth of NNs.

To gain further insight into the proposed mechanism, we obtained additional HRTEM data from various different regions on a single ZnO NS, close to the ZnO film-NS interface. Three analysis regions are labeled in Figure 2a as region A, region B and region C, corresponding to the ZnO NSs, ZnO film, and r-sapphire-ZnO film interface, respectively and shown in Figure 2b-d. First we note from Figure 2c-d that the ZnO film-r-plane substrate interface was atomically sharp and the film appears to have lot of structural defects such as stacking faults and/or crystal dislocations. This observation further indicates the formation of frustrated ZnO film from the lateral growth of NNs along and at shallow angles to the substrate, similar to Ref. [45]. On this ZnO film, we found the homoepitaxial growth of obliquely aligned ZnO NSs which is devoid of any obvious stacking faults and/or crystal dislocations (Figure 2b). This epitaxial relationship is evident from both the high-resolution images and the respective selected area electron diffraction (SAED) patterns in the inset of Figure 2b and 2c.

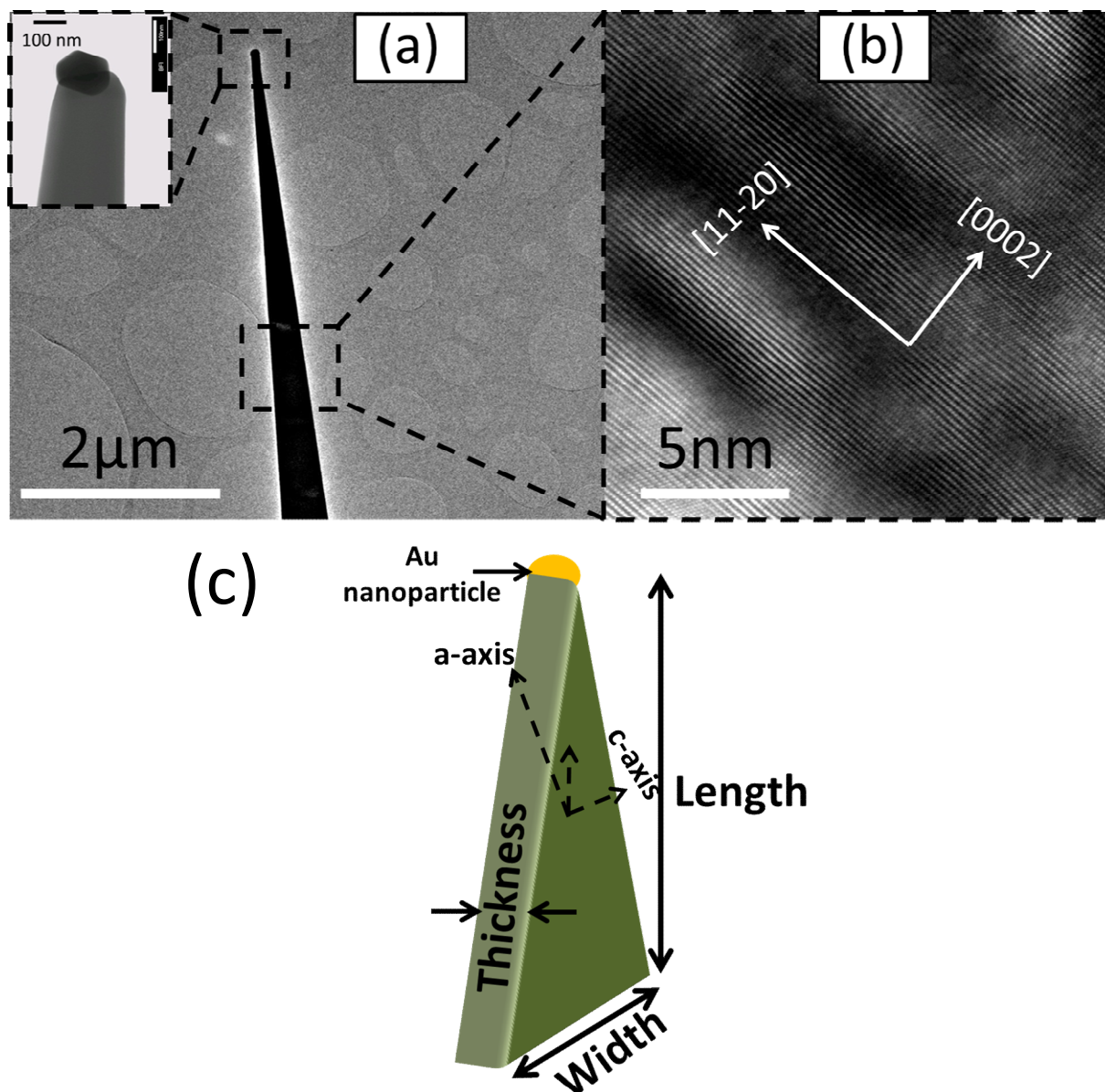


Figure 3. (a) HRTEM image of a single ZnO NS. The inset is high magnification TEM image showing the Au NP at the tip of the NS. (b) HRTEM image of ZnO NS showing the distinct lattice fringes of wurtzite ZnO confirms the single-crystalline nature of the NS and also showing the growth directions. (c) Schematic illustration of NS length, width, thickness and growth directions.

The morphology and growth axis of ZnO NSs were also characterized individually by HRTEM and schematically drawn in Figure 3. Figure 3a-b shows the resulting HRTEM images from this

investigation. A low magnification image of ZnO NS is shown in Figure 3a. From this figure, it can clearly be seen that the NSs were tapered along the growth axis, with the catalyst particle at the tapered end (inset in Figure 3a). This observation confirms the growth of the NSs by catalyst-governed VLS mechanism. The resolved lattice images in Figure 3b further confirms the single-crystalline nature of the NSs produced in this work, which predominantly grew perpendicular to the (0002) planes.

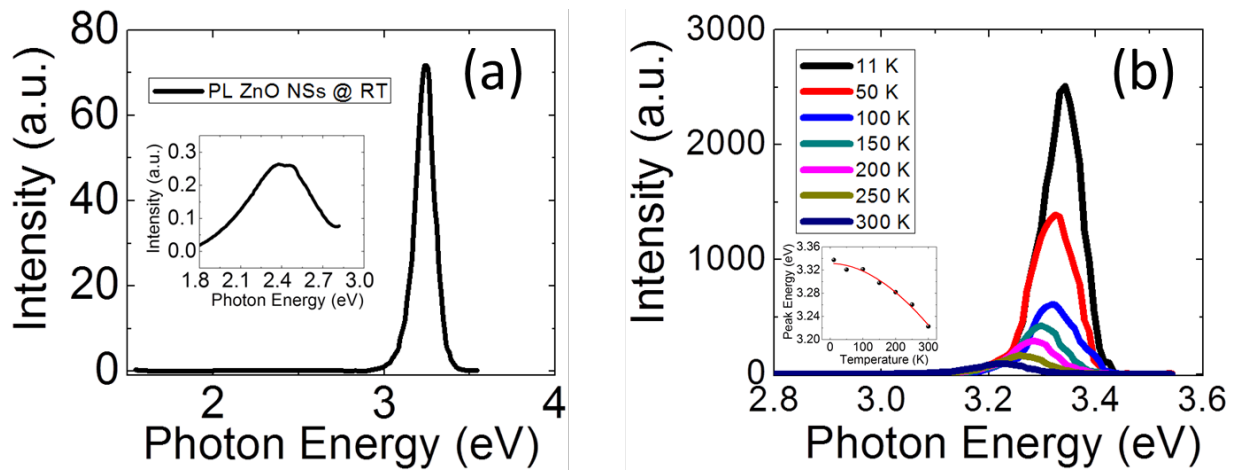


Figure 4. PL spectra of ZnO NSs measured at (a) room temperature. Inset shows the magnified view of the visible region. (b) Temperature ranges from 11 K to 300 K. Inset shows the peak energy position change with sample temperature and Varshni model fitting.

### 2.3 Optical properties of ZnO NSs

As a direct wide band-gap semiconductor, ZnO is characterized by a high excitonic binding energy of 60 meV at RT which is larger than most of the widely used semiconductors (GaN ~ 26meV or ZnSe ~20 meV) in the optoelectronic industry. Such a high excitonic binding energy makes ZnO a promising material for a wide range of optoelectronic applications such as UV lasers,<sup>46</sup> UV sensors,<sup>47</sup> etc. Moreover, nanostructured materials are expected to carry improved

optical properties because of quantum confinement effects. However, in ZnO, along with a near-band emission peak in the UV region, there is also a visible emission associated with native defects. Despite several attempts by many researchers to elucidate the exact source of these defects, the origin of the visible emissions is hotly debated.<sup>48</sup> While many studies have attributed the origin of the visible emission to intrinsic native defects such as zinc interstitial ( $Zn_i$ ), oxygen vacancies ( $V_O$ ) and zinc vacancies ( $V_{Zn}$ ),<sup>48-50</sup> other associate such visible emission to the presence of hydrogen impurities<sup>51,52</sup> in ZnO. However, irrespective of the origin of these defects, presence of deep-level (DL) emission is not acceptable for many applications such as piezoelectric nanogenerators.<sup>53</sup> In this respect, it is desired to grow high quality micro/nano structures of ZnO which are free from native defects.

Figure 4 represents the RT PL spectral data for the ZnO NSs measured using an excitation wavelength of 325 nm at a wide range of photon energies. From this experimental data (Figure 4a), it can be seen that the PL spectra shows a strong UV peak centered at  $\sim 3.24$  eV. The observed UV peak is very close to the ZnO band-gap emission of  $\sim 3.37$  eV at RT. Since the UV band energy peak is close to the ZnO band gap, we refer to it as near band edge emission (NBE). It is also worth noting that the commonly observed DL emission peak in ZnO nanostructures (inset of Figure 4a), which is attributed to nonstoichiometric defects such as stacking faults, surface defects, dislocation, etc. was found to be extremely weak ( $< 0.4\%$ ) with respect to the NBE peak.

In order to study the origin of the observed UV peak, temperature dependent PL measurements were conducted on as-grown ZnO NSs. Temperature dependent PL was performed between 11 K and 300 K, in steps of  $\sim 50$ K. The resulting experimental data is shown in Figure 4b. From this data, it can be seen that UV peaks shows consistent red-shift with increasing temperature. The

inter-band emission peak follows the well-known Varshni formula, due to the temperature-induced lattice dilation and electron-lattice interactions, described by [54]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T} \quad \text{Equation (1)}$$

where  $E_g(T)$  is the band-gap at an absolute temperature  $T$ ,  $E_g(0)$  is the optical band-gap maxima at 0 K and  $\alpha$  and  $\beta$  are the Varshni thermal coefficients related to given materials. The solid fitting line, using Eq.1 to the peak NBE as a function of temperature (from 11 K to 300 K), is shown in the inset of Figure 4b. The obtained fitting parameters of  $E_g(0)$ ,  $\alpha$  and  $\beta$  are 3.32 eV,  $2.3 \times 10^{-3}$  eV/K and 1590 K, respectively, which are comparable to the values reported for ZnO nanostructures.<sup>49</sup> The near perfect fitting of the Eq. 1 to the experimentally observed values proves the excitonic origin of the NBE peak in the UV region. From an optical perspective, the presence of strong NBE UV peak with negligible peak in the visible region confirms the high crystalline quality of our ZnO NS material.

## 2.4 Electrical Characterization of ZnO NS-FETs

The electrical properties of the as-grown ZnO NSs were characterized by fabricating single ZnO NS based field-effect transistors (NS-FETs) on both rigid (Si/SiO<sub>2</sub>) and flexible (PET) substrates. For the transfer of nanomaterials, such as nanowires (NWs), precisely onto the target device substrates, various methods like drop-cast,<sup>54</sup> roll transfer printing,<sup>55</sup> Langmuir-Blodgett technique,<sup>56</sup> magnetic field alignment,<sup>57</sup> and dielectrophoresis (DEP)<sup>58</sup> have been developed. In the present work, we have used 'drop-cast' approach for the transfer of ZnO NSs, as it is inexpensive, uncomplicated and can be accomplished at room temperature. "Figure 5 shows the schematic process steps for transferring our NSs from sapphire to the solution and onto device

substrates (both rigid (Si/SiO<sub>2</sub>) and flexible (PET) substrates) (see experimental details for the description of the process).

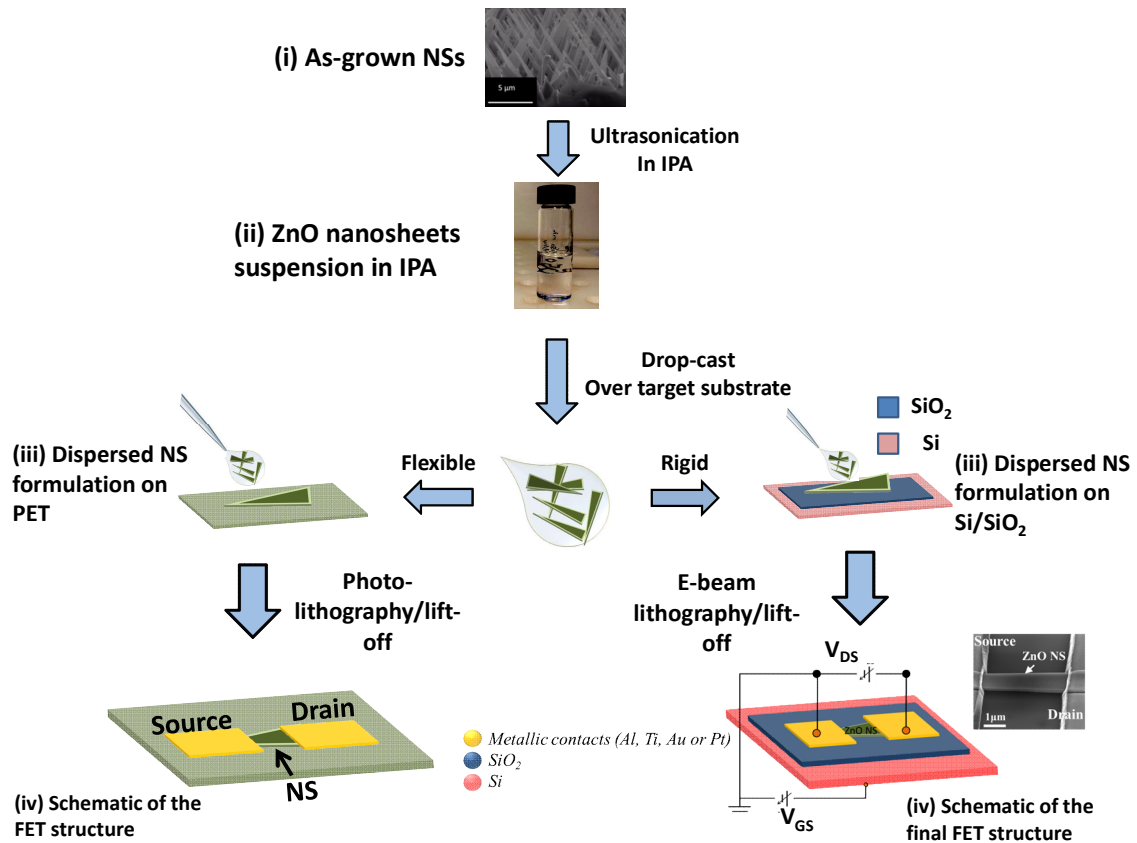


Figure 5. The process flow for the dispersion of as-grown ZnO NSs over both rigid and flexible substrates.

We first examine the ZnO NS-FETs fabricated on a p<sup>++</sup>Si/SiO<sub>2</sub> (~170 nm) substrate which are used as the back-gated NS-FETs. Figure 6 shows the schematic and optical images of a NS-FET device as well as transfer and output scan of the fabricated device. For the device under investigation, the channel length (L) and width (W) are ~5 μm and ~2.2 μm, respectively. To obtain the transfer scans, the gate-source voltage (V<sub>GS</sub>) was swept from -20 V to +5 V at a drain bias (V<sub>DS</sub>) of 1V (Figure 6(c)). The family of output scans were obtained by sweeping V<sub>DS</sub> from -10V to 10V (only positive V<sub>DS</sub> voltages shown) and V<sub>GS</sub> was incrementally stepped from -7 V to 1 V after a full sweep of V<sub>DS</sub> (Figure 6(d)). From the experimental data, it can be seen that by

increasing  $V_{GS}$  towards more positive values resulted in an increase of the drain current ( $I_{DS}$ ). This behavior of the FET device suggests an n-channel accumulation-type of operation. A linear extrapolation of  $I_{DS}$  to  $V_{GS}$  intercept revealed a negative threshold voltage ( $V_{TH}$ ) of  $\sim -4$  V, consistent with an n-channel depletion mode device. The observed increase in  $I_{DS}$  with incremental increase of  $V_{GS}$  in the output scans (Figure 6(d)) further confirms the n-channel behavior exhibited by the device. Notably, the low  $V_{DS}$  region in the output scans ( $V_{DS} \leq \sim 0.5$  V) shows a linear dependence of  $I_{DS}$  with increasing  $V_{DS}$  without any inflection point. This behavior of the device is typical of a FET operating in the linear regime with low energetic contact barriers.<sup>59</sup> This result suggests that the low work function metal Ti, used as s/d electrode, provides efficient contacts to the conduction band of the ZnO NSs for electron injection/extraction.

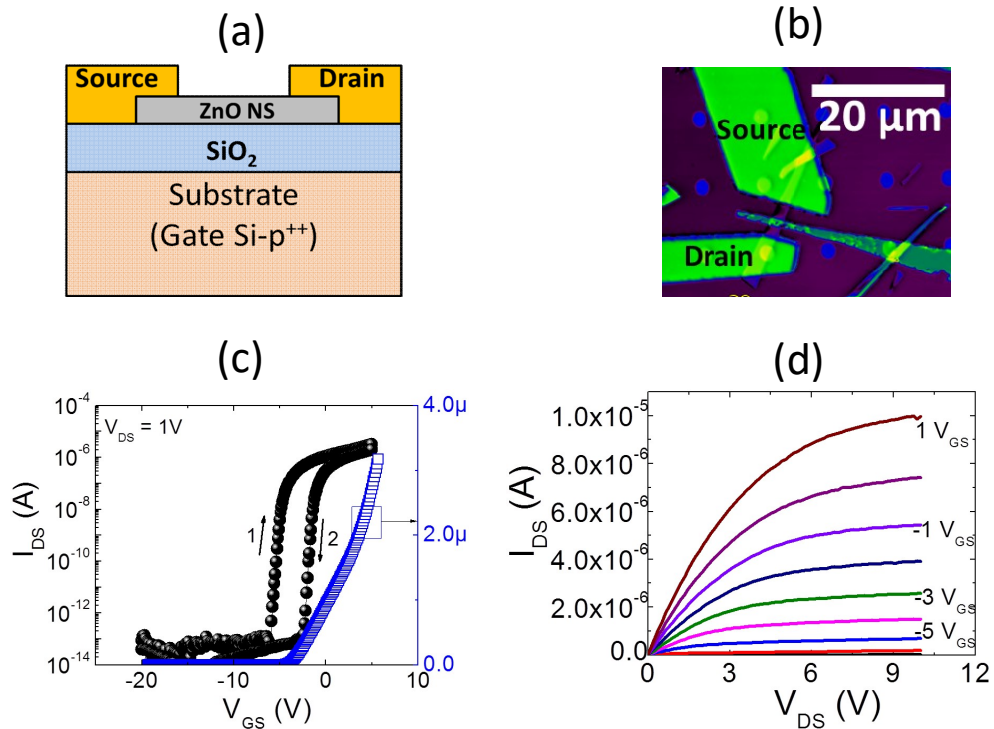


Figure 6. (a) Schematic image while (b) is optical image of the NS-FET. (c)  $I_{DS}$ - $V_{GS}$  transfer scan log and linear curves measured at  $V_{DS} = 1$  V, and (d) the corresponding  $I_{DS}$ - $V_{DS}$  output scan curves varying the gate bias from -7 to 1 V with a step of 1 V.

In terms of FET performance metrics, key parameters to consider include: on-state current ( $I_{on}$ ), off-state current ( $I_{off}$ ), current on/off ratio ( $I_{on/off}$ ), effective mobility ( $\mu_{eff}$ ), and sub-threshold slope (s-s). For this device, the logarithmic plot of the transfer scan in Figure 6(c) revealed an  $I_{on}$  ( $\sim 10 \mu A$ ) /  $I_{off}$  ( $\sim 0.1 pA$ ) current ratio of  $\sim 10^8$  suggesting an excellent gate-channel control. The s-s value has been estimated to be  $\sim 250$  mV/dec. While the obtained s-s value from our NS-FETs is larger than the ideal thermodynamic limit at room temperature (60 meV), it is still smaller than those often reported for ZnO NW-FETs.<sup>60</sup> Finally, the field-effect mobility in the device was evaluated using conventional MOSFET model in the linear regime,<sup>23,59</sup> as given by Eq.2.,

$$\mu_{FE} = \frac{L}{W} \frac{g_m}{C_{ox} V_{DS}} \quad \text{Equation (2)}$$

where  $L \sim 5 \mu m$  is the channel length,  $W \sim 2.2 \mu m$  is the average channel width,  $g_m$  is the transconductance ( $dI_{DS}/dV_{GS}$ ), and  $C_{ox} \sim 1.15 \times 10^{-4} F/m^2$  is the gate-channel capacitance expressed as  $\epsilon_0 \epsilon_r / d_{ox}$  where  $\epsilon_r = 3.9$  is  $SiO_2$  relative permittivity and  $d_{ox} \sim 170$  nm is  $SiO_2$  thickness. Using Eq. 2 and the extracted  $g_m$  value, the  $\mu_{FE}$  of this sample was estimated to be about  $100 cm^2/Vs$  at RT.

In order to investigate the performance metrics for ZnO NS-FETs, several different NS-FETs with similar Ti contacts were fabricated and measured under identical conditions. The distributions of the obtained mobility, current on/off ratio and s-s values were further extracted for the 15 NS-FETs (Figure S3, statistical data distribution of 15 ZnO NS-FET devices fabricated on Si/SiO<sub>2</sub>: (i) mobility, (ii) on/off ratio and (iii) s-s value). The statistics are summarized in Table 1. From this set of data, we found an average  $\mu_{FE}$  value of  $95 cm^2/Vs$ ,

comparable to the reported state-of-the-art data for both single-crystalline ZnO NWs<sup>60</sup> and high quality polycrystalline Li-doped ZnO thin-film devices,<sup>61</sup> employing similar bottom-gate configurations. For high performance digital applications, high current on/off ratio is desirable while maintaining a high mobility value. Single layer Graphene, with a mobility value exceeding 10000 cm<sup>2</sup>/Vs, is undoubtedly the first choice. However, the main drawback limiting the widespread use of Graphene is the material's zero band-gap. Therefore, there are very limited numbers of reports on Graphene as digital electronic material with current on/off ratio limited to 10<sup>1</sup>-10<sup>2</sup>. Jariwala and coworkers summarized the field-effect mobility and current on/off ratio values for all possible semiconductor candidate for unconventional electronics reported so far.<sup>62</sup> The initial results on ZnO NSs (Figure 5, S3 and Table 1), confirm the potential of our material for high performance digital electronics with mobility comparing to the Transition metal dichalcogenides (TMDCs) and poly-crystalline silicon while maintaining a current on/off ratio of 10<sup>7</sup>-10<sup>9</sup>, one of the best reported data for inorganic semiconductors.

In general, ZnO nanostructure based FETs can be constructed in two distinct operational modes i.e. depletion mode (D-mode) with a negative threshold voltage ( $V_{TH}$ ), and enhancement mode (E-mode) showing a positive  $V_{TH}$  <sup>63,64</sup>. Both operation modes are important and needed for electronic applications. In particular, E-mode devices are much preferred for low power application due to their superior power saving capabilities in the off-state.<sup>65,66</sup> However, D-mode NW-FETs are also useful for quantitative and scalable sensing applications.<sup>67-69</sup> Moreover, for a wide applications of NW-FETs in logic circuits, both D-mode FETs and E-mode FETs are required.<sup>70,71</sup> They can also be used as active loads in MOS technologies.<sup>70</sup> The default 'on' nature of depletion modes makes them excellent for boot-up sequences of electronic systems

also. Thus, a tight control over the threshold voltage is very important for the device applications.

It is to note that FET devices fabricated in this work (data from 15 NS-FETs), showed large variation in the threshold voltage (-9 to 5 V). We acknowledge that in the present work, we have not mastered the threshold voltage in our ZnO NS-FETs, where the value varies in between -9 to +5 V. In thin film transistors and/or nanomaterial based FETs, which work in depletion/accumulation mode,  $V_{TH}$  is influenced by many factors, such as charge density in the nanomaterial, energy bands at both s/d metal-semiconductor contact interface, dielectric/semiconductor interface quality and adsorbed species on semiconductor channel.<sup>25,72,73</sup> The carrier concentration in these NSs, can be evaluated using our NS-FET devices, using the parallel plate model giving  $n_e = Q_{tot}/qAt_{NS}$  where  $Q_{tot} = C_{ox} \times V_{TH}$  is the total charge in the channel,  $q$  is elementary charge,  $t_{NS}$  is the thickness of ZnO NS and  $A$  is the active area of the device. From this expression, we deduce the effective carrier concentration (from 15 devices) to be  $1.2 - 5 \times 10^{16} \text{ cm}^{-3}$ . The calculated carrier density proves that the as-grown ZnO NSs are moderately doped semiconductors and therefore, it does not seem to be the possible reason for negative threshold voltage. Although to investigate the exact cause of such device to device  $V_{TH}$  variation is beyond the scope of the present manuscript however, several strategies have been developed in an effort to control the  $V_{TH}$  and operation modes of ZnO based FETs. For example, Hong et al. explored a surface architecture control method to achieve both D-mode and E-mode ZnO FETs.<sup>63</sup> Besides the surface engineering of nanomaterial during the growth, the effects of post-growth treatment, on tuning the electronic properties of ZnO NWs have also been utilized to control the  $V_{TH}$  parameter in ZnO nanowire FETs. Qian et al. demonstrated a positive shift in the threshold voltage of their ZnO FETs by introducing a high Schottky barrier at the s/d electrode.<sup>72</sup>

The Schottky barrier was created by introducing MoO<sub>x</sub> thin layer at the interface of source metal electrode and ZnO channel. Park et al. reported the adjustment of the operational voltage in their ZnO FETs by treating the ZnO NWs with isopropyl alcohol (IPA).<sup>74</sup> Also both D-mode and E-mode ZnO NW-FETs were fabricated by treating the device under ozone ambient.<sup>75</sup>

No. of devices	Dielectric type	Mobility (cm <sup>2</sup> /V-s)	s-s (mV/dec)	I <sub>on</sub> /I <sub>off</sub> current ratio	V <sub>TH</sub> range (V)	Charge density (/cm <sup>3</sup> )
15	SiO <sub>2</sub>	95±20	400±150	10 <sup>7</sup> -10 <sup>9</sup>	-9 to +5	1.2-5 × 10 <sup>16</sup>

Table 1. Summary of the performance of ZnO NS-FET from 15 fabricated devices on rigid substrate.

## 2.5 Low-Hysteresis Loop in Top-Gate Flexible ZnO NS-FETs

Next, we fabricate the flexible ZnO NS-FETs by transferring the above demonstrated material technologies to flexible PET substrates. For FETs based on nanostructures, the top-gate geometry is preferred, since a top-gate electrode can wrap around the nanostructure and effectively control the charge transport in the semiconductor. Realization of top-gated configuration on flexible substrates requires a gate dielectric which can be deposited at RT. This gate dielectric should also provide a conformal coverage over the nanostructure with minimal defect density at the semiconductor / dielectric interface, and provide a large capacitance per unit area. In order to satisfy all of the above mentioned conditions, we have used parylene C as our top-gate dielectric material. The high transparency, quality, reliability and outstanding barrier to moisture combined with the advantage of RT deposition of parylene C have potential to be integrated with flexible electronics. Before implementing parylene C on flexible substrates, we

investigated a dual-gate NS-FET device on SiO<sub>2</sub>, as bottom-gate dielectric and parylene C as the top-gate dielectric. The electrical characterization results, for both top- and bottom-gated device, confirms parylene C as equally good dielectric material as that of silicon dioxide (Figure S4, transfer and output graph of a dual gated NS-FET device: (a) and (b) bottom gate using SiO<sub>2</sub> as dielectric while (c) and (d) for top gated structure using parylene C as top gate dielectric and Table S1, summary of the electrical characterization results of a dual gated NS-FET device).

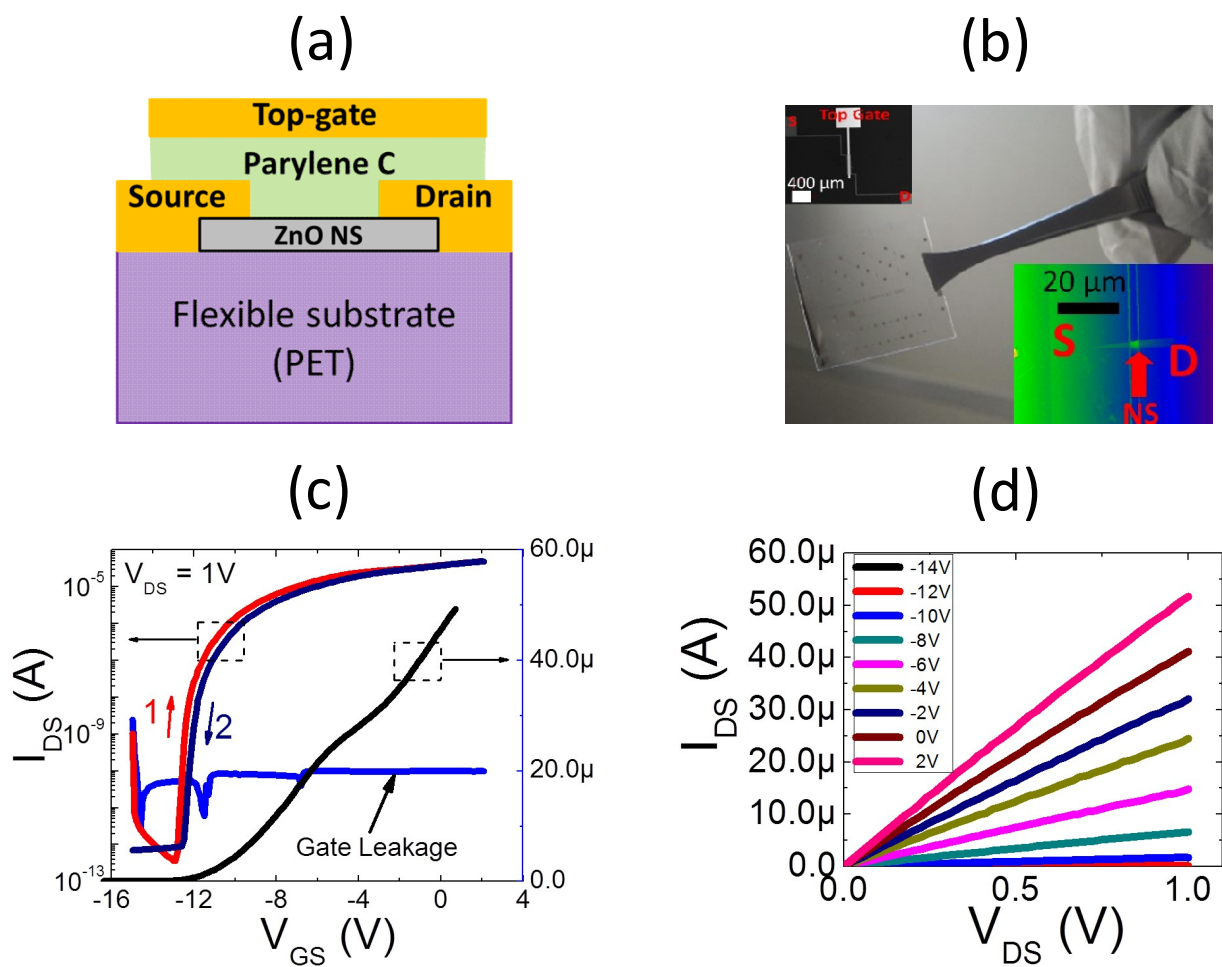


Figure 7. (a) Schematic image while (b) is optical images of the NS-FET of flexible top gated ZnO NS-FET. (c)  $I_{DS}$ - $V_{GS}$  transfer scan log curves measured at  $V_{DS} = 1$  V, and (d) the corresponding  $I_{DS}$ - $V_{DS}$  output scan curves varying the gate bias from -14 to 2 V with a step of 2 V.

The electrical characterization results of flexible ZnO NS-FETs on PET substrate with parylene C as top-gate dielectric are shown in Figure 7. Figure 7a and b shows the schematic and optical images, respectively of one of the fabricated flexible devices. The experimental transfer ( $I_{DS}$ - $V_{GS}$ ) scans at constant drain bias ( $V_{DS} = +1$  V) for  $V_{GS}$  bias range of -15 V to 2 V are shown in Figure 7c. The device showed excellent field-effect transport characteristics such as high on current ( $I_{on}$ ) of  $> 40$   $\mu$ A, high effective mobility ( $\mu_{eff}$ ) of  $>200$   $\text{cm}^2/\text{Vs}$  (taking  $C_{ox} = 1.56 \times 10^{-4}$   $\text{F}/\text{m}^2$ ), very high current on/off ratio ( $I_{on/off}$ ) of  $\sim 10^9$ , steep sub-threshold swing (s-s) of  $\sim 150$  mV/decade and low gate leakage current (100 pA). Also, negligible hysteresis is observed by scanning forward and reverse transfer scans between -15  $V_{GS}$  to +2  $V_{GS}$ . As can be seen from Figure 7d, the output characteristics showed near linear behavior below  $< 0.5$  V, confirming the formation of ohmic contacts.

Stable operation of TFTs is a prerequisite for practical device applications. For this, we assessed the stability of our devices examining transistor transfer scans at a fixed  $V_{DS}$ , whilst continuously sweeping the gate voltage between certain  $V_{GS}$  range. For bias-stress evaluation, we obtained the drain current by sweeping the gate voltage from -15 V to +4 V (forward voltage sweep) and from +4 V to -15 V (reverse voltage sweep) at fixed  $V_{DS} = 1$  V. The shift in the threshold voltage ( $\Delta V_{TH}$ ) of the device between the forward transfer scan and reverse transfer scan is called “hysteresis”. This full scan (from forward to reverse voltage sweep) is considered as one cycle of bias-stress. The value of the gate voltage sweep rate is fixed at 0.5V/sec for the entire test. Figure 8 shows results of the electrical gate-bias stress for NS-FET where the transfer scan was performed continuously up to 250 cycles/340 min. Adding one more test to the bias-stress evaluation, we have also performed transfer scan at different drain-source voltages. As can be seen from Figure 8a, the device showed consistent increase in the  $I_{on}$  with the increase of  $V_{DS}$

voltage up to 1V from 1mV with almost no shift in the on-voltage ( $V_{ON}$ , gate voltage at which drain current start to rise up). Notably, it can also be seen from this data (Figure 8b) that the device demonstrated negligible  $V_{ON}$  and  $V_{TH}$  shifts, even with prolonged measurements. Such high performance and stable electrical results showed the promise of these ZnO NS materials for the possible nanomaterial for future flexible electronics. However, as can be seen from Figure 8b, with prolonged gate-bias stress (340 min), there is an increase in the  $I_{off}$  of the device and a small decrease in the  $I_{on}$ . The decrease in the  $I_{on}$  with electric bias stress is a typical feature of an n-channel TFT with prolonged bias stress, as electrons in the channel are trapped at the immobile defect states present at the channel/dielectric interface during the bias stress. To elucidate the mechanism of trapping at semiconductor/insulator interface, important information from the transfer scans were extracted (mobility, transconductance, s-s, and hysteresis) and plotted in the Figure 8c-d.

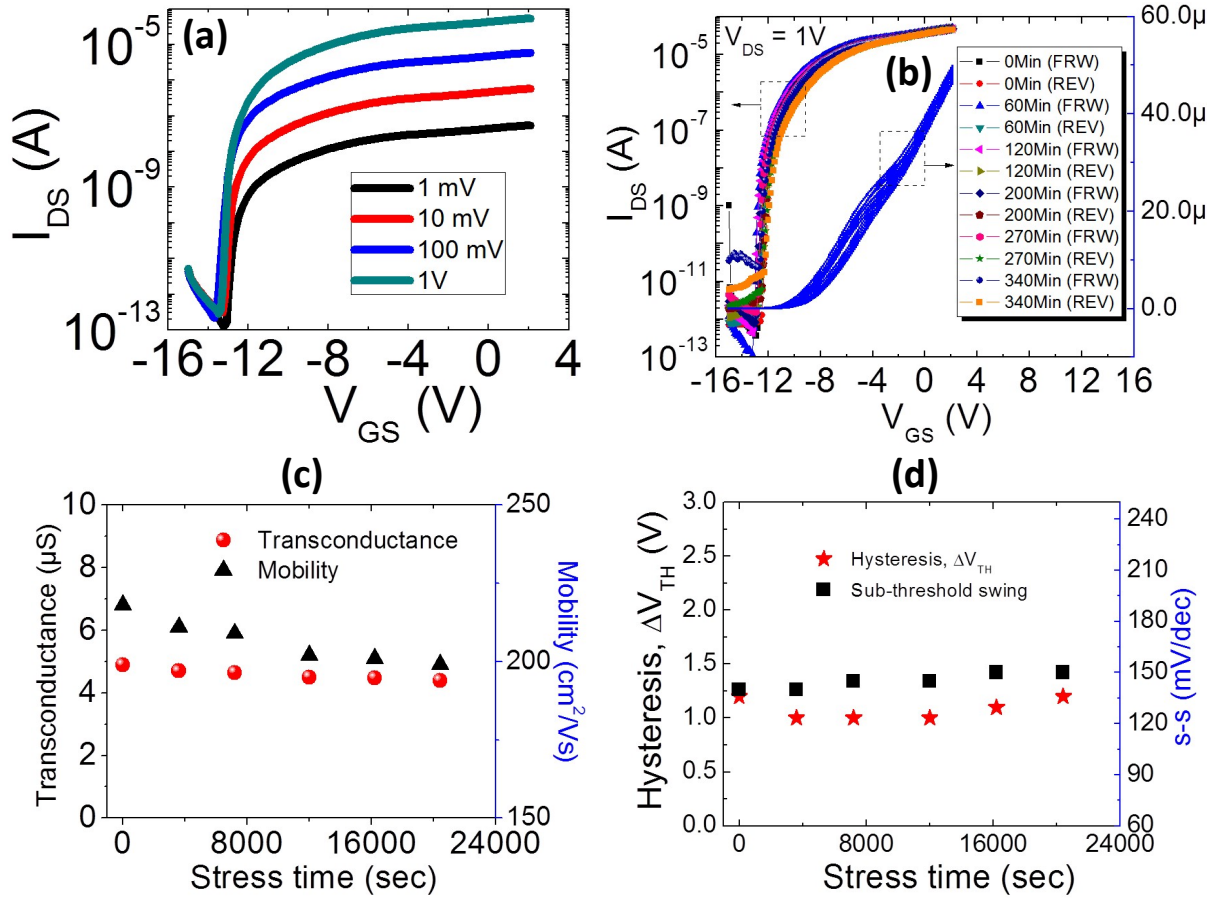


Figure 8. Electrical characterization of top-gate ZnO NS-FET device on PET substrate: (a)  $I_{DS}$ - $V_{GS}$  transfer scan log curves measured at  $V_{DS} = 0.001, 0.01, 0.1$  and  $1$  V. (b)  $I_{DS}$ - $V_{GS}$  transfer characteristics showing negligible threshold shift up to 340 min of continuous operation. (c-d) Gate bias stress evaluation as a function of measurement time: (c) transconductance and mobility, (d) hysteresis and s-s.

For the complete understanding of the underlying mechanism of the decrease in  $I_{on}$  and consequently device transconductance (Figure 8c), we have extracted the mobility, magnitude of hysteresis and s-s values with the stress time (Figure 8c-d). In general, a decrease in  $I_{on}$  during the electrical bias stress is related to charge trapping at the semiconductor/insulator interface or in the bulk of gate dielectric or semiconductor.<sup>76-78</sup> On the other hand, an increase in  $I_{on}$  is correlated with the presence of dipoles that can be oriented at the gate dielectric or charge injection from the gate electrode.<sup>76-78</sup> For n-type TFTs, the positive shift of  $V_{TH}$  with gate-bias

stress is often attributed to the charge-trapping model.<sup>79</sup> There are two charge-trapping mechanisms have been proposed in the literature for the observed threshold shift in TFTs. One of which is specific to amorphous silicon ( $\alpha$ -Si) and arises because of the motion of bonded hydrogen in the  $\alpha$ -Si channel during prolonged gate bias-stress and creates extra defect sites in the channel.<sup>80</sup> These defect sites act as a trap center for charge carriers and cause a reduction in the TFT current. The second mechanism for the shift in  $V_{TH}$  is common to all materials and is the transfer of mobile charges to immobile trapping states at the semiconductor/insulator interface or at the semiconductor / ambient interface.<sup>79</sup> Broadly, two types of traps can be present, shallow traps, responsible for the hysteresis characteristics, and deep level traps causing the strong decrease in  $I_{on}$  during continuous electrical stress.<sup>78</sup> As can be seen from Figure 8c, the transconductance of the device was stable with stress time, therefore we can conclude the type of trap are shallow in nature. Furthermore, to identify the exact source of charge-trapping, it has been shown that observing the s-s and hysteresis values, with stress time, can give an idea of the trap type, which is given by :<sup>81</sup>

$$s - s = \ln 10 \left( \frac{kT}{q} \right) \left( 1 + \frac{q}{Cox} \left( \sqrt{\frac{\epsilon_{semi} N_{bt}}{kT}} + qD_{it} \right) \right) \quad \text{Equation (3)}$$

where  $k$  is the Boltzmann's constant,  $T$  is the temperature,  $q$  is the elementary charge of electron,  $\epsilon_{semi}$  is the dielectric constant of 2D semiconductor,  $N_{bt}$  is the bulk trap density and  $D_{it}$  is the interface trap density. In the present case, we can assume  $N_{bt} = 0$ , considering only shallow trap. While an increase in s-s value signifies generation of new charge-traps at the semiconductor-oxide interface, on the other hand, a constant s-s value represents charging and discharging of preexisting traps.<sup>79</sup> As can be seen from Figure 8d, the s-s value remains constant for the entire test. The hysteresis ( $\Delta V_{TH}$ ) value has also been evaluated from the transfer scan with stress time.

As can be seen from Figure 8d, the  $\Delta V_{TH}$  value remains very stable ( $\sim 1$  V) with the stress time. This information suggests that the observed fixed  $\Delta V_{TH}$  in our devices is related to the filling of already present trap-states at the semiconductor/insulator interface. The presence of such shallow interface traps results in degradation of transconductance and effective channel mobility of the device (Figure 8c). We have also quantified the occupied trap charge density at the parylene C / ZnO NS interface using the relation<sup>81</sup>:

$$\Delta Q = \Delta V_{TH} \times C_{ox} \quad \text{Equation (4)}$$

Using the hysteresis curve, the Si-based device (Figure 6) showed  $D_{it}$  value of  $2.4 \times 10^{11} / \text{cm}^2$  ( $\Delta V_{TH} = 3.4$  V,  $C_{ox} = 1.15 \times 10^{-4}$  F/m<sup>2</sup>) whereas for the flexible NS-FETs, the  $D_{it}$  value is  $0.9 \times 10^{11} / \text{cm}^2$  ( $\Delta V_{TH} = 1$  V,  $C_{ox} = 1.56 \times 10^{-4}$  F/m<sup>2</sup>). The estimated value of  $D_{it}$ , present at the parylene C / NS interface, appeared to be less than an order of magnitude occupied at SiO<sub>2</sub> / semiconductor interface for nanomaterial based FETs in the past<sup>81,82</sup> and 2.5 times lower than compared to the device showed in Figure 6 of the present manuscript. This difference better explains the observed high stability and low hysteresis in our organic / inorganic hybrid FET devices. The experimentally observed difference in the trap charge density is explained as follows:

It is widely accepted by many researchers that the presence of surface-bound water molecules, which binds via the hydrogen bonds on the silanol groups on the silicon dioxide (SiO<sub>2</sub>) gate dielectric surface, is principally responsible for the hysteresis in carbon nanotube (CNT),<sup>83,84</sup> organic,<sup>85,86</sup> ZnO NW,<sup>22</sup> and Si NW FETs<sup>87,88</sup>. In order to remove/suppress the hysteresis phenomenon in such devices, organic dielectrics such as PMMA,<sup>83,89,20</sup> ODPA,<sup>20</sup> etc. have been used. The use of organic dielectrics to remove hysteresis has been attributed to several key

factors: (1) curing the organic material such as PMMA releases surface bound water on both the dielectric and nanomaterial surfaces that causes hysteresis, (2) the material can bond with the silanol groups on SiO<sub>2</sub>, and (3) most organic materials are hydrophobic, and both factors 2 and 3 keep water from being reabsorbed, preventing hysteresis from readily returning. In the present PET based devices, we have employed organic material parylene C as our top gate dielectric. Before the deposition of parylene C, we annealed the device at 130 °C for 1h in vacuum to remove most of the adsorbed water molecules on ZnO NS surface and then immediately transfer the device for the deposition of parylene C. This process ensures a high quality semiconductor / dielectric interface with less possibility of introducing traps which are mainly responsible for hysteresis of the device.

### **3. Conclusions**

In summary, we have demonstrated the controlled growth of single-crystalline ZnO nanosheets on r-plane sapphire surface. In-depth growth mechanism for such obliquely aligned 2D ZnO nanostructures was also presented and discussed. Using series of HRTEM images, we show that before the growth of ZnO NSs, a heteroepitaxial ZnO film is formed on the sapphire surface because of the low lattice mismatch (1.5%) between [0001] ZnO to [10-11] sapphire substrate. The formation of this ZnO film, at the base of NSs, can be related to sterically frustrated horizontal nanowire growth. The room temperature photoluminescence confirm the high optical quality of the as-grown ZnO NSs with negligible deep level emission (less than 0.4 %) compared to UV emission peak. The temperature dependent PL further confirms the excitonic nature of the observed UV peak. The material's electrical properties were first extracted by fabricating 15 NS-FETs devices over rigid Si/SiO<sub>2</sub> substrates. The obtained mobility, current on/off ratio and s-s values confirmed the high quality of the material produced. Furthermore, we have fabricated

flexible top-gated organic / inorganic hybrid ZnO NS-FETs on PET substrates using parylene C as gate dielectric at room temperature. The fabricated devices showed excellent field-effect transport characteristics ( $\mu > 200\text{cm}^2/\text{Vs}$  and  $s-s < 200\text{ mV/dec}$ ) and low gate leakage current (100 pA) at  $V_{\text{DS}} = 1\text{V}$ . Also, after device fabrication optimization, flexible ZnO NS-FET device showed negligible hysteresis at room temperature and very low threshold shift with prolonged electrical stress up to 340 min. The presence of low interface charge trap density ( $\sim 10^{11}\text{ q.cm}^2$ ) at the parylene C / NS interface explains the observed low hysteresis in our organic / inorganic hybrid FET devices. The present investigation showed the promise of these ZnO NS materials as the potential nanomaterial for future low-power flexible nanoelectronics.

## **4. Methods**

### **4.1 ZnO Nanosheet Synthesis and Structural Characterization**

The ZnO nanosheets (NSs), studied in this work, were grown inside a horizontal quartz furnace by carbothermal reduction of ZnO nanopowder on (01-12) r-plane sapphire substrates. Prior to NSs synthesis, r-plane sapphire substrates were cleaned using Piranha solution in a 1:1 mixture of sulfuric acid ( $\text{H}_2\text{SO}_4$ ) and hydrogen peroxide ( $\text{H}_2\text{O}_2$ ) for 15 min. The substrates were then coated with Au film ( $2 \pm 1\text{ nm}$ ) using electron-beam evaporation. Next, the Au-coated r-plane sapphire substrates and the source material (ZnO and C at 1:1 weight ratio) were placed on top of an Alumina ‘boat.’ This boat was inserted close to the center of furnace. During the growth process, an Ar ambient was maintained in the growth chamber, without any vacuum system. In this work, the growth temperature was fixed at  $900\text{ }^\circ\text{C}$  with a ramp rate of  $30\text{ }^\circ\text{C min}^{-1}$  up to the dwell temperature while the growth time at the plateau was 180 min. After the growth, the furnace was switched off and left to cool down naturally to room temperature. Samples were then removed from the growth chamber and characterized.

## 4.2 Morphological and structural characterizations

Results of the nanomaterial growth were characterized using several methods. First, a dual beam FEI Strata 400 focused ion beam (FIB) coupled to a scanning electron microscopy (SEM) system was used. It is equipped with a flip stage, a scanning transmission electron microscopy (STEM) detector, and an energy-dispersive X-ray spectroscopy (EDX) for sample transfer, observation, and elemental composition characterization, accordingly. Additionally, NSs lamellas were prepared using the FIB mode and then characterized in high resolution TEM mode (HRTEM), using a JEOL 2100 F operating at an accelerating voltage of 200 kV. ZnO nanostructure crystallinity was studied using X-ray diffraction (XRD) with  $\text{CuK}\alpha_1$  radiation on the high resolution parallel beam diffractometer Bruker D8 discover. The scans were performed in the  $2\theta$  range from  $20^\circ$  to  $80^\circ$  at a scanning rate of  $0.01^\circ \text{ s}^{-1}$ . Room temperature Raman spectra of as-grown ZnO nanostructures were obtained using a Renishaw Invia Reflex instrument. An excitation wavelength of 514.5 nm and a power less than 1 mW was used. A lens of 100x magnification was used to focus the laser beam and to collect the scattered light dispersed by a holographic grating with 2400 lines/mm. The diameter of the resulting laser spot was around 1  $\mu\text{m}$ . Photoluminescence (PL) was utilized to study the optical quality of the grown ZnO nanomaterials. PL measurements were performed by pumping at 1.5 mW the 325 nm line of a He-Cd laser chopped through an acousto-optic modulator at a frequency of 55Hz. The PL signal was analyzed by a single grating monochromator, detected with a Hamamatsu visible photomultiplier, and recorded with a lock-in amplifier using the acousto-optic modulator frequency as a reference. PL spectra were taken in air as well as in vacuum within a cryostat ( $\sim 10^{-6}$  mbar).

### 4.3 Single Crystal ZnO NS-FET Fabrication and Charge Transport Studies

Fabrication of ZnO NS-FET devices was done using standard electron-beam / photolithography. As shown in the Figure 5, a flow directed assembly process based on a 'drop-cast' approach was employed to transfer ZnO NSs onto the target device substrates, as it is inexpensive, uncomplicated and can be accomplished at room temperature. Following the growth of the NSs by the VLS process, substrates containing as-grown NSs were inserted into a vial filled with the desired solvent (isopropanol (IPA) in the present case). A brief agitation on a sonic bath (5-10 sec), yield sufficient release and subsequent suspension of NSs in desired solvents. The NSs-solvent formulation was transferred directly onto the various device substrates using pipette.

To define the source/drain (s/d) contacts on the single ZnO NS, 'lift-off' approach was used. Using electron beam lithography (EBL), we have fabricated single channel bottom-gate (SiO<sub>2</sub>/Si) ZnO NS-FET devices. The fabrication of NS-FETs on flexible PET substrates was done using standard industrially scalable photolithography. During the EBL process, Si/SiO<sub>2</sub> was coated with bi-layer resist based on poly- (methyl methacrylate) and (methacrylic acid) (PMMA/MA, 33 %), which is a positive e-beam resist. The exposed areas of the bi-layer of the e-beam resist were thus removed by immersion in a solution of methyl isobutyl ketone (MIBK) and IPA (1:3). In the case of flexible devices, a bi-layer positive photo resist were employed. LOR 5A was first spin coated at 4000 rpm and then baked at ~105 °C for ~10min to remove solvent residue. This was then followed by AZ 5214E coating under identical conditions followed by baking at ~100 °C/5min. An optical mask is then used to open selected regions on substrate surfaces for s/d contact metallization.

The s/d contact metallization was performed either by magnetron sputtering or electron beam evaporation  $\leq 10^{-6}$  mbar. The formation of ohmic s/d contacts for the devices was achieved using

low work-function metals such as Ti or Al. After metallization, the PMMA / photo resist mask and unwanted metal layers were stripped from the surface of the substrates using acetone. A Cascade Microtech Summit 11k with a single source measuring unit (2636A by Keithley Instruments) was used to perform current voltage measurements under dark ambient conditions.

#### **4.3.1 Organic Parylene C Gate Dielectric Deposition**

To ensure that the organic / inorganic hybrid FET devices, investigated in this work, were fully compatible with low temperature device assembly protocols, a room temperature vapor phase deposition process was chosen for the deposition of parylene C as dielectric layers. A three stage deposition system (Sublimation, Pyrolysis and Polymerization), which afforded room temperature (RT) polymerization during deposition, was used. The parylene C films were formed by vaporizing the powdered dimer over 100 °C, creating molecular changes in the gaseous dimer by thermal energy at approximately 690 °C, and polymerization on the chosen substrate at RT.

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#### ***Conflict of interest***

The authors declare that they have no conflict/competing interests.

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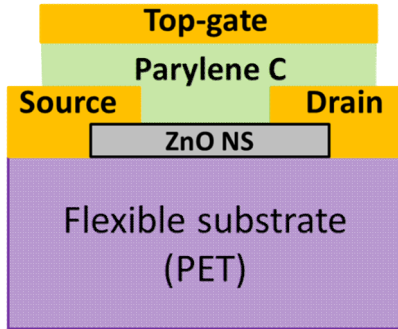
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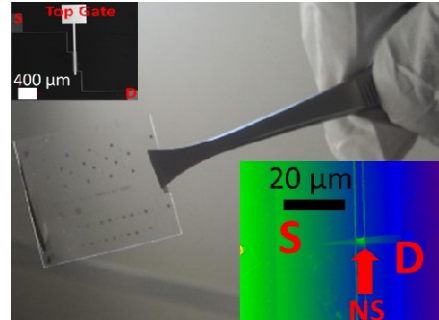
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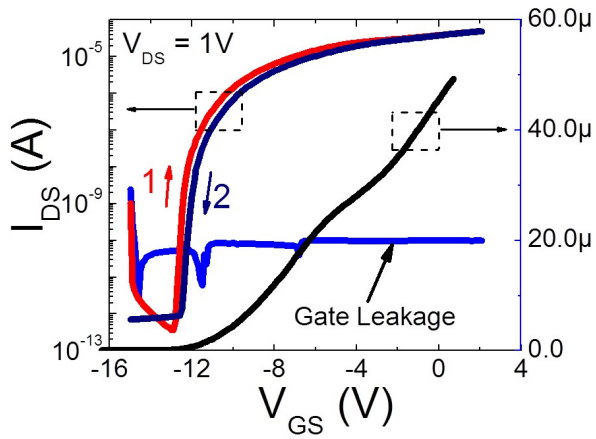
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