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25 kV-50 Hz railway power supply system emulation for Power-Hardware-in-the-Loop testings

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Caroline Stackler^{1,2*}, Nathan Evans¹, Luc Bourserie¹, François Wallart¹, Florent Morel^{1,3}, Philippe Ladoux²

¹ ITE SuperGrid Institute SAS, 23 rue Cyprien, 69100 Villeurbanne, France

² Université de Toulouse, INPT, UPS, CNRS, LAPLACE (Laboratoire Plasma et Conversion d'Énergie), ENSEEIHT, 2 rue Charles Camichel, BP 7122 F, 31071 Toulouse Cedex 7, France

³ Université de Lyon, Ecole Centrale de Lyon, Laboratoire Ampère, UMR CNRS 5005, 36 avenue Guy de Collongue, 69134 Ecully Cedex, France

* E-mail: caroline.stackler@supergrid-institute.com

Abstract: This paper presents a methodology to consider the impedance of a grid in power hardware in the loop (PHIL) experiments to validate power converter control in presence of harmonics or resonances in the network impedance. As the phenomena to emulate are in a large frequency range, the skin effect in conductors has to be taken into account. A procedure is developed to model the network. Then, the model is simplified to reduce the computation requirements and discretised for real-time implementation. The proposed method has been applied to analyse the harmonic interactions due to on-board converters running on a 25 kV-50 Hz railway infrastructure for frequencies from 0 to 5 kHz. The model is computed in Matlab-Simulink, a SpeedGoat Performance Machine and a linear power supply are used for a real time implementation. The converter under test and the test bench are presented. Some experimental results are presented, showing the feasibility and the usefulness of the proposed approach.

1 Introduction

Becoming more and more commonly used by Power Electronics R&D teams in Energy and Transportation sectors [1, 2] and for educational purposes [3], power hardware in-the-loop (PHIL) systems are deployed with the aim of testing a physical power system and its control, such as a solar panel or a power converter, within a simulation environment. The emulated system, which can be the model of a grid [4], wind turbines or converters, runs on a real-time simulation target (RTST). This RTST is interfaced with the device under test (DUT) (e.g. the actual power system) thanks to AD/DA (analogue-to-digital, digital-to-analogue) converters and power amplifiers, as illustrated in Fig. 1. The DUT includes the converter and its controller. Rapid control prototyping (RCP) softwares with automatic code generation allow the change of the parameters of the network and on-line interactions between the user and the emulated environment, hence making the test bench very flexible and realistic [5].

In the development process, PHIL experiment comes after the modelling of the system components. It allows the validation of the control principles and their implementation, taking into account computation time, sampling frequency, jitters and other parasitic and stray elements, which are difficult to include in the system level modelling. It also allows the study of the interactions between the tested power device and the environment, as transients, short-circuit... Thanks to PHIL testing, some phenomena not observable in simulation, such as instabilities, can then be studied. The benefit of this type of system is that the converter control system design can be fully tested on a scaled-down model of the power converter, with respect to converter ratings and also capital expenditure. To do that, the model of the infrastructure has to be implemented to control the amplifier supplying the mock-up of the converter, as shown in Fig. 1.

Some limits of PHIL, which have to be taken into account, come from the minimum step-time of RTST compared to the high frequency of the transient signals [6, 7], the stability issues which can appear due to the delay of each components of the system [1, 2] or the extrapolation of the results if the DUT has to be a small scale mock-up for safety or cost and time savings.

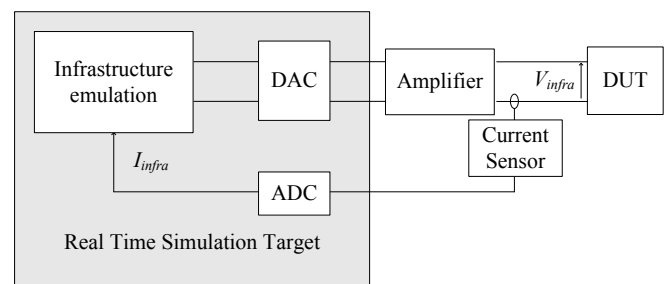


Fig. 1: Diagram of PHIL of the power supply system emulation for a small scale mock-up of on-board converter

In the field of rail transport, many research efforts are dedicated to the study of new topologies of on-board converters, such as power electronic traction transformers (PETT) [8–10]. A special care must be assigned to the interactions between the railway network and the converter. A model of the infrastructure is thus requested.

Simplified models of a railway infrastructure have already been emulated to study harmonic interactions thanks to passive components [11]. However, in this case, the parameters of the infrastructure and the train position cannot be easily modified.

In this paper, PHIL experiments are considered to emulate the power supply network. Thanks to this emulation, both the train position on the network and the geometry of the network can easily be modified. To our knowledge, no PHIL implementation of railway infrastructure has been presented in the literature.

As on-board power converters running on railway infrastructure reject harmonics into the overhead line, which can be amplified by the impedance of the overhead line [12], some overvoltages, possibly resulting in disturbances for other trains on the infrastructure or for rail signalling, can be observed. Both standards, such as the standard EN 50388 [13], and railway companies limit the tolerated level of harmonics injected into the infrastructure by on-board converters [14]. Then, while PHIL experiments are generally used

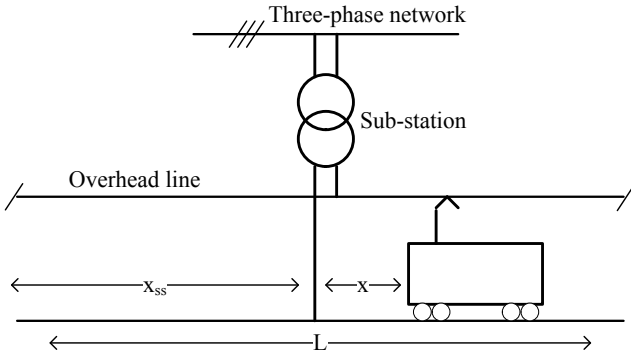


Fig. 2: Diagram of a sector of 25 kV-50 Hz infrastructure

to analyse either the stability of the network, i.e. considering only the fundamentals, or the transients, here, PHIL is used to study harmonics.

After a brief presentation of the theory used to model the 25 kV-50 Hz railway infrastructure, an electrical circuit will be introduced in section 2.2 to take into account the skin effect in the overhead line. A state space representation approach of the infrastructure will also be described. In the next section, the methodology used to emulate the infrastructure model for PHIL applications will be presented. It includes the main contributions of the paper, i.e. the process to reduce the number of states in the representation and to discretise the state space representation. Then, the methodology is applied to a small scale mock-up of an electronic transformer. The converter topology and the mock-up are presented in section 4. The last section is devoted to the results of the tests validating the theory. A conclusion and some perspectives close this paper.

2 Infrastructure modelling

2.1 State of the art

A typical 25 kV-50 Hz railway infrastructure is divided in electrically independent sectors, from 30 km to 90 km, as presented in Fig. 2, [14]. Each of them is supplied by a sub-station with single phase transformer, connected between two phases of the three-phase grid.

Lumped series inductances and resistances are generally used to roughly model both the sub-station and the three-phase grid [14–18]. Beyond some kilohertz, the wave length of the overhead line is in the same range than the length of a sector. Therefore, the overhead line is usually modelled by distributed parameters to take the propagation effects into account. The set constituted by the rails and the overhead line is then described using the multi-conductor transmission lines theory (MTL) and the Telegrapher's equations [14–18]. For frequencies under a few kilohertz, a single conductor equivalent model can be used to represent the overhead wires [15]. For higher frequencies, typically beyond 5 kHz, this hypothesis is not valid anymore due to interactions between overhead wires, rail geometry or soil conductivity.

To avoid having the complexity of hyperbolic functions of complex variables and simplify the implementation of the Telegrapher's equations, cascaded quadripoles with lumped parameters are often used to discretise the line. The length of a quadripole has to be chosen as small compared to the wave length at the maximum considered frequency, to keep a fair approximation of the propagation effects. A diagram of a line section modelled with distributed parameters and a line quadripole are presented respectively in Fig. 3 a) and b).

Applying the theory in Matlab-Simulink, the impedance seen by a train on an infrastructure has been calculated. The line parameters used for the calculation [14] are given in Table 1, and results are drawn in black in Fig. 4. The infrastructure impedance presents some resonances at characteristics frequencies.

Table 1 Overhead line and substation parameters

Overhead line per-unit-length parameters	Sub-station parameters	Lengths (x and x_{ss} refer to Fig. 2)
$r = 0.16 \Omega/km$	$R_{ss} = 1.17 \Omega$	$L = 90 km$
$l = 1.55 mH/km$	$L_{ss} = 21.2 mH$	$x_{ss} = 45 km$
$c = 7.4 nF/km$	$V_{ss} = 27.5 kV$	$x = 10 km$

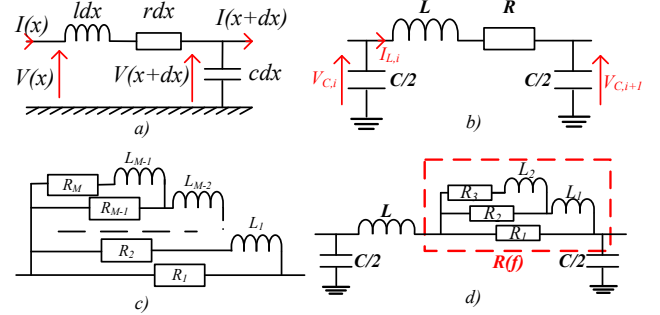


Fig. 3: a) single equivalent conductor overhead line section; b) overhead line quadripole without skin effect; c) RL ladder circuit modelling the skin effect in the time domain; d) overhead line quadripole with skin effect

2.2 Skin effect modelling

Beyond a few hundreds of hertz, the line radius, typically 5.8 mm for a copper catenary, becomes bigger than the skin depth. Therefore, the line resistance increases, which results in an attenuation of the resonances present in the infrastructure impedance, as one can see in red in Fig. 4. Moreover, the attenuation is more important when the frequency increases. Nonetheless, the resonant frequencies are independent of the skin effect.

To model the skin effect in the line in the time domain, a circuit with resistances and inductances disposed in ladder has been proposed [19, 20] for transmission lines. An example is shown on Fig. 3 c). In low frequency, the impedance of the circuit is equivalent to all the resistances in parallel. When the frequency increases, the impedance of the inductances increases too. Thus, the impedance of the i^{th} branch becomes high regarding R_{i-1} . The i^{th} branch becomes then negligible in front of the resistance of the $(i-1)^{th}$ branch. When the frequency increases, the total impedance of the ladder circuit increases from all the resistances in parallel to R_1 . If the values of resistances and inductances are well-chosen, such a circuit can be used to mimic the skin effect in the line resistance. The number of branches depends on the considered frequency range.

The RL ladder circuit can also be implemented in a line quadripole to model the skin effect in the resistance, as shown on Fig. 3 d). An optimisation, detailed in [12], has been made to calculate the values of the parameters. Finally, a three-resistance-two-inductance-ladder-circuit has been obtained as an accurate model of a quadripole resistance with skin effect up to 5 kHz. The impedance seen by a train obtained on a Matlab-Simulink, using "SimPower Systems" model with cascaded quadripoles including the skin effect RL ladder circuit is drawn in blue in Fig. 4, validating the approach.

3 Infrastructure emulation

3.1 State space representation

In order to emulate the model presented in the previous sections for PHIL applications, the state space representation of the infrastructure model is calculated in Matlab-Simulink. It takes in input the substation voltage (V_{ss}) and the current(s) drawn by the train(s) ($I_{train,i}$) and outputs the voltage(s) at the terminals of the train(s) ($V_{train,i}$) and the substation current (I_{ss}), as illustrated in Fig. 5.

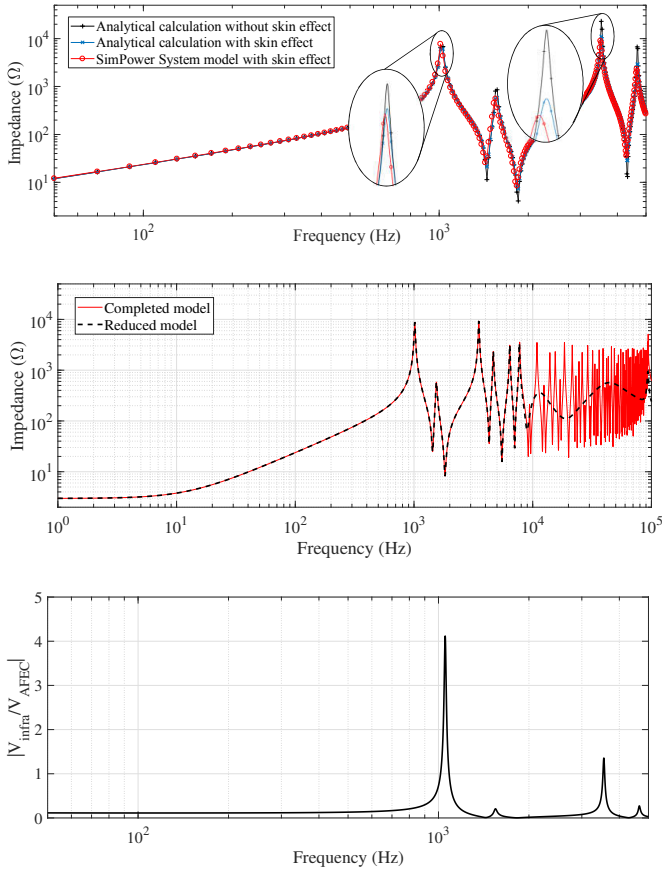


Fig. 4: Impedance seen by a train on the sector: analytical calculations and simulation in Matlab-Simulink without and with skin effect (top), complete and reduced model (middle) and ratio between the infrastructure voltage at the pantograph of a train and the voltage at the terminals of the AFEC (bottom)

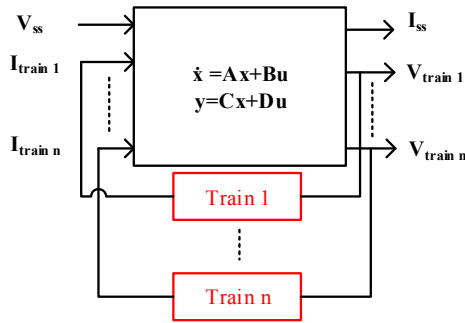


Fig. 5: Diagram of the state space representation of the infrastructure

The states of the representation are the currents in the inductances and the voltages at the terminals of the capacitors of the cascaded quadripoles.

A sector modelled with cascaded quadripoles with RL ladder circuit representing 1 km of the line, i.e. small compared to the wave length at 5 kHz, counts, typically, some hundreds of states. However, the number of operations realisable in real time by the microprocessor supporting the infrastructure model for PHIL experiments is much more limited. Thus, a methodology has been developed to drastically reduce the number of states of the representation.

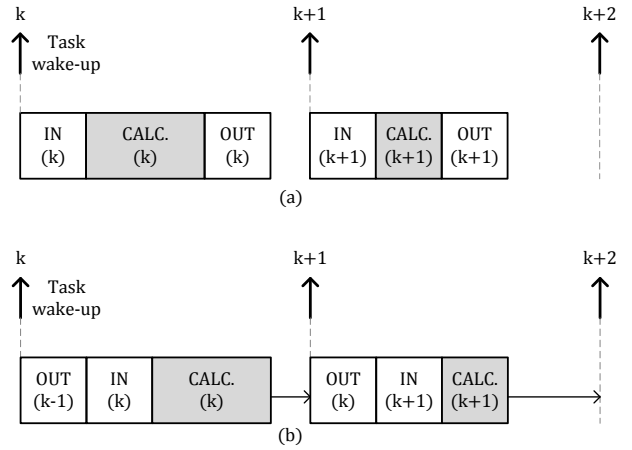


Fig. 6: Alternatives for execution order inside the task: (a): outputs updated at the end of the period; (b): outputs updated at the beginning of next period

3.2 Reduction of the number of states

To obtain a reduced model, the so called *balanced realisation* of the state space representation [21], organising the states in function of their energy, is first calculated in Matlab. Then, the states are selected in function of their observability and their controllability. That is, the states with lower observability and controllability are eliminated. Another constraint is also added on the frequency range: the states which contribute to frequencies beyond 5 kHz are removed.

Thanks to tools provided by Matlab toolbox "Control System Toolbox", this reduction is quite easily made. However, due to both the wide frequency range of the modes and the disparate values of the corresponding Gramian, characteristic of the observability and controllability of the states [21], the reduction, sometimes, results in unstable state space representations caused by numerical inaccuracies. The stability of the model has then to be verified.

With this method, for the sector whose parameters are given in Table 1, a ten-state-representation can be obtained from a state space representation with, initially, hundreds of states. The impedance seen by a train obtained with the simplified state space representation for a frequency range between 50 Hz and 5 kHz is displayed in the middle of Fig. 4.

3.3 Discretisation of the state space representation

After having reduced the number of states, the model is discretised in order to be implemented for real time applications, classically using zero-order hold on the inputs and a sample time T_s (Eq. (1)).

$$\begin{cases} X_{k+1} = FX_k + GU_k \\ Y_k = CX_k + DU_k \end{cases} \quad (1)$$

Where the inputs U_k are the substation sinusoidal voltage and the train current $[V_{ss} \ I_{train}]^t$ and the output Y_k is the voltage at the terminals of the train V_{train} . As the inputs do not have a direct impact on the output, the feed forward matrix D is equal to zero.

For the real time implementation, the execution order inside the task is a key point. Usually, a period starts by the acquisition of the inputs, then the calculations are realized and in the end, the outputs are updated (Fig. 6 (a)). The problem with this execution order is that the calculation time depends on the load of the CPU: any request that is of a higher priority for the CPU will interrupt the calculation. This leads to a jitter in the output update and the moment the outputs are updated is quite unpredictable inside the task.

To solve this problem, the outputs are chosen to be updated at the beginning of the next period (Fig. 6 (b)). The consequence of this new execution order is that a pure delay of one period appears between the inputs and the outputs. However, this delay can be easily

compensated using the discretised system as a prediction (Eq. (2)). Note that it is only possible because, in our application, the D matrix is null.

$$\begin{cases} X_{k+1} = FX_k + GU_k \\ Y_{k+1} = CX_{k+1} \end{cases} \quad (2)$$

This model will be used in PHIL with the small scale mock-up described in the next section.

4 Considered converter

4.1 Electronic transformer topology

The considered converter is one of the new topologies of PETT. This PETT structure is that of an indirect AC-DC voltage source converter, composed of modular H-bridge switching cells (Fig. 7 (a) and (b) [8–10, 22, 23]). The first stage of this topology is an active front end converter (AFEC), in reality a cascaded H-bridge structure, interfaced with the overhead line by way of an inductance.

The second stage of the power conversion is enabled by a multilevel DC-DC converter structure, with inputs isolated from one another and a parallel connection at the output i.e. the DC traction bus. Isolation from the overhead line in this structure is provided by the medium frequency transformers (MFT) seen in the AC-links of the DC-DC converter cells. This power converter topology can be operated in traction or braking mode, where the power is transmitted either in the direction of the load (traction), or from the load to the overhead line (braking).

4.2 Interleaved Pulse Width Modulation

Harmonics in the overhead line of the railway infrastructure are due to AFEC voltage harmonics generated by on-board converters. The harmonic content of the infrastructure voltage depends then on the modulation techniques used to control the AFEC.

The modulation of the cascaded H-bridges cells in the AFEC is in the form of hard-switched pulse-width modulation (PWM), whereby the points at which the carrier waveform intersects with the modulating waveform generates the duty cycle of the converter cells.

Given that there are a number of H-bridges connected in series in the AFEC, a carrier signal is required for each one of these. In order to reduce the total harmonic distortion (THD) of the AFEC voltage and thus of the input current, either phase-shifted, also called horizontally shifted PWM or vertically shifted PWM can be used to control the AFEC [24, 25]. In this type of power converter association using these modulation techniques, a multilevel voltage waveform is generated. The greater the number of levels in the voltage waveform, the closer it approximates to a sinusoid. Therefore, the quality of the waveform increases proportionally to the number of cascaded cells.

For phase-shifted PWM, the i^{th} carrier is shifted by $\frac{\pi}{N}$ regarding the $(i+1)^{th}$ carrier, where N is the number of H-bridges in the AFEC. The harmonics are thus centred on multiples of $2Nf_{AFEC}$ and, as a consequence, the THD is significantly reduced.

For vertically shifted PWM, the THD is also highly reduced. However, the harmonics are not shifted in higher frequency. Moreover, it can result in unbalances in the use of the H-bridges [24, 25].

In order to limit unbalances between the cells and push back the harmonics in higher frequency to be compliant with railway standards, phase-shifted PWM has been chosen for the converter and then for the mock-up in PHIL experiments.

5 Test bench and results

5.1 Power hardware-in-the-loop test bench

PHIL experiments have been carried out on a small scale mock-up of a 150 W converter, supplied by 50 Hz voltage up to 50 V. The

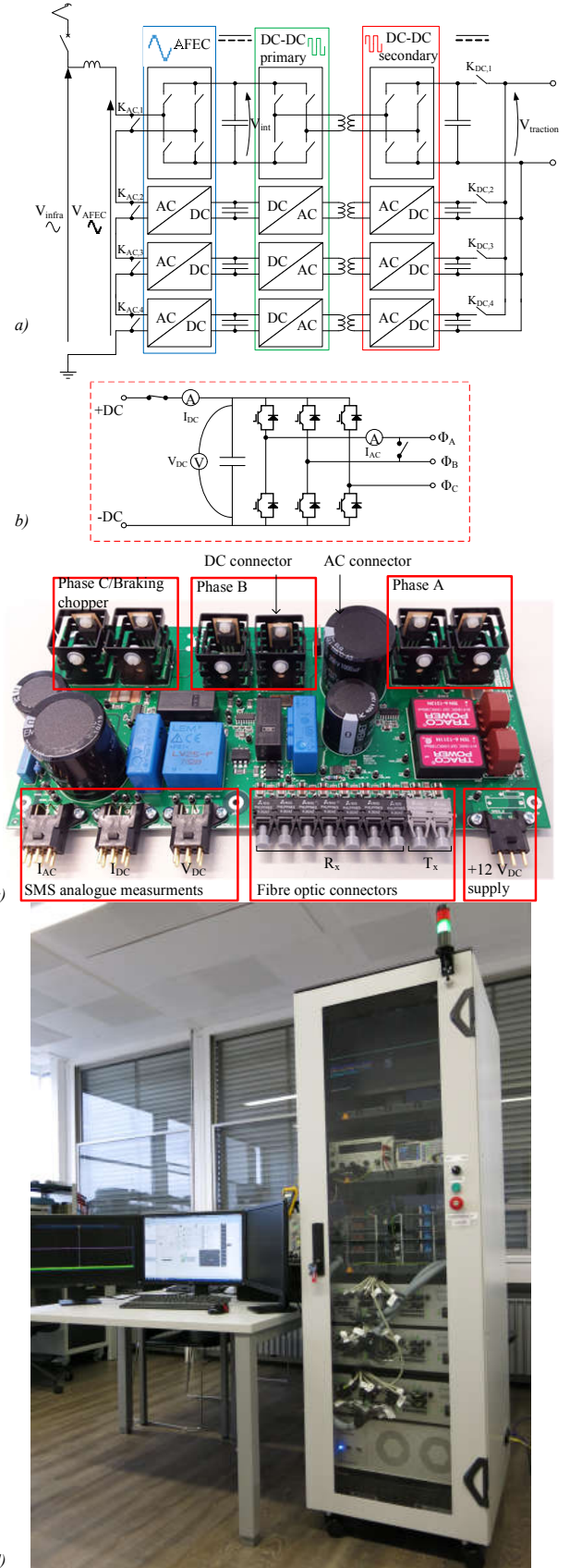


Fig. 7: The PETT converter structure is shown in (a), where each AC/DC block is constructed of H-bridge switching cells (b). The implementation of this in the PHIL circuit is by way of a modular 125 mm x 253 mm H-bridge PCB (c). The PHIL test bench is shown in (d).

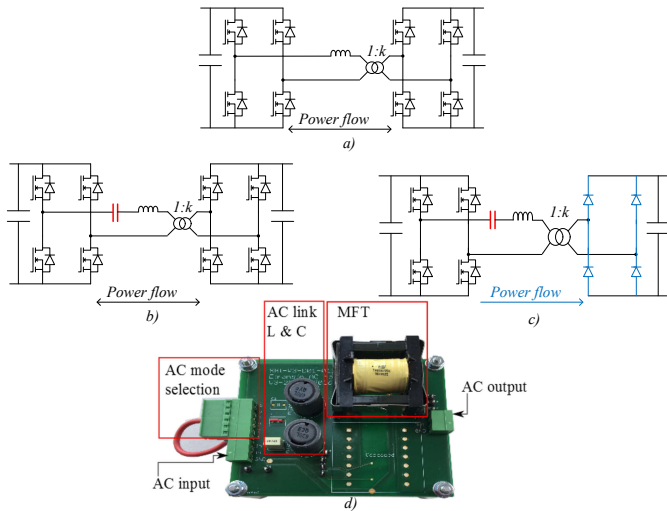


Fig. 8: DC-DC elementary cell, which can be electrically hardwired to operate in NRDAB mode (a), RDAB mode (b), or in RSAB or NRSAB mode (c). The AC-link of the DC-DC cells employ an MFT-based PCB (d)

4 cells of the AFEC switch at 450 Hz. The DC-DC cells, switching at 20 kHz, supply a 50 Ω resistive load from the intermediate 25 V buses.

The PETT topology is implemented in a PHIL circuit, housed within a 19" rack (Fig. 7 (d)). This rack contains the real-time controller, a power amplifier (AE Techron 7224), a rheostat in parallel with a current source as load and three interface boards to isolate the controller from the test circuit.

The modular H-bridge PCB (Fig. 7 (b) and (c)) adds a number of important functionalities to the PETT PHIL circuit: command and protection of the MOSFETs used within the circuit, circuit protection and reconfiguration on the DC- and AC-side of the PCB by way of electromagnetics relays, respectively $K_{DC,i}$ and $K_{AC,i}$ on Fig. 7 (a), by which a failing cell can be isolated, AC current and voltage signal measurement, DC current measurement, and the choice between either operating with a three-phase MFT or with a single-phase MFT and phase C acting as a chopper, to protect the DC capacitor against over-voltages.

The DC-DC cells in the converter structure are electrically reconfigurable, offering the choice to operate the AC-link in the cells either in non-resonant dual active bridge (NRDAB) or resonant dual active bridge (RDAB) mode, the schematics of which are shown in Fig. 8 (a) and (b), respectively [26]. This choice is hardwired by a connector on the AC-link PCB, shown in Fig. 8 (d).

The DC-DC cells in the PETT are modulated by way of phase shifting the square wave voltage of the secondary side H-bridge with respect to the square wave voltage generated by the primary bridge. This leads to a trapezoidal current waveform in the AC-link, if the NRDAB is used, or a quasi-sinusoidal AC current, if the RDAB or the RSAB are used.

Furthermore, it is possible to operate with only one of the bridges switching, with the bridge on the secondary of medium frequency transformer operating as a diode bridge rectifier. This mode of operation, which can be either non-resonant or resonant, is called non-resonant/ resonant single active bridge mode (NRSAB/ RSAB) and is configurable within the PHIL software environment.

The hardware used for the implementation is a SpeedGoat Performance Machine [27]. The discretised system is implemented in the CPU of the 3.5 GHz core i7 motherboard. The analogue input acquisition and the outputs signal generation are realized by the ADC and DAC of the IO323 board which is connected to the motherboard by a PCI express bus. The sample time is set to 40 μs ($f_s = 25 \text{ kHz}$), which is the smallest time to keep from overloading the CPU but is

enough to generate the maximum frequency of the considered signal (5 kHz).

The interface algorithm used to implement the infrastructure is the voltage-type ideal transformer model (ITM), well-known for its accuracy, and described, for example, in [28]. With this algorithm, a simulated voltage, here, the output of the state space representation modelling the railway infrastructure, is transformed by the linear amplifier to supply the mock-up converter. The current drawn by the hardware, here the PETT mock-up, is measured and fed back to the simulation.

5.2 Tests results

To illustrate the usefulness of the infrastructure model, some tests have been carried out on the small scale mock-up of the on-board converter presented in the previous section. The length of the modelled spectra, it can be seen that, as expected with phase shifted PWM, the voltage and current harmonics are centred on 3.6 kHz, when generated by the 4-cell converter and on 2.7 kHz, when generated by the converter in degraded mode (i.e. with 3 cells).

The infrastructure model has then been reduced, discretised and implemented within the controller, following the methodology presented previously, to supply the converter. Then, some tests have been carried out with the full converter, i.e. with 4 cells, and with 3 cells to depict the operation in degraded mode, i.e. as if isolating a faulty cell. First, the tests have been compared to simulations, validating the emulation methodology.

Some time-domain results of the tests are shown in traction mode Fig. 9. The corresponding spectra are displayed Fig. 10. Analysing the spectra, it can be seen that, as expected with phase shifted PWM, the voltage and current harmonics are centred on 3.6 kHz, when generated by the 4-cell converter and on 2.7 kHz, when generated by the converter in degraded mode (i.e. with 3 cells).

Moreover, it can be noticed that the harmonics in the infrastructure voltage are much higher when the converter operates with 4 cells than when it operates with 3 cells, while the magnitude of AFEC voltage harmonics is almost the same. Considering the ratio between the AFEC voltage and the infrastructure voltage at the terminals of the converter (Eq. (3)), presented on the bottom of Fig. 4, one can note an amplification at 3.5 kHz, whereas at 2.7 kHz, the ratio is much smaller than 1. Thus, the infrastructure highly amplifies the current harmonics close to 3.5 kHz, but not the ones around 2.7 kHz.

$$V_{infra} = V_{AFEC} \frac{Z_{infra}}{Z_{infra} + j\omega L} \quad (3)$$

The PHIL tests have also exposed a problem which is not observable in simulation. On some occasions, high harmonics at lower frequencies than the ones generated by the cascaded H-bridges, appears in the infrastructure voltage and current. Examples are given on Fig. 11 in full traction both in the time and frequency domains. These harmonics are independent of the power drawn by the converter. Interleaving the carriers by an angle $\frac{\pi}{N}$ cancel some harmonics. However, if the sampling are not synchronous, some interleaving problems can appear. As for each cell, the modulating signal is sampled at the switching frequency, i.e. 450 Hz, and in phase with each carrier signal. Some harmonic around 900 Hz, 1800 Hz or 2700 Hz, i.e. multiples of the switching frequency, can appear. Moreover, the ratio between the AFEC voltage and the infrastructure voltage at the terminals of the train is high at 1 kHz, as shown on the bottom of Fig. 4. Thus, the harmonics rejected around 900 Hz are highly amplified by the infrastructure. To avoid the interleaving quandary, the modulating signal should be sampled once for the modulation of every cell. Besides, either the measurement or the control could be filtered to eliminate potential harmonics disturbing the modulating signal. These tests highlight the interest of emulating network resonances in PHIL. Indeed, simulation, alone, cannot reveal such problem.

In addition, implementing a simulation within PHIL can lead to instabilities, even if the initial simulation is stable [28]. Even though, the time delay induced by the discretisation of the state space representation has been compensated thanks to (2), the stability of

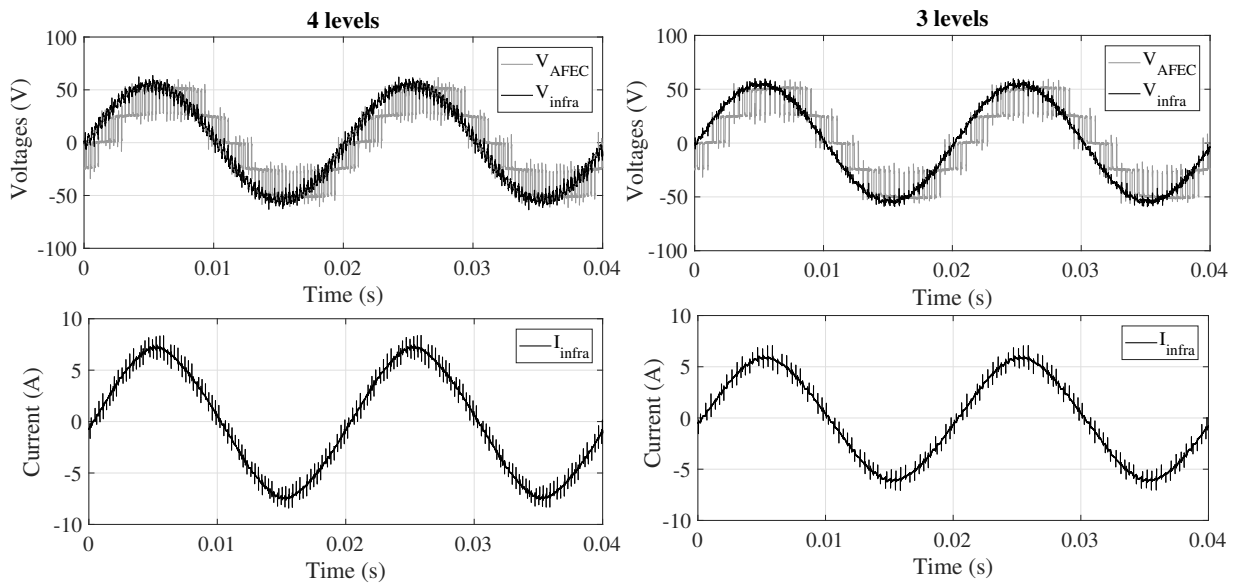


Fig. 9: Input voltages (top) and current (bottom) in the time domain, in full traction mode, of the small scale mock-up operating with 4 cells (left) and in degraded mode, i.e. with 3 cells (right)

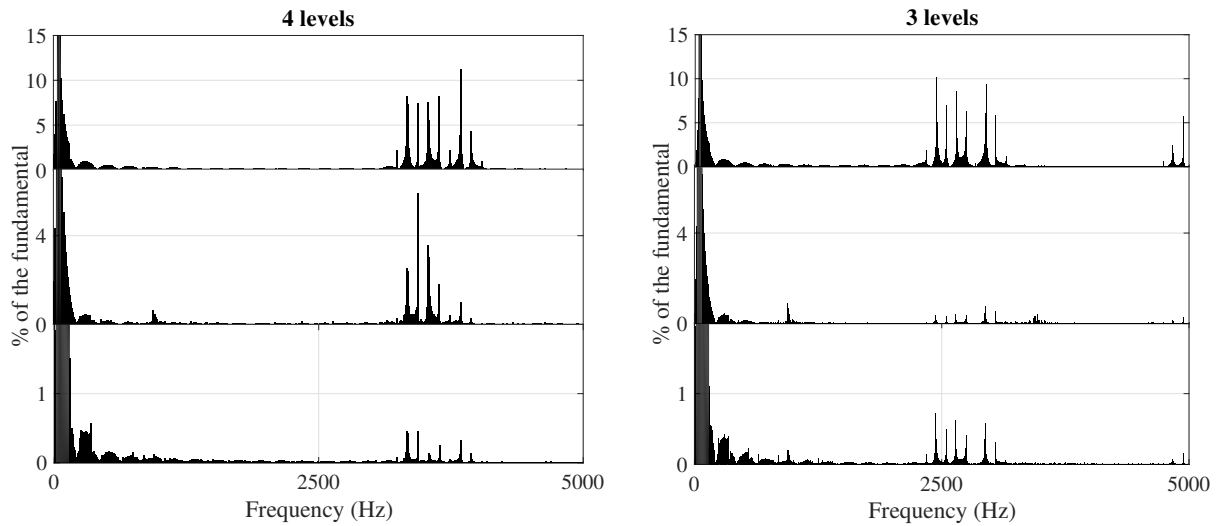


Fig. 10: Spectra of the AFEC voltage (top), infrastructure voltage (middle) and current (bottom) in full traction mode, of the small scale mock-up operating with 4 cells (left) and in degraded mode, i.e. with 3 cells (right)

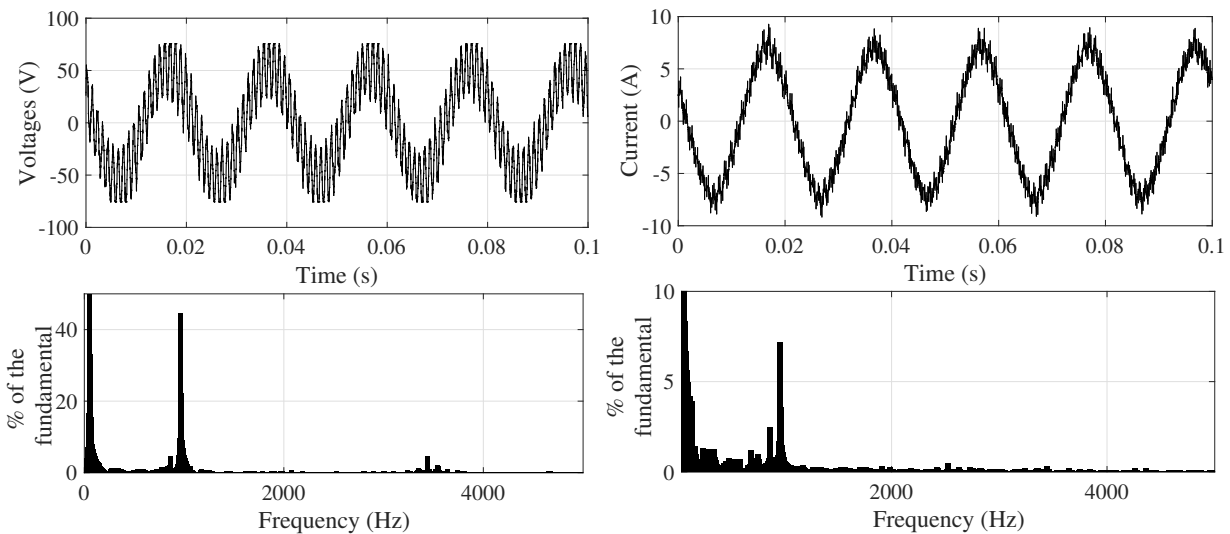


Fig. 11: Infrastructure voltage (left) and current (right) in the time domain (top) and in the frequency domain (bottom) obtained with harmonic amplifications due to the control, on the 4-cell mock-up in full traction

the system could probably be improved by using another interface algorithm, more suitable to non-linear converters.

6 Conclusion

A methodology to consider the amplification, in grids, of harmonics rejected by power converters in PHIL experiments has been presented. Its application for 25 kV-50 Hz railway infrastructure has been detailed. An equivalent circuit, composed by resistances and inductances disposed in ladder has been proposed to model the skin effect in the overhead line. A new method based on the state space representation of the infrastructure, the reduction of the number of states and the discretisation have also been introduced for PHIL applications. Then, an example of a 150 W mock-up of a multilevel electronic transformer supplied by the emulated infrastructure model has been presented. Some test results illustrate the interactions between an on-board converter, controlled by multilevel PWM and the railway infrastructure. It has been especially shown that, the amplification, in the infrastructure, of harmonics generated by on-board converters highly depends on the infrastructure sector geometry and the converter characteristics, such as the switching frequency and the number of cells. Moreover, some interleaving problems, caused by the PHIL implementation process, have been highlighted.

7 Outlooks

The infrastructure model presented in this paper is only valid up to a few kiloHertz. Indeed, beyond that, the skin and proximity effects in the sub-station transformer are not negligible and, a priori, highly impact the infrastructure impedance. The model can be further improved by using the ladder circuit modelling the skin effect to take this phenomenon into account in the transformer.

Moreover, electronic transformer controlled by phase shifted PWM are expected to reject harmonics at higher frequency. Thus, the model should be extended to comply with the converter frequency range.

The PHIL experiments can also be improved by adding virtual trains on the infrastructure. Thus, harmonic interactions between several trains running on a same infrastructure sector can be analysed.

This methodology, developed to emulate a railway grid for PHIL experiments, can also be applied to study other types of networks, such as three-phase network or offshore wind farm collector. Thus, the control of a power converter in a grid or the interactions between them can be experimented in PHIL. However, the stability of the PHIL should be improved, for example by using another interface algorithm such as the damping impedance method [28].

8 Acknowledgments

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9 References

- 1 'RTDS Technologies website', Available at <https://www.rtds.com/>, accessed 27 February 2018
- 2 'OPAL-RT Technologies: Power Hardware in the Loop - A revolution in the industry', Available at <https://www.opal-rt.com/power-hardware-in-the-loop/>, accessed 27 February 2018
- 3 Mahmoudi, H., Aleenejad, M., Ahmadi, R.: 'Reconfigurable rapid prototyping platform for power electronic circuits and systems for research and educational purposes'. IET Power Electronics, 2018, vol. 11, pp 1314-1320
- 4 Zhang, S., Liu, B., Zheng, S. *et al.*: 'Development of a Converter-Based Transmission Line Emulator with Three-Phase Short-Circuit Fault Emulation Capability', IEEE Transactions on Power Electronics, 2018, vol. 33, pp 10215 - 10228
- 5 Bélanger, J., Venne, P., Paquin, J.-N.: 'The what, where and why of real-time simulation', IEEE PES General Meeting, Minneapolis, USA, July 2010, pp. 25-29
- 6 Martinez-Velasco, J. A.: 'Transient Analysis of power systems, solution techniques, tools and applications', (Wiley-IEEE Press, USA, 1st edn. 2015)

- 7 Faruque, O. M. D., Strasser, T., Lauss, G., *et al.*: 'Real-Time Simulation Technologies for Power Systems Design, Testing, and Analysis', IEEE Power and Energy Technology Systems Journal, June 2015, vol. 2, pp. 63-73
- 8 Dujic, D., Kieferndorf, F., Canales, F., *et al.*: 'Power electronic traction transformer technology'. Proc. Int. Conf. Power Electronics and Motion Control Conference (IPEMC), Harbin, China, June 2012, pp.636-642
- 9 Farnesi, S., Marchesoni, M., Vaccaro, L.: 'Advances in locomotive Power Electronic systems directly fed through AC lines'. Proc. Int. Conf. International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM), Anacapri, Italy, June 2016, pp. 657-664
- 10 Feng, J., Chu, W. Q., Zhang, Z., *et al.*: 'Power Electronic Transformer Based Railway Traction Systems: Challenges and Opportunities'. IEEE Journal of Emerging and Selected Topics in Power Electronics, 2017, 5, (2), pp 1237-1253
- 11 Hu, H., Tao, H., Blaabjerg, F. *et al.*: 'Train-Network Interactions and Stability Evaluation in High-Speed Railways-Part I: Phenomena and Modeling', IEEE Transactions on Power Electronics, 2018, vol. 33, pp. 4627-4642
- 12 Stackler, C., Morel, F., Ladoux, P., *et al.*: '25 kV-50 Hz railway supply modelling for medium frequencies (0 - 5 kHz)'. Proc. Int. Conf. Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles International Transportation Electrification Conference (ESARS-ITEC), Toulouse, France, November 2016, pp. 1-6
- 13 EN 50388: 'Railway Applications. Power supply and rolling stock. Technical criteria for the coordination between power supply (substation) and rolling stock to achieve interoperability.', 2012
- 14 Suarez, J.: 'Etude et modélisation des interactions électriques entre les engins et les installations fixes de traction électrique 25 kV-50 Hz'. PhD thesis, INP Toulouse, 2014
- 15 Ferrari, P., Pozzobon, P.: 'Railway lines models for impedance evaluation'. Proc. Int. Conf. Harmonics and Quality of Power Proceedings, Athens, Greece, October 1998, pp 641-646
- 16 Frugier, D., Ladoux, P.: 'Voltage disturbances on 25 kV-50 Hz railway lines - Modelling method and analysis'. Proc. Int. Conf. Power Electronics Electrical Drives Automation and Motion (SPEEDAM), Pisa, Italy, June 2010, pp 1080-1085
- 17 Holtz, J., Klein, H. J.: 'The propagation of harmonic currents generated by inverter-fed locomotives in the distributed overhead supply system'. IEEE Transactions on Power Electronics, 1989, 4, (2), pp 168-174
- 18 Paul, C. R.: 'Analysis of multiconductor transmission lines' (John Wiley & Sons, USA, 1994, 2nd edn 2007)
- 19 Sen, B. K., Wheeler, R. L.: 'Skin effects models for transmission line structures using generic SPICE circuit simulators'. Proc. Int. Conf. Electrical Performance of Electronic Packaging, West Point New York, USA, October 1998, pp 128-131
- 20 Yen, C.-S., Fazarinc, Z., Wheeler, R. L.: 'Time-domain skin-effect model for transient analysis of lossy transmission lines'. Proc. Int. IEEE, 1982, 70, (7), pp 750-757
- 21 Ogata, K., 'Modern Control Engineering', Pearson, USA, 2010
- 22 Evans, N., Lagier, T., Perreira, A.: 'A preliminary loss comparison of solid-state transformer technology in rail application employing Silicon Carbide (SiC) MOSFET switches', Proc. Int. Conf. PEMD Glasgow, UK, 2016
- 23 Steiner, M., Reinlod, H.: 'Medium frequency topology in railway applications'. Proc. Int. Conf. Power electronics and applications, Aalborg, Denmark, September 2007, pp 1-10
- 24 Angulo, M., Lezana, P., Kouro, S., *et al.*: 'Level-shifted PWM for Cascaded Multilevel Inverters with Even Power Distribution'. Proc. Int. Conf. Power Electronics Specialists Conference (PESC), Orlando, USA, June 2007, pp 2373-2378
- 25 Aspalli, M. S., Wamanrao, A.: 'Sinusoidal pulse width modulation (SPWM) with variable carrier synchronization for multilevel inverter controllers'. Proc. Int. Conf. Control, Automation, Communication and Energy Conservation (INCAEC), Perundurai, India, June 2009, pp 1-6
- 26 Krismer, F.: 'Modeling and optimization of bidirectional dual active bridge DC-DC converter topologies'. PhD Thesis, ETH Zürich, 2010
- 27 'SpeedGoat website: Real-time simulation and testing', Available at <https://www.speedgoat.com>, accessed 27 February 2018
- 28 Ren, W., Steurer, M., Baldwin, T.L.: 'Improve the Stability and the Accuracy of Power Hardware-in-the-Loop Simulation by Selecting Appropriate Interface Algorithms'. IEEE Transactions on Industry Applications, July 2008, vol. 44, pp 1286-1294