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# dc and low frequency noise analysis of Fowler–Nordheim stress of *n*-channel metal-oxide semiconductor field-effect transistors processed in a 65 nm technology\*

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The authors studied the degradation of metal-oxide semiconductor field effect transistors with 5 nm oxide thickness under Fowler–Nordheim (FN) stress. In order to study the generated damage in the oxide, they have analyzed the dc characteristics and low frequency noise. The FN stress induces no significant increase in  $1/f$  noise. At the same time random telegraph signal (RTS) noise is also observed, and its amplitude associated with the drain current is investigated. The failure of the RTS amplitude model assumes that this noise is related to a conductive path. © 2009 American Vacuum Society. [DOI: 10.1116/1.3130166]

## I. INTRODUCTION

The Fowler–Nordheim (FN) tunneling has been widely used for programming and erasing memory cells in electrically-erasable programmable read-only memory (EEPROM). It has been found that the high electrical field in this regime induces the gradual degradation of the oxide properties such as oxide charge and interface trap generation, which causes the shift of threshold voltage and the degradation of transconductance.<sup>1</sup> Low frequency noise (LFN) is well known to be a very sensitive characterization tool for probing slow oxide traps,<sup>2</sup> and should therefore be an accurate method for characterizing the oxide degradation phenomena.

The aim of this study is to investigate the impact of FN degradation on drain low frequency noise behavior. Firstly, dc characterization is performed and the evolutions of  $I_D$ - $V_G$  are analyzed as a function of time-dependent stress. Then, noise measurements have been performed and discussed before and after FN stress. The deduced degradations are compared to those obtained in the case of hot carrier (HC) effects.<sup>3</sup>

## II. EXPERIMENTAL DETAILS

Throughout this work, we used *n*-channel metal-oxide-semiconductor (NMOS) transistors obtained from a 65 nm complementary-MOS (CMOS) technology fabricated on 300 mm diameter silicon wafers. The oxide is obtained by rapid thermal nitridation process, which means that nitrogen atoms are incorporated in the pure silicon oxide ( $\text{SiO}_2$ ) by thermal diffusion. The detailed device fabrication can be found in Ref. 4. The N-profile obtained in the oxide layer is reported in Ref. 5. However, the growth of oxide is carried out for longer than in the original process in order to obtain

an oxide thickness of 5 nm. The transistors have individual drain electrodes, while the gate, source, and bulk terminals are shared among several devices of different dimensions. The tested devices are of the dimensions  $W=5 \mu\text{m}$ ,  $L=0.3 \mu\text{m}$ , and  $t_{\text{ox}}=5 \text{ nm}$ .

A complete current-voltage characterization using an Agilent 4156C semiconductor parameter analyzer was performed before carrying out noise measurements. LFN measurements were performed using a HP89410A dynamic signal analyzer loaded with a high sensitivity current/voltage converter EG&G 5182.

The devices are stressed in the FN tunneling regime as function of time up to 210 s with  $V_{\text{GS}}=4 \text{ V}$  and with all other terminals tied to ground. In these conditions, the degradation of the oxide is uniform along the channel. After each stress cycle, we monitored the drain current and its flicker noise. The described behavior was reproducibly found in all the samples tested.

## III. RESULTS AND DISCUSSIONS

### A. dc characterization

We have reported in Fig. 1 the transfer characteristics before and after FN stress as a function of the stress time, and as inset  $\Delta V_T$  versus stress time. We clearly observe a shift of the threshold voltage toward higher gate voltage values, while the subthreshold slope is not significantly affected. This signifies that the density of created interface states is negligible.

According to the analytical expression of the threshold voltage [Eq. (1)], the threshold voltage shift is mainly due to the generation of fixed oxide traps during the stress cycle,

$$\Delta V_T = - \frac{\Delta Q_{\text{it}}(2\phi_f) + \Delta Q_{\text{ot}}}{C_{\text{ox}}} \approx \frac{\Delta Q_{\text{ot}}}{C_{\text{ox}}}, \quad (1)$$

where  $C_{\text{ox}}$  is the oxide capacitance per unit area,  $\Delta Q_{\text{it}}$  is the

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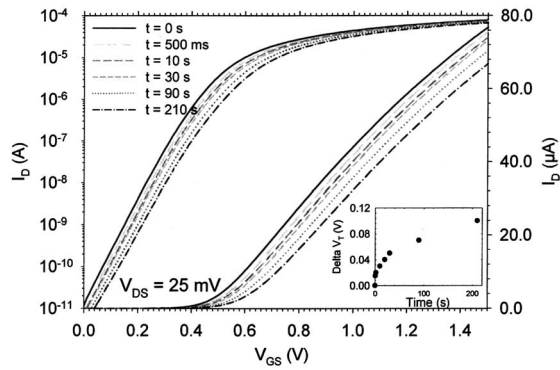


FIG. 1.  $I_D$ - $V_{GS}$  of  $n$ MOSFET subject to Fowler–Nordheim stress at  $V_{DS}=4$  V as a function of stress time inset  $\Delta VT$  vs stress time.

generated interface state density, and  $\Delta Q_{ot}$  is the generated fixed oxide trap density.

## B. Low frequency noise investigation

The drain current noise characteristics were investigated at low drain voltage  $V_{DS}=25$  mV and with  $V_{GS}$  varying from 0.3 to 1 V, before and after FN stress. We have reported on Fig. 2 the evolution of PSD before and after FN stress. We note that for unstressed devices, only  $1/f$  noise is observed, whereas for stressed devices, some Lorentzian components appear.

### 1. RTS noise

In order to identify the origin of the Lorentzian shape, we have investigated the drain current at a fixed drain and gate bias as a function of time. The drain current exhibits a discrete switching between two levels in time domain (Fig. 3). Such fluctuations are known as random telegraph signal (RTS) which gives the Lorentzian component in the frequency domain. The RTS noise is generally generated through the capture and emission of a single electron to and from an individual defect located in the oxide close to Si/SiO<sub>2</sub> interface or by a scattering center in the vicinity of the inversion layer of the device.<sup>6</sup> In the literature, several

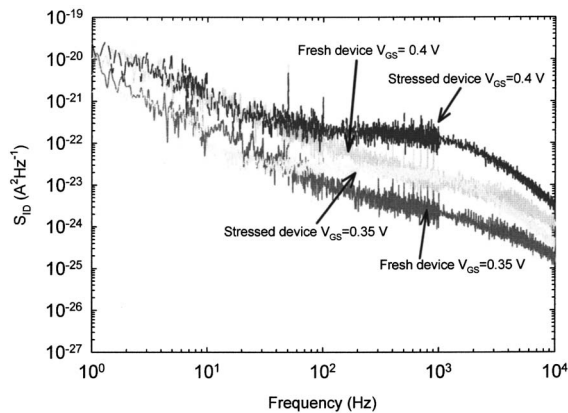


FIG. 2. Drain current noise measurements of  $n$ MOSFET on fresh and stressed devices subjected to Fowler–Nordheim tunneling at  $V_{GS}=4$  V during 90 s.

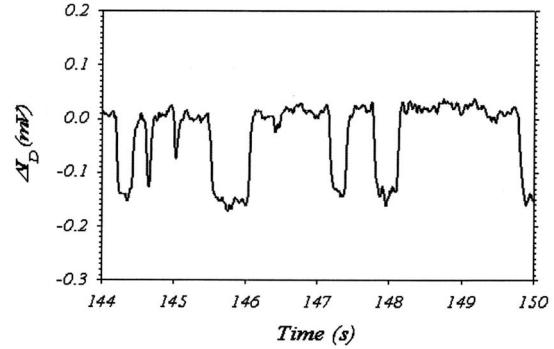


FIG. 3. RTS fluctuations in drain current after Fowler–Nordheim stress for  $V_{GS}=0.3$  V.

methods describe the extraction of trap activation range values, their maxima of activation, and the trap positions in the oxide. Generally RTS noise is observed only for devices with a gate area smaller than  $1 \mu\text{m}^2$ , whereas our devices have a gate area of  $1.5 \mu\text{m}^2$ . The main physical model proposed to explain the origin of the switching events is based on localized conductivity fluctuations of the channel.<sup>7</sup> Using the concept of flatband voltage fluctuations, the flatband fluctuation induced by the capture of single electron is given by

$$\delta V_{FB} = \frac{q}{\Delta x \Delta z C_{ox}} \cdot \left[ 1 - \frac{x_t}{t_{ox}} \right], \quad (2)$$

where  $t_{ox}$  is the oxide thickness,  $x_t$  is the trap position in the oxide from the Si/SiO<sub>2</sub> interface, and  $\Delta x \Delta z$  is the elementary surface area.

The fluctuation of the drain current  $\Delta I_D$  can be expressed as

$$\Delta I_D = g_m \frac{q}{WLC_{ox}} K \cdot \left[ 1 - \frac{x_t}{t_{ox}} \right], \quad (3)$$

where  $g_m$  is the transconductance of the device and  $WL$  is the gate area. Taking into account Eq. (3), we have calculated drain current fluctuations assuming that  $x_t \ll t_{ox}$ . The calculated results are then compared to experimental data in Fig. 4. We observe that the experimental and theoretical results follow the same slope, but the model underestimates the

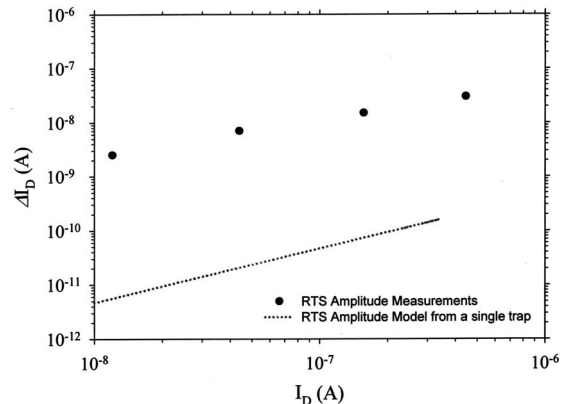


FIG. 4. Drain current fluctuations  $\Delta I_D$  vs drain current.

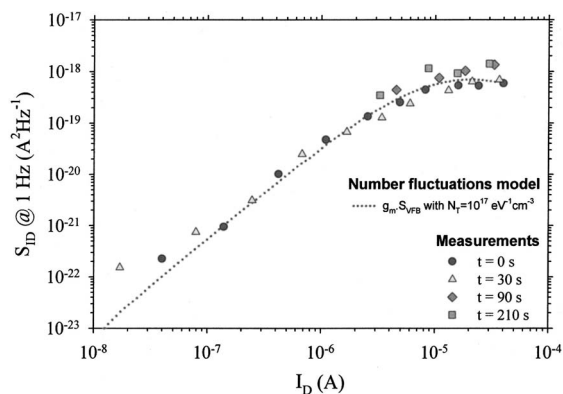


FIG. 5.  $1/f$  noise level at 1 Hz vs  $I_D$  before and after FN stress measured at  $V_{DS}=25$  mV.

value of RTS amplitude. The failure of the model suggests that the origin of RTS noise is not related to the activity of a single trap. The high value  $\Delta I_D$  as observed in Fig. 4 can be explained by the capture and emission of a single electron by a slow oxide trap close to conductive path. RTS noise has already been observed in large geometry transistors after FN stress and a similar model has already been proposed by Briere *et al.*<sup>8</sup> From statistical considerations, however, the probability that the active trap is not part of the breakdown path, but merely a trap which is coincidentally near conductive path, is very small. This implies that the traps causing RTS constitute the conductive path.

## 2. $1/f$ noise

In this section, the impact of FN stress on  $1/f$  noise is studied. We have reported in Fig. 5  $1/f$  noise levels versus drain current before and after stress at  $V_{DS}=25$  mV and  $V_{GS}$  varying. No significant rise of the  $1/f$  noise magnitude is observed after FN stress. In the subthreshold regime, we observe a quadratic variation followed by a plateau in the Ohmic regime. This behavior can be explained by the number fluctuation model ( $\Delta N$  model).<sup>9</sup> From this, we extracted a slow oxide trap density of around  $10^{17}$  eV<sup>-1</sup> cm<sup>-3</sup>. This value is independent of the stress time. This suggests that the created oxide traps responsible for the threshold voltage shift are not involved in  $1/f$  noise mechanism. These results agree with those published by Ren *et al.*<sup>10</sup> They have reported that oxide nitridation suppresses the interface trap creation and strongly limit the  $1/f$  noise degradation. According to DiMaria *et al.*,<sup>11</sup> hole trapping and H<sup>+</sup> migration are important for oxide and interface trap creation. In the case of positive FN injection, hole/H<sup>+</sup> can be generated by high energy tail hot electrons close to the poly-Si/SiO<sub>2</sub> interface and migrate inside the oxide to SiO<sub>2</sub>/Si interface. When the mobile hole/H<sup>+</sup> recombine with the injected electrons, defects are produced. In the case of our devices, the nitrated oxide layers formed a poly-Si/SiO<sub>2</sub> interface act as barrier with respect to moving species such holes and H<sup>+</sup>.

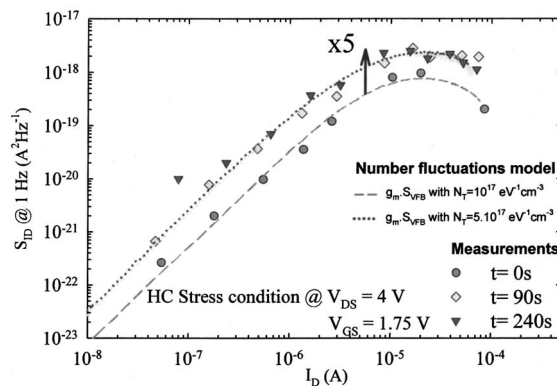


FIG. 6.  $1/f$  noise level at 1 Hz vs  $I_D$  before and after HC stress measured at  $V_{DS}=25$  mV (Ref. 3).

These behaviors differ from those observed during HC stress. We have previously published<sup>3</sup> the results reported in Fig. 6, showing that the HC stress increases the  $1/f$  noise level. It was shown that the oxide traps are created close to the drain for short stress periods and spread throughout the channel for long stress periods.

## IV. CONCLUSION

dc characteristics and LFN measurements have been performed on stressed devices in order to evaluate oxide degradation. We observe a threshold voltage variation correlated to the creation of fixed oxide traps. Concerning LFN, we observe the apparition of RTS noise after stress despite the large area of the gate. The model of drain current fluctuation  $\Delta I_D$  does not agree with experimental data, in particular. The failure of the RTS model leads us to conclude that this RTS noise is attributed to a conductive path dominated by a single trap. In contrast, no significant rise of  $1/f$  noise is observed. This is due to the nitrated oxide layer above the gate which strongly reduces the migration of holes and H<sup>+</sup> under FN stress, and hence avoids the increase of  $1/f$  noise.

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