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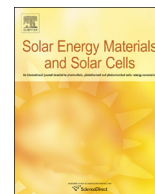
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Influence of plasma process on III-V/Ge multijunction solar cell via etching

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ABSTRACT

In this paper, the impact of the plasma process for III-V/Ge heterostructure etching on both the morphology and the photovoltaic performance is investigated for the fabrication of multijunction solar cells with a through cell via contact architecture. Three different plasma chemistries (BCl_3/Cl_2 , $\text{SiCl}_4/\text{Cl}_2$, and $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$) have been studied in order to obtain anisotropic etching through the multijunction heterostructure without inducing photovoltaic performance loss. SiCl_4 -based plasma chemistries have been found more suitable to achieve deep via hole etching ($\sim 30 \mu\text{m}$) without lateral etching. The study suggests that SiCl_x passivation is more efficient to protect the sidewalls compared to BCl_x . The addition of H_2 in $\text{SiCl}_4/\text{Cl}_2$ mixture appears to reinforce the sidewall passivation and thus to limit the lateral etching. III-V/Ge triple junction solar cells with standard grid line and busbar front and back contact have been fabricated on which shallow via-holes have been etched in order to assess the associated photovoltaic performance loss to each plasma etching process. Despite the fact that similar hole sidewall profiles are obtained, the electrical performances are plasma chemistry dependant. This study demonstrates that the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process presents the lowest losses with almost no induced open-circuit voltage degradation, which makes it promising for the through cell via contact architecture recently proposed for concentrated photovoltaics (CPV) solar cells.

1. Introduction

A new contact architecture has recently been proposed for multijunction solar cells [16]. Replacing the standard grid line and busbar front contact for through cell via contacts (TCVC) could increase the solar cell efficiency. A schematic of this new architecture is presented in Fig. 1. These contacts use insulated and metallized vias in order to forward the front side generated carriers to the backside where both contacts are located.

This interconnection design could result in a reduced series resistance since the millimeters-long grid lines could be replaced by micrometers-long vias. Moreover, the anode/cathode contacts on the backside do not create shading. Therefore, this architecture reduces the trade off between the series resistance and the shading that is required for conventional front side contacts. Thus, larger contacts could be fabricated on the backside which will also reduce the series resistance [20]. Furthermore, this architecture allows the suppression of the grid lines which results in a shading reduction. Both of these characteristics

could increase the cell efficiency by 3 absolute percent as shown by simulation results [16]. Moreover, since both contacts are now on the backside, the busbars are not longer required. The busbar suppression could optimize the active area and increase the power yield per wafer by 20% [16]. A first multijunction solar cell with through cell via contacts has been fabricated on a GaInP/AlGaAs heterostructure showing the technical feasibility of this architecture [15]. The inverted dual junction epitaxial structure proposed in the latter article allowed to fabricate TCVC with shallow vias ($\sim 5 \mu\text{m}$ -deep) [15]. However, such process is not suitable for TCVC fabrication on thicker epitaxial structures such as III-V/Ge triple junction heterostructures. Therefore, this new architecture faces a technological challenge: the capability to etch deep ($\sim 30 \mu\text{m}$) via holes through a complex stack of III-V/Ge heterostructures while keeping anisotropic and undamaged sidewalls with good optoelectronic surface properties. This depth would be sufficient to fabricate this new architecture if the Ge wafer is thinned from the backside. Moreover, the $30 \mu\text{m}$ target could prevent photovoltaic performance losses associated to wafer thinning [3]. Etching via-holes

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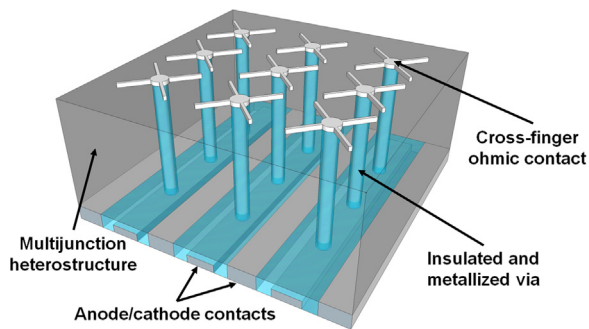


Fig. 1. Schematic of a multijunction solar cell with a through cell via contact architecture.

increases the edge area, thus increasing surface recombination at perimeter of the solar cell [5]. Moreover, it is likely that surface recombination velocity could be enhanced if the plasma process introduces damage on the sidewalls. Development of a viable TCVC technology for III-V/Ge solar cells is not possible without a suitable etching process that allows a good sidewall profile with low induced defects.

Over the past decades, several publications have reported III-V material plasma etching in chlorine-based plasmas. Indeed, Cl_2 [11,12], BCl_3 [13,14], and SiCl_4 [21,7], are all suited to etch a wide variety of III-V compounds. However, only a few studies have reported plasma etching of III-V/Ge triple junction heterostructures containing InGaP, InGaAs, GaAs, AlInP, AlGaAs, AlGaInP layers and quantum dot compounds [5,7,6].

In this study, three plasma chemistries; $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$, $\text{SiCl}_4/\text{Cl}_2$, and BCl_3/Cl_2 are investigated to perform via-hole etching on III-V/Ge multijunction heterostructures. The etch morphology presented by all three chemistries has been studied in order to evaluate which one is the most suitable for III-V/Ge heterostructure anisotropic etching. Moreover, the performance loss induced by via etching with those plasma processes has been assessed. To carry out this study, III-V/Ge triple junction solar cells with standard grid line and busbar front contact and back contact have been fabricated on which via-holes have been etched for all three plasma chemistries. Their external quantum efficiency (EQE) and open-circuit voltage (V_{oc}) have been compared to those of reference cells without via-holes to assess the performance loss associated to each plasma process.

2. Experiments

2.1. Via morphology

The samples consist of 1 cm^2 dies diced from a 100 mm commercial quantum dot enhanced cells epiwafers with III-V/Ge triple junction heterostructures consisting of an InGaP top cell, an (In)GaAs middle cell, and a Ge bottom cell [8]. The III-V heterostructure was grown on $\sim 170\text{ }\mu\text{m}$ -thick Ge wafers. The first experiment was performed to assess the etch morphology on shallow ($\sim 10\text{ }\mu\text{m}$) or deeply etched vias ($\sim 30\text{ }\mu\text{m}$). A silicon dioxide hard mask was deposited by plasma-enhanced chemical vapor deposition (PECVD) for the deep vias while photoresist was used as a mask for the shallow vias. A photolithography followed by a CF_4 plasma etching process for the samples with a hard mask were

performed to define $10\text{ }\mu\text{m}$ diameter holes in the hard mask. All III-V/Ge plasma etching processes have been performed in a Multiplex Inductively Coupled Plasma (ICP) SR III-V system from Surface Technology Systems (STS). Both the inductive source power and the bias power are operated at 13.56 MHz. The samples are mounted with Crystalbond™ on a 8" silicon carrier wafers covered with PECVD silicon oxide. A helium flow is applied to the backside of the carrier to stabilize its temperature at $20\text{ }^\circ\text{C}$ for all experiments. BCl_3 and SiCl_4 -based plasmas chemistries have been investigated to achieve via-hole etching on III-V/Ge multijunction heterostructures. The three plasma process conditions are shown in Table 1. Those conditions were chosen because they are suited to etch the III-V/Ge triple junction heterostructures [5,7].

After plasma etching, scanning electron microscopy (SEM) cross-sections were performed to study the via morphology before the passivation layer removal. A second observation was performed after the passivation layer removal using hydrofluoric acid (HF).

2.2. Impact of etching process on solar cell performance

In order to demonstrate if plasma etching process could impact the performance of a TCVC solar cell, III-V/Ge triple junction solar cells were fabricated using a standard grid line contact and via-holes were etched in the interdigitated space using different plasma processes. Fig. 2 presents schematics of the fabricated devices: a reference cell without via-holes (Fig. 2a) and a cell with via-holes (Fig. 2b).

The detailed microfabrication process is presented in a previous publication [5]. The first step consisted of a Ni/Au evaporation on the backside of the epiwafers to form the back contact. Then, a first photolithography was performed to define the grid line and busbar metallization on the front side. This metallization was fabricated by a Ni/Ge/Au/Ni/Au evaporation and a lift-off. This step defines a cell area of $5.5 \times 5.5\text{ mm}^2$. The grid line width and pitch were respectively $6\text{ }\mu\text{m}$ and $115\text{ }\mu\text{m}$. Then, a second photolithography was performed to define the via-holes. The via diameter and pitch were varied from one cell to another to study the impact of those parameters on the cell performance. One row of vias was patterned between every grid line. The pitch between the vias was 60, 80 or $100\text{ }\mu\text{m}$ and the via diameter was either 10 or $20\text{ }\mu\text{m}$. The via etching reduces the active area of 30.25 mm^2 by a factor ranging between $\sim 0.66\%$ and $\sim 4.44\%$ depending on the via diameter and pitch. Moreover, the via etching increases the perimeter to area ratio of the solar cell from $\sim 8\text{ cm}^{-1}$ to a value ranging from $\sim 35\text{ cm}^{-1}$ to $\sim 101\text{ cm}^{-1}$ depending on the via diameter and pitch. Via-holes through the III-V/Ge heterostructure were fabricated by plasma etching. A sample for each plasma process described in Section 2.1 (BCl_3/Cl_2 , $\text{SiCl}_4/\text{Cl}_2$ and $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$) and each diameter/pitch configuration was fabricated, the aim being to evaluate if the plasma chemistry used could have an impact on the cell performance.

For all three processes, the processing time was set to obtain a shallow via depth ($\sim 10\text{ }\mu\text{m}$) since only the junctions need to be etched to assess the performance loss. During the plasma etching step, the reference cells were fully protected by the photoresist film in order to expose them to the plasma process without etching any via-holes. Then, the cells were electrically insulated by saw-dicing. Finally, the contact layer was etched by a $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ solution which also etched the (In)GaAs layers via-hole sidewalls.

Table 1
Plasma conditions of the three etching processes.

Process	BCl_3 flow (sccm)	SiCl_4 flow (sccm)	H_2 flow (sccm)	Cl_2 flow (sccm)	Pressure (mTorr)	Temperature ($^\circ\text{C}$)	ICP Power (W)	Bias Power (W)
BCl_3/Cl_2	10	0	0	45	4	20	440	260
$\text{SiCl}_4/\text{Cl}_2$	0	25	0	25	4	20	440	260
$\text{SiCl}_4/\text{H}_2/\text{Cl}_2$	0	20	20	10	4	20	440	260

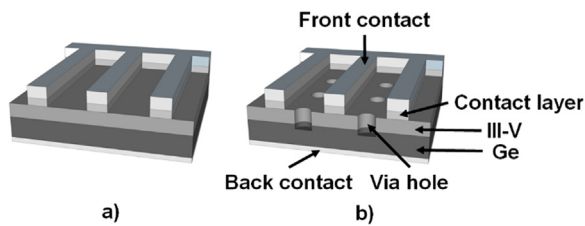


Fig. 2. Schematics of a) a reference cell without via-holes and b) a cell with via-holes [7].

External quantum efficiency (EQE), one-sun current-voltage (IV) and concentration flash measurements have been performed in order to assess the photovoltaic performance loss. The device under test is stabilized at 25 °C during all measurements on all three setups. The EQE setup consists of a QEX7 spectral response from PV measurements calibrated with a Si and a Ge photodetectors. During a subcell measurement, the other subcells are biased using two white light sources properly filtered to obtain current matching. The bottom cell EQE has been corrected to remove the measurement artifacts [17].

One-sun IV measurements are performed to obtain the one-sun open-circuit voltage (V_{oc}). The light source used is the Newport Oriel Sol1A with an AM1.5G spectrum, and the setup was calibrated with a Si solar cell. Therefore, the irradiance is $\sim 1000 \frac{W}{m^2}$. For the measurements under concentration, an AM1.5D spectrum flash tester was used. The short-circuit current density (J_{sc}) and the open-circuit voltage were measured between a concentration of 100 and 600 sun by steps of 100 sun. The real sun concentration for each measurement was obtained by dividing the J_{sc} of a specific concentration by the one-sun AM1.5D J_{sc} calculated from the EQE of the current-limiting subcell of the device. Since the real sun concentration could vary from a measurement to another, the raw data were fitted with a linear regression of the V_{oc} as a function of the logarithm of the concentration. The results presented consist of the fitted V_{oc} at a concentration of 100–600 sun by steps of 100 sun.

For the IV measurements at both one-sun and under concentration, no spectral calibration has been performed to ensure that the subcells are current-matched. However, in this specific study, the analysis is based on a comparative evaluation between the cells with via-holes and the reference cells without via-holes. Therefore, despite the fact that a spectral mismatch may occur, a V_{oc} change can be solely attributed to the via-hole etching.

3. Results and discussion

3.1. Via morphology

Fig. 3 presents cross-section SEM images of shallow vias ($\sim 10 \mu\text{m}$ -deep) etched by a) the BCl_3/Cl_2 , b) the $\text{SiCl}_4/\text{Cl}_2$ and c) the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ plasma processes described in Table 1.

From these results, all three processes etch vias in the three junctions and the tunnel junctions. Moreover, all three processes lead to about similar diameter ($\sim 10 \mu\text{m}$), confirming that a photovoltaic performance change can be assigned to the plasma process rather than a simple geometric effect such as a larger via diameter. A passivation layer can be observed on the via sidewall as shown on Fig. 3 d), e) and f). Despite the fact that all plasma processes present a passivation layer, lateral etching can be observed on the BCl_3/Cl_2 etched via as presented on Fig. 3 a) indicating that the passivation layer does not completely protect the via sidewall in the vicinity of the (In)GaAs layer. This is not observed on the vias etched with a SiCl_4 -based process as shown on Fig. 3 b) and Fig. 3 c).

BCl_3 and SiCl_4 plasmas are known to respectively provide BCl_x and SiCl_x species likely to redeposit on the patterned sidewalls and protect them from lateral erosion. Moreover, it was shown that if oxygen is

present in the gas phase (either intentionally added [10] or coming from SiO_2 cover plate sputtering or coming from the reactor walls [2]), the SiCl_x passivation layers are oxidized and turn into SiO_xCl_y -like layers which favors the deposition and makes denser passivation layers. In the case of BCl_3 plasmas, oxygen does not directly participate in the passivation layer deposition, even if a few percent of oxygen may also be incorporated into the layer [18]. The lateral erosion occurring with BCl_3 plasmas tends to suggest that $\text{B}(\text{O}_x)\text{Cl}_y$ -like layers are more permeable to plasma radicals and less resistant to the sputtering than SiO_xCl_y -like layers.

A selective sidewall erosion larger than $\sim 1 \mu\text{m}$ will complexify both the electrical insulation and the via metallization processes. The lateral etching occurring with BCl_3 plasma chemistry is problematic in achieving deeper via hole of $30 \mu\text{m}$ needed in a real integration scheme of TCVC, since it will increase with the processing time and lead to unacceptable via hole enlargement. Indeed, a sidewall erosion of $\sim 3 \mu\text{m}$ can be observed for $\sim 27 \mu\text{m}$ deep vias etched with such chemistry (not shown here). Thus, SiCl_4 -based plasmas have been further investigated for the etching of deep via holes. Fig. 4 presents cross-section images performed on deep ($\sim 30 \mu\text{m}$) vias etched by the $\text{SiCl}_4/\text{Cl}_2$ plasma process a), b) and c) before HF cleaning and d) after HF cleaning and e) the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ plasma process after HF cleaning. On the $\sim 30 \mu\text{m}$ deep vias, a thick passivation layer detached from the sidewalls can be observed on some of the III-V layers (Fig. 4 b) and the Ge (Fig. 4 c).

On an etch depth of $33.5 \mu\text{m}$, lateral etching can be observed as shown on Fig. 4 d). The $\text{SiCl}_4/\text{Cl}_2$ process results in an isotropic etch in the III-V layers with low indium concentration such as (In)GaAs for $> 30 \mu\text{m}$ -deep etching processes. The isotropic behaviour creates a lateral etch depth of $2 \mu\text{m}$ that can be observed in the III-V layers as presented on Fig. 4 d). Fig. 4 e) presents a cross-section SEM image of a via-hole etched with the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process after HF cleaning. A depth of $27.5 \mu\text{m}$ could be obtained with minimal lateral etching in the III-V layers ($< 500 \text{ nm}$). Adding H_2 in the $\text{SiCl}_4/\text{Cl}_2$ plasma has the major effect of scavenging the chlorine radicals present in the gas phase and form HCl. This has two major impacts: it decreases the Cl radical flux which is mainly responsible from lateral erosion and it reinforces the passivation layer by scavenging the Cl present in the SiO_xCl_y passivation layer to turn it into a more SiO_x -like layer [9]. Note that this improvement cannot be explained by a higher oxygen flow since the SiO_2 etch rate is identical for both SiCl_4 -based processes. This mechanism indicates that hydrogen addition may be important to reduce lateral etching and minimize sidewall damage.

As a result, the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process is the most promising plasma chemistry to achieve deep via etching of III-V/Ge heterostructures. However, plasma process optimization is still required since sidewall roughness and damage are present for all processes.

3.2. Solar cell performance

The next step was to determine the most suitable process from the solar performance standpoint. In this section, shallow vias of about $10 \mu\text{m}$ are etched using the three plasma processes presented previously. External quantum efficiency results according to the plasma process used are presented in Fig. 5.

Only the cells with via-holes with the diameter and pitch configuration presenting the highest area losses ($20 \mu\text{m}$ diameter and $60 \mu\text{m}$ pitch) are presented on this graph. A significant loss can be observed on the EQE of the InGaP top cell ($300\text{--}700 \text{ nm}$) and the (In)GaAs middle cell ($700\text{--}900 \text{ nm}$) from the via addition. This EQE loss induces a $\sim 5\%$ short-circuit current reduction, which is explained by the area loss from via etching. This characteristic is also confirmed by the fact that a lower EQE loss is obtained for smaller via diameters and larger via pitches (not shown here). However, this behaviour cannot be observed on the Ge bottom cell EQE ($900\text{--}1750 \text{ nm}$). This may be explained by the fact that the EQE artifact correction of shunt resistance related effects is

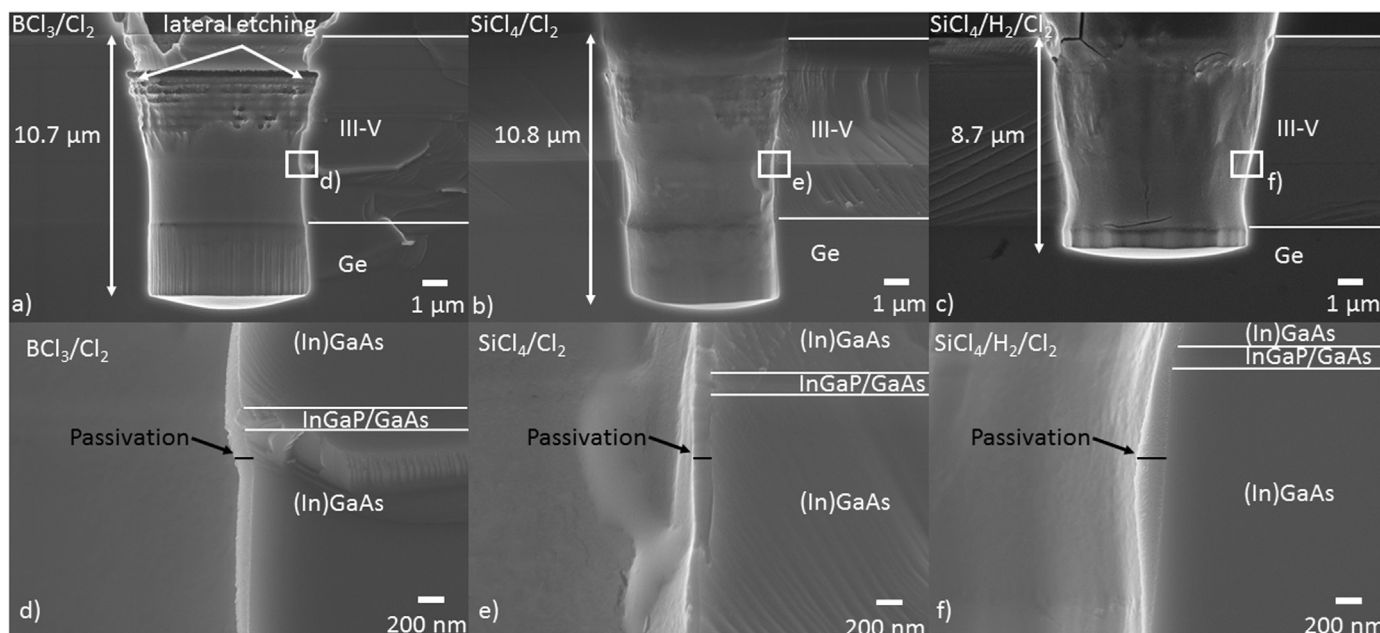


Fig. 3. Cross-section SEM images of shallow (~ 10 μm) vias etched with a) the BCl₃/Cl₂, b) the SiCl₄/Cl₂, and c) the SiCl₄/H₂/Cl₂ plasma etching processes. Cross-section SEM images of the passivation layers formed on the sidewalls of the vias etched with d) the BCl₃/Cl₂ (close-up of fig. Fig. 3 a), e) the SiCl₄/Cl₂ (close-up of fig. Fig. 3 b), and f) the SiCl₄/H₂/Cl₂ (close-up of fig. Fig. 3 c) plasma etching processes.

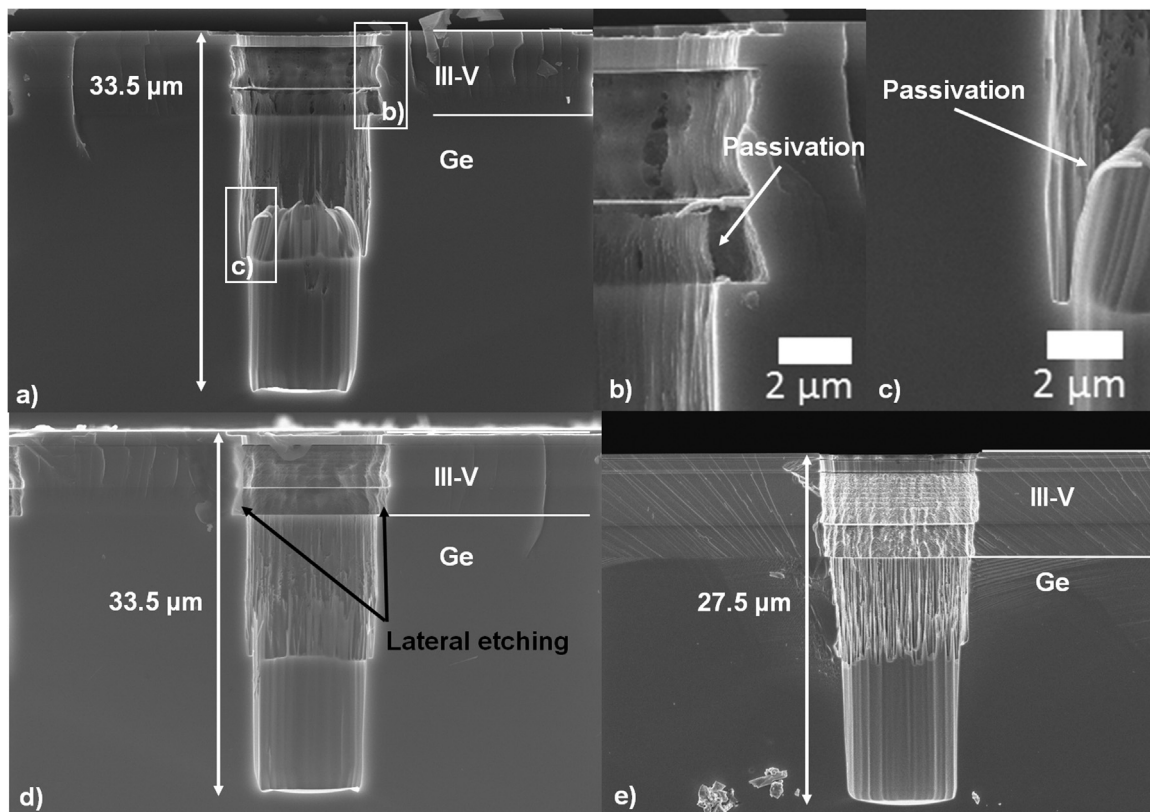


Fig. 4. Cross-section SEM images of deep vias etched with a), b) and c) the SiCl₄/Cl₂ process without HF cleaning, d) the SiCl₄/Cl₂ process with HF cleaning and e) the SiCl₄/H₂/Cl₂ process with HF cleaning. Figure b) and c) are close ups of figure a) showing the passivation on the III-V and Ge sidewall respectively.

greater than the area loss from via etching. Indeed, the expected EQE loss from the via area is ~ 4% whereas the EQE artifact correction may exceed 10%. However, the quantum efficiencies of the cells with vias presented on Fig. 5 are similar, regardless of the plasma process. Therefore, it is possible to conclude that the plasma chemistry does not affect the performance of the cells with via-holes from the external

quantum efficiency standpoint.

Fig. 6 presents the open-circuit voltage of the cells with ~ 10 μm-deep via-holes etched with the three plasma processes as a function of the via pitch. The line corresponds to the V_{oc} of the reference cell, without via-holes. In all cases, a V_{oc} loss from via etching can be observed. For smaller pitches and/or larger vias, the V_{oc} losses are more

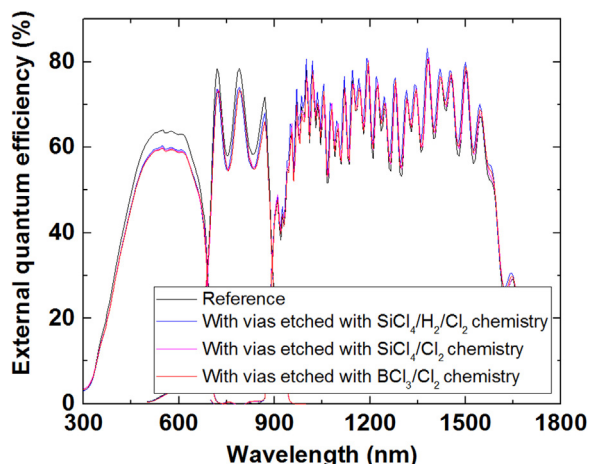


Fig. 5. External quantum efficiency of the reference cell and the cells with via-holes etched with the three plasma processes as a function of the wavelength. The results of cells with via-holes are those that maximize the perimeter to area ratio (20 μm diameter and 60 μm pitch).

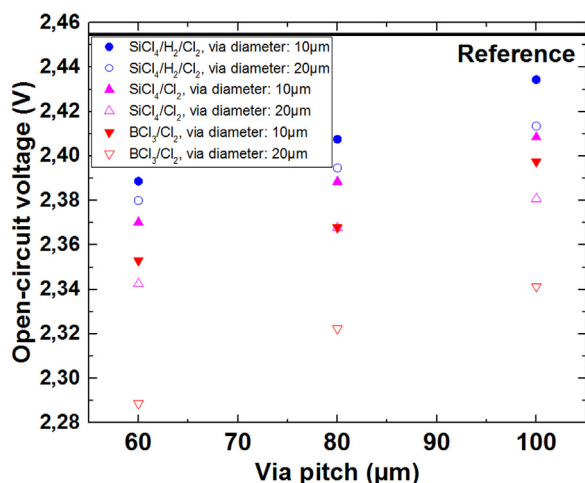


Fig. 6. One-sun open-circuit voltage of the cells with via-holes etched with the three plasma processes as a function of the via pitch. The line corresponds to the V_{oc} of the reference cell without via-holes.

pronounced. The relative V_{oc} loss from via etching for the BCl_3/Cl_2 process ranges from 2% to 7% depending on the diameter and pitch configuration. Those results are in agreement with what was previously published [5]. However, the $\text{SiCl}_4/\text{Cl}_2$ process presents a lower relative V_{oc} loss (2–5%) compared to the BCl_3/Cl_2 . Even better results can be obtained with the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process as it presents a loss ranging from 1% to 3%. The data shows that the plasma chemistry has a significant impact on the cell performance. From these results, it suggests that the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process is the most suitable one to limit the photovoltaic performance loss.

The origin of the V_{oc} loss can be explained by perimeter related effects such as an increase of the total edge recombination as reported previously [5,1,4]. A larger via diameter and a smaller pitch both increase the overall edge recombination, which can explain the behaviour observed on Fig. 6.

Fig. 7 presents the open-circuit voltage of the reference cell and the cells with via-holes etched with the three plasma processes as a function of the sun concentration.

Only the cells with via-holes with the diameter and pitch configuration presenting the highest area losses (20 μm diameter and 60 μm pitch) are presented on this graph. The losses from via-hole etching at one sun (Fig. 6) persist at higher sun concentration. However, the

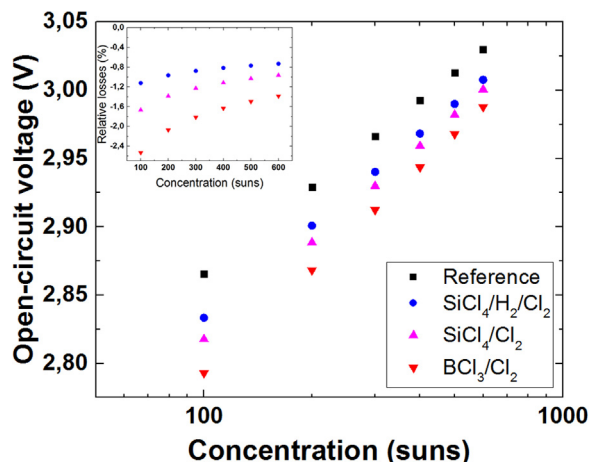


Fig. 7. Open-circuit voltage of the reference cell and the cells with via-holes etched with the three plasma processes as a function of the sun concentration. Inset: relative open-circuit voltage losses from via-hole etching for the three plasma processes. The results of cells with via-holes are those that maximize the perimeter to area ratio (20 μm diameter and 60 μm pitch).

absolute and relative reductions generated from the via-hole process decrease with larger sun concentration as confirmed in the inset of Fig. 7. This behaviour has also been observed previously [5]. This property is beneficial considering the optimum operating conditions of the through cell via contact technology is at high concentration (around or in excess of 1000 suns) [16]. Furthermore, the impact of the plasma process observed at one sun (Fig. 6) is also present at higher sun concentration. By changing the BCl_3/Cl_2 process for the $\text{SiCl}_4/\text{Cl}_2$ one, the relative V_{oc} loss from via-hole etching can be reduced from 1.4% to 1% at 600 suns using the diameter and pitch configuration that maximizes the losses. Relative losses lower than 1% can be obtained by using the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process.

The improvements can be observed at all the studied sun concentrations, which show that plasma etching optimization is a key step in the fabrication of solar cells with a through cell via contact architecture for high concentration operation. Despite the similar shallow via morphologies, plasma process has a large impact on the photovoltaic performance. It could be explained by two mechanisms: (1) The improved passivation from SiCl_4 -based processes and its enhancement from the hydrogen addition may provide further sidewall protection from the plasma damage. (2) The hydrogen addition may also provide a non-radiative defect passivation during the plasma process [19].

These results support that, by choosing the proper etching process, the output voltage-related photovoltaic performance loss induced by via-hole etching can be controlled and limited. As an example, Fig. 8 presents the relative open-circuit voltage loss as a function of the sun concentration for a promising via configuration that could be used for the new architecture (10 μm diameter, 100 μm pitch). With the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process, the relative loss is below 0.2% over a large sun concentration range, which is below the precision of the measurement setup. This shows that the losses are not significant even without a $(\text{NH}_4)_2\text{S}$ passivation treatment. Such a post-etch passivation treatment was required after the BCl_3/Cl_2 process in order to reduce the losses [5]. Furthermore, the variation of the relative losses with the sun concentration is much lower for the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ than that presented by the other processes. The observed saturation of the V_{oc} reduction for the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process indicates that this process limits the performance loss to a minimum. Therefore an increase in sun concentration does not further reduce the performance loss. From these results, the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process is clearly the most suited one for concentrated photovoltaic applications.

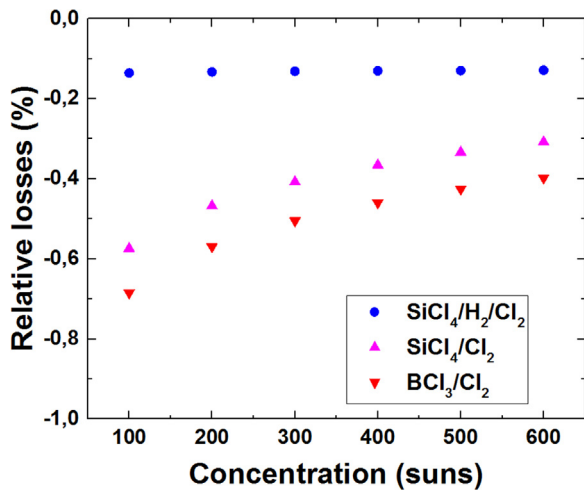


Fig. 8. Relative open-circuit voltage loss of the cell with via-holes etched with the three plasma processes as a function of the sun concentration. The via diameter is 10 μm and the pitch is 100 μm .

4. Conclusion

In conclusion, three plasma processes have been studied to etch deep anisotropic vias through a III-V/Ge triple junction solar cell heterostructure. The BCl_3/Cl_2 chemistry is not suitable to etch via deeper than 10 μm since it creates an important isotropic etching in some of the III-V layers. The anisotropy can be improved by using the $\text{SiCl}_4/\text{Cl}_2$ process. However, from the via morphology standpoint, the best process was the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ one as it can etch deep vias ($\sim 30 \mu\text{m}$) without significant isotropic etching. Moreover, the associated photovoltage performance loss has been measured in order to assess the possibility of using those processes for the fabrication of a through cell via contact architecture. For this experiment, the vias were 10 μm -deep to prevent lateral etching. A small EQE loss can be observed from via etching, independently of the plasma chemistry used. This is explained entirely by the associated area loss in active semiconductor material. An open-circuit voltage loss can be observed from via etching and its magnitude is different depending on the plasma chemistry. Both the absolute and relative V_{oc} losses decrease at higher sun concentration for all plasma processes. The performance changes are not related to the etch morphology since the via diameter and depth are almost similar for the three plasma processes. The V_{oc} losses can be reduced by using the SiCl_4 -based plasma chemistries instead of the BCl_3 one. It can even be further reduced by introducing H_2 in the $\text{SiCl}_4/\text{Cl}_2$ mixture, which makes it the most suitable process from the photovoltaic performance standpoint. The source of these losses can be explained by an increased perimeter recombination as supported by a previous study [5]. This work has shown that by using the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process to etch via-holes in the solar cells, a relative V_{oc} loss below 0.2% could be obtained compared to standard cell, which is typically below the precision of the measurement. The sidewall roughness is increased when deep etching is performed and this may induce additional performance losses. Additional developments based on the the $\text{SiCl}_4/\text{H}_2/\text{Cl}_2$ process can therefore lead to solar cell architectures based on deep vias with low roughness sidewalls and minimal photovoltaic performance loss.

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