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To cite this version:

D. Ziane, Jean Marie M Bluet, Gérard Guillot, Phillippe Godignon, J Monserrat, et al.. Characterizations of SiC/SiO2 Interface Quality Toward High Power MOSFETs Realization. International Conference on Silicon Carbide and Related Materials 2003, Oct 2003, Lyon, France. pp.1281-1286, 10.4028/www.scientific.net/MSF.457-460.1281 . hal-02060794

HAL Id: hal-02060794

https://hal.science/hal-02060794v1

Submitted on 15 Mar 2019

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Materials Science Forum *Online: 2004-06-15*
ISSN: 1662-9752, Vols. 457-460, pp 1281-1286
doi:10.4028/www.scientific.net/MSF.457-460.1281
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Characterizations of SiC/SiO_2 interface quality toward high power MOSFETs realization

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Keywords: MOS, Interface states, Sublimation epitaxy, C-V, G-V.

Abstract. The low channel mobility in N-MOS 4H-SiC transistor is a major key issue for the development of power devices with satisfactory on state characteristics. Previous works have demonstrated that this low channel mobility is due to high interface state density (Dit) near the conduction band edge. Furthermore, the realization of SiC MOSFETs sustaining high reverse field necessitates thick epitaxial layer growth. An important thickness (> 30 µm) unfortunately involves important surface roughness which may result in a high interface trap density (Dit) and surface potential fluctuation (σ_s) at the SiC/SiO_2 interface. In this study, we focus on SiO_2/SiC MOS interface quality characterization as a function of process conditions and material properties (dopant type, thick layer growth technique). Investigations of the oxide quality on thick layers grown by CVD and PVT has been realized using CV under UV lightening and GV techniques. We evidenced that the Dit value (between 10^{10} $cm^{-2}.eV^{-1}$ and 9×10^{10} $cm^{-2}.eV^{-1}$ from 0.9 Ev to 0.2 eV below Ec) and σ_s value (60 mV) were slightly lower for thick PVT layers. A discrepancy in the Dit values obtained from C-V and G-V measurements is attributed to the large surface potential standard deviation. Results from an original oxide growth process using a deposited sacrificial silicon layer under UHV conditions are also presented.

Introduction

Impressive progress in 4H-SiC MOSFETs performance, notably in the blocking capability, has been realized in the past ten years [1]. For instance a D-MOS device blocking 10 kV has been presented in this conference [2]. Nevertheless, one of the major key issues for the development of marketable 4H-SiC power MOSFETs is the reduction of the on state specific resistance. Indeed, despite the advantage, in comparison with silicon, of a lower epitaxial layer resistance at a given voltage, the specific R_{ON} is higher than expected. This is due to the high resistance of the channel which contribution to the total resistance can be as high as 82% [3] at room temperature. This high resistance comes from the presence of a large acceptor interface trap density (D_{it}) increasing steeply toward the conduction band [4]. Consequently, an important part of inversion electrons does not participate in the conduction, given they are trapped at these defects. This point has been confirmed by Thermally Stimulated Current [5] and Hall Effect measurements [6-7]. The high density of trapped electrons causes an important coulombic scattering for the remaining conductive ones which is the reason for the low channel mobility in N-MOS 4H-SiC transistors [8-10]. An NMOS inversion transistor will be realized on a p implanted channel. In order to optimize the oxide growth process, it is then necessary to measure with accuracy the Dit at the vicinity of the conduction band edge using a capacitor on a p-type layer. Toward this end we used CV measurements used under UV illumination. Layers grown by the sublimation method (PVT) were studied because the realization of power SiC MOSFETs sustaining high reverse field necessitates thick epitaxial layer growth. Indeed very high speed growth (50 $\mu m.h^{-1}$) is reached by this method. An important

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thickness (> 30 µm) unfortunately involves important surface roughness which may increase the interface trap density (Dit) and the surface potential fluctuation (σ_s) at the SiC/SiO_2 interface. To investigate this point, conductance measurements were carried out on n-type thick layers grown by the CVD and PVT methods.

Experimental

In order to measure Dit, MOS capacitors were realized on n^- and p^- type 4H-SiC layers (respectively 10µm, $N_D = 5\times10^{16}$ cm^{-3} and 4.9 µm, $N_A = 1.2\times10^{16}$ cm^{-3}). Samples were oxidised using dry oxidation at 1150°C followed by in-situ anneal in argon and wet re-oxidation at 950°C. Aluminium was sputtered, and finally different circular dots were patterned. Additional capacitors were realized on thick epitaxial layers (30 µm, 10^{16} cm^{-3}) realized by physical vapour transport (PVT). The details about PVT epitaxy can be found in [11]. This conventional oxide growth process is compared to an original approach using a sacrificial silicon layer called SSOI hereafter. The process consist in a surface cleaning in ultra high vacuum condition followed by an e-beam evaporation of a Si layer on the SiC surface and finally in the wet oxidation at 950°C followed by ROA and POA in Ar at 950°C [12].

The CV measurements were realized at high frequency (1 Mhz) and low frequency (20-100 Hz) using a HP4140A RLC meter. A mercury lamp was used as the UV source. The samples were illuminated directly on the front side or on the substrate side using a mirror. In the last case the CV measurements were performed on lateral structures.

The interface trap density and the surface potential (σ_s) fluctuation have been extracted by the conductance method at room temperature. The frequency was scanned from 100 Hz to 1 MHz and the gate voltage in the range of -10V + 10V. The Dit profiling in the band gap was limited to 2.3 eV<E_t-E_v<3eV by the explored frequency range.

C-V Results and discussion

Because of the very low intrinsic carrier density due to the SiC wide band gap, inversion regime cannot be obtained during low frequency CV measurement. Consequently, interface defects can only be measured near the majority carrier band. Nevertheless, for N-MOS gate oxide optimisation, using standard CV characterization on capacitors, it is necessary to assess Dit near the conduction band on a p-type layer. Toward this end, we used UV illumination from a mercury lamp in order to create minority carrier and to get full inversion. The measurements were performed from accumulation to inversion. As can be seen in figure 1, in the case of n-type samples, we first obtained very broad low frequency CV curves under UV illumination due to a progressive shift of the characteristics toward negative bias. Consequently, the inversion occurs but for abnormally high gate voltage and the apparent extracted surface potential (Ψ_s) excursion is of 6 eV (shown in the insert) which is about two times the SiC band gap. The reason is that the UV light has to be maintained during the whole measurement because of the low minority carrier

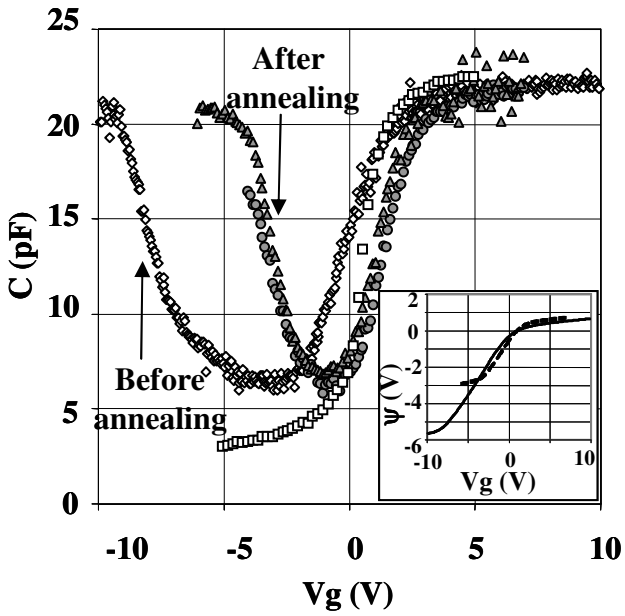

Fig. 1 High frequency (1MHz) CV curve (open squares) and low frequency (20Hz) CV curves before and after annealing (450°C, 1 hour in H_2). Before annealing the CV drifts towards negative bias, after annealing (450°C, 1h.) abrupt inversion is reproducibly found.
The insert represents the Ψ_s excursion before (solid line) and after (dashed line) the annealing.

lifetime in SiC (in the order of 100 ns). The proposed mechanism is that a positive charge is progressively created in the oxide by the discharge of slow negative traps, during the measurement. In the case of fresh p-type samples, the inversion regime was not observed at all even under UV light. An additional annealing (450°C, 1 hour in N_2 atmosphere) was then performed and the CV measurements carried out again. After this treatment, abrupt inversion has been obtained both for n^- and p^- type samples (see figure 1). The Ψ_s excursion was then corresponding to the 4H band gap and we succeed in Dit profiling versus energy in the whole band gap both for n^- and p^- type 4H-SiC MOS capacitors. The results for the both type is presented in figure 2. In the case of n-type, an almost symmetric profile is found with a minimum Dit of 6×10^{10} $cm^{-2}eV^{-1}$ at midgap and a very important increasing near the conduction band edge. In the case of p^-, the Dit is globally more important in the whole band gap with again a very strong increasing near the conduction band. Using this measurement technique, we can probe acceptor states at the neighbourhood of the conduction band for p-type layers and then have feed-back to optimize the SiO_2/SiC interface in order to realize N-MOS transistors. Furthermore, the efficiency of a given process in reducing Dit in the whole bandgap can be evaluated in one measurement on a unique sample (n or p type). Nevertheless, in the case of important disorder at the interface which induces important surface potential fluctuations, the Dit extraction by CV methods (Terman, C_{HF}-C_{LH} or quasi static) is over-estimated [13, 14]. In order to estimate these surface potential fluctuations, we then carried out conductance measurements on the capacitors.

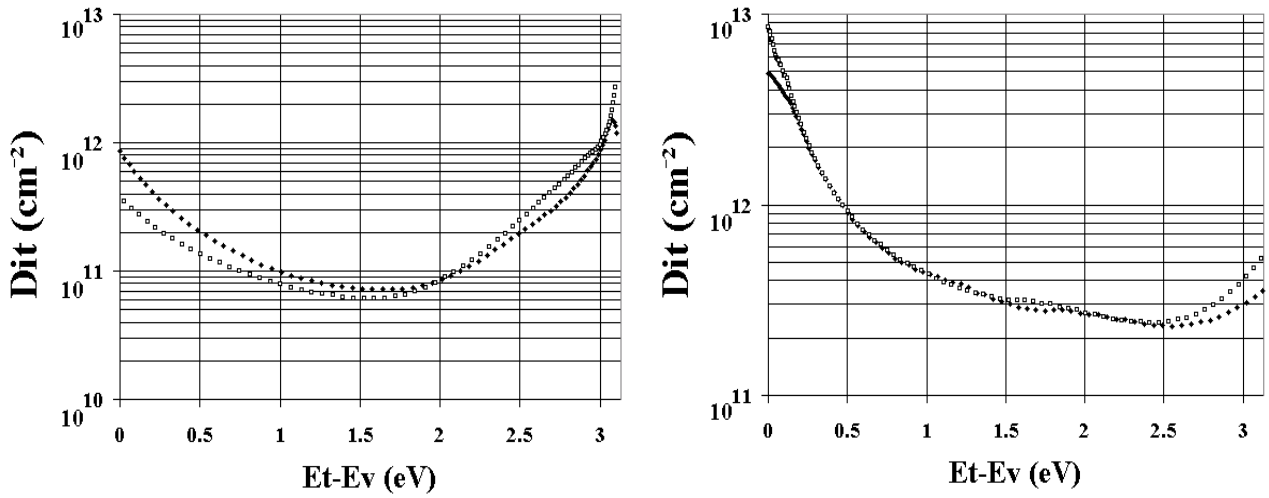

Fig. 2 D_{it} profiles in the whole bandgap for n-type (left figure) and p-type (right figure) epitaxy.

G-V Results and discussion

The conductance method consists of the measurement of the equivalent parallel capacitance (C_p) and conductance (G_p) parameters during a frequency sweep for a given gate bias. The measurement is then repeated for different gate bias values. After serial resistance correction, interface state densities are extracted for each gate bias, and then for the corresponding surface potential, from the peak value of the (G_p/ω) ratio. Surface potential fluctuation represents the deviation from the adopted interface state model (in our case continuum model), and give the influence of the oxide charge disorder on the surface potential estimation. Conductance technique also allows estimation of the emission time (10^{-6} s) and the cross section (10^{-18} –10^{-20} cm^2) of defects.

Figure 3 shows the interface state density extracted for four different samples using different process. Three points are noticeable from this figure:

First we clearly observe a great difference between the two SSO samples. In the case of sample SSO_2, the Dit distribution looks like usual results for SiC/SiO_2 interface: an exponential increase near the conduction band (CB). At the opposite, for sample SSO_1 the interface states profile is almost flat with extremely low value of 6×10^{10} cm^{-2} even near the CB. The difference between the two samples is the silicon overlayer oxidation duration (shorter for SSO_1). The good results for SSO_1 may then be due to incomplete oxidation of the silicon overlayer. The extracted interface state density is then the one of SiO_2/Si interface. Ellipsometry measurements have been performed to clarify this point [16]. In the case of sample SSO_2, the SiC has been oxidized. Because the oxidation process and the POA are not optimized for SiC oxidation, the interface state density is high. The difficulty of the SSO process is to stop the Si oxidation just at the Si/SiC interface. An other possibility is to use a nitridation of the surface [17] or the deposit of a thin Si_3N_4 layer [18] before the silicon overlayer deposition.

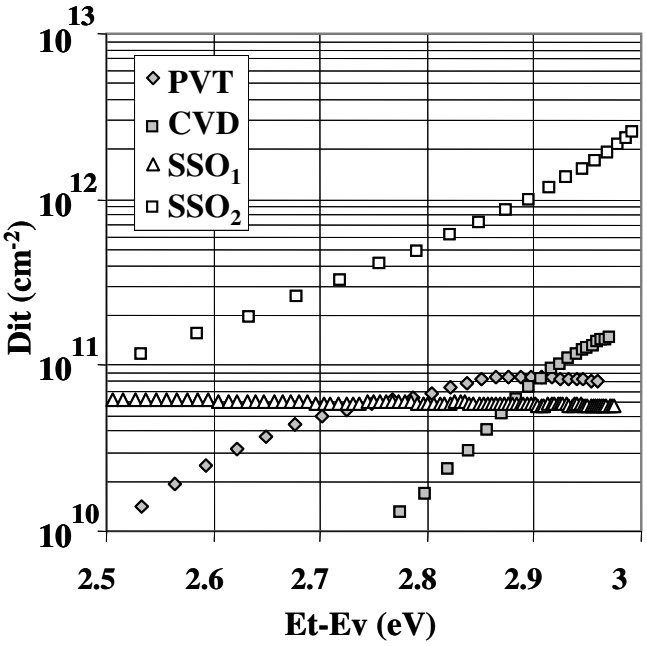

Fig. 3 Interface state density ditribution near CB for different samples.

Second, we evidence a slightly lower Dit for the oxide grown on the thick PVT layer (between 1×10^{10} $cm^{-2}eV^{-1}$ and 9×10^{10} $cm^{-2}eV^{-1}$) than for the CVD layer. This difference cannot be attributed to a better purity of the PVT layer as the impurity level (Al and B compensation, metallic impurities) may not be lower than in the CVD one. Furthermore it has been shown that SiC/SiO2 interface defects are most probably intrinsic defects [4, 19]. The difference may then be attributed to a better surface morphology.

Finally, the obtained Dit values are much lower than those from CV measurements. In the previous section we supposed that the Dit extracted from CV measurements could be overestimated because of a high fluctuation of the surface potential. The standard deviation (σ_s) of the surface potential has been extracted for the different samples using the method proposed by Nicolian and Goetzberger [20]. The results are presented in figure 4. First, we notice that σ_s is slightly lower in the case of PVT layers. The very low value for SSO has been obtained for sample SSO_1 and is consequently characteristic of the Si/SiO_2 interface. Secondly, the σ_s values are high (in comparison with silicon). These σ_s values between 2 and 4 kT/q imply that the method of extraction itself is not accurate. Indeed the linear approximation of the Boltzman relation

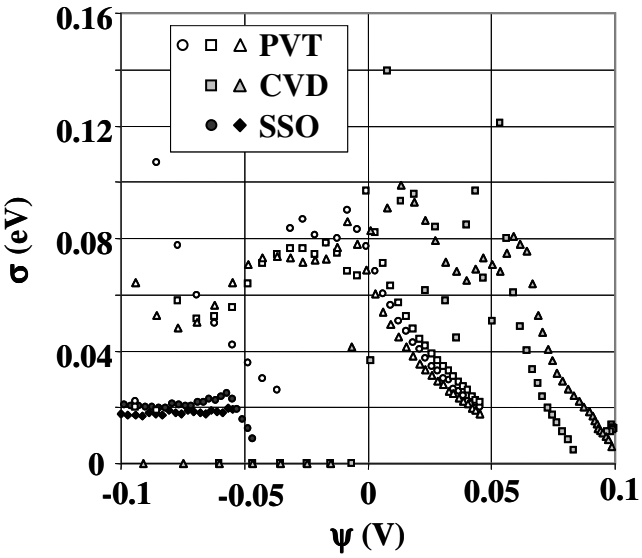

Fig. 4 Standard deviation of the surface potential as a functionof the surface potential for the different samples.

between surface charge variation and surface potential variation is correct for a surface potential variation smaller than the thermal energy. These high σ_s values lead to an underestimation of the interface state density by the GV method.

Another reason for Dit underestimation using the GV method could be the presence of different populations of interface traps resulting in a non unique G_p/ω vs ω bell curve. This effect was observed in the case of PVT layers and is illustrated on figure 5. For the left figure corresponding to CVD layers only one peak is observable in Vg = const. planes. For the right figure, corresponding to the PVT layer, two peaks are present at some Vg. These two peaks may be due to two populations of interface traps responding to two different frequencies. When taking into account only the absolute maxima of the Gp/ω vs ω curve, one can underestimate the total amount of interface traps.

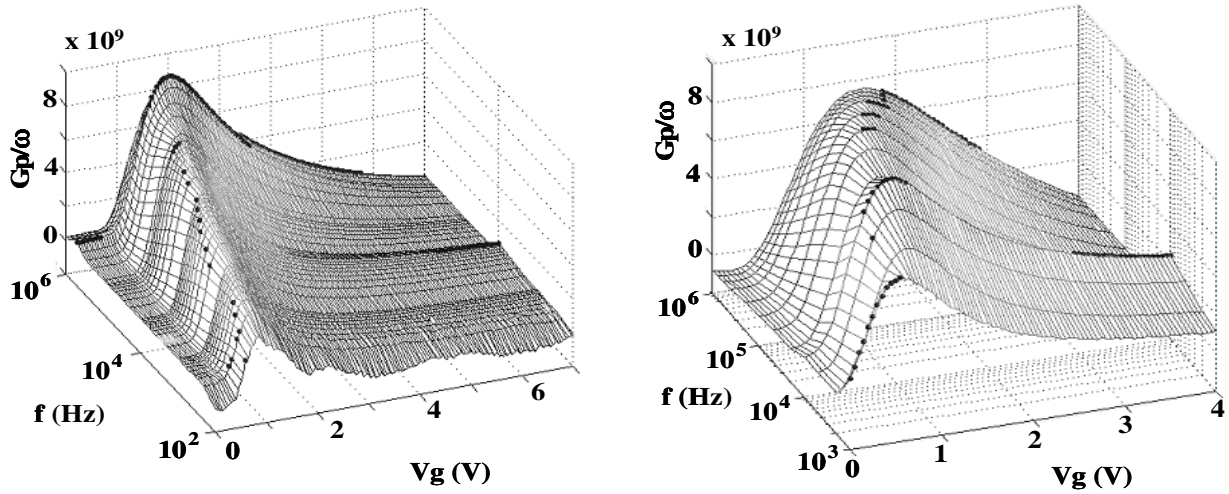

Fig. 5 Gp/ω as a function of Vg and frequency. The black points are the maxima of the Gp/ω vs ω curves.

Conclusion

The C_{HF}-C_{LF} technique has been adapted to silicon carbide using UV illumination in order to get full inversion. Using this measurement method, the interface trap density has been determined, for the first time, in the whole bandgap for both n and p type materials. Complementary conductance measurements show that an important disorder measured by the surface potential standard deviation (σ_s) is present at the SiC/SiO_2 interface using conventional dry oxidation. These high values of σ_s imply that the interface trap density is overestimated when extracted from capacitance measurement and underestimated when extracted from conductance measurements. A slightly lower value of σ_s and of the interface trap density was obtained in the case of thick PVT layers. This better interface quality is most probably due to a better surface morphology of the epitaxy (no more polishing scratches for instance after a sublimation epitaxy). This makes the sublimation epitaxy technique, promising for thick drift layers growth.

Acknowledgements

This work has been performed under the Frame work of ESCAPEE project funded by the European Community.

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