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Abstract. V_{TH} instabilities of SiC MOSFET are made of a permanent and a recoverable part. V_{TH} hysteresis is a recoverable instability which affects the operation of the device since the threshold voltage depends on the negative bias applied previously, but is erased when the MOSFET is biased above the threshold voltage. In this paper, the phenomenon is assessed through experiments and TCAD simulation. The results are in good agreement and show that the V_{TH} hysteresis is mainly caused by the hole trapping in the oxide near the interface. The C(V) characteristics of the measured device is similar to the simulated device having a concentration of 10^{12} holes/cm^2 trapped at the interface.

Introduction

4H-SiC MOSFETs are available in the market as discrete devices or power modules. These devices present many advantages for power conversion compared to Si IGBTs but still suffer from some (reliability) drawbacks [1-3]. The threshold voltage instability of SiC MOSFETs is a topic that mainly focuses on permanent drift of the V_{TH}. Recoverable enhancement of the drain current in the subthreshold domain has been previously pointed out for SiC MOSFETs [4] and has gained interest since it may affect the stability of the device. This phenomenon is not completely unknown since it affects Si devices as well [5], but the Wide Band Gap of SiC enhances it and can produce a shift of the V_{TH} up to several volts. As a consequence, V_{TH} hysteresis can make the devices switch faster [6], which could be an advantage to normal operation, but it can also make the devices switch on at lower gate bias, thus making them prone to undesired switching, leading to short circuit failure.

4H-SiC MOSFETs V_{TH} subthreshold hysteresis can range from several tens of millivolts to several volts depending on the structure of the device [7]. They are usually attributed to the modification of the surface potential induced by holes captured at the edge of the oxide when the gate is negatively biased [4,8]. In this paper we will focus only on the V_{TH} subthreshold Hysteresis of planar MOSFETs through measurements and TCAD simulation. This will give a better understanding of the role of the interface states that are generated by the oxide traps.

Drain Current Hysteresis measurement and analysis

The subthreshold drain current depends strongly on the prior state of the device. In order to obtain the same value of drain current at the subthreshold domain, a higher gate bias is needed when going from on-state to off-state than vice versa. Once the gate is biased above the V_{TH} voltage, the drain current doesn't depend on the previous state anymore. This behaviour is illustrated in figure 1, where depending on the off-state starting voltage the subthreshold drain current varies by 2 decades. The measurements in Fig. 1 were performed at room temperature on commercially available 120 mΩ – 900 V MOSFETs. The bias voltage has been swept-up from a starting voltage in the range V_{GS}^{Start} = [- 20 V, - 10 V, - 5 V, - 2 V and 0 V] to just above the threshold voltage (V_{GS} = 4 V) with a step of 100 mV and a delay of 50 µs, while the drain bias

voltage was kept constant at 1 V. The measurements are done at constant rate and the negative bias has not been applied before the sweep, in order to avoid any unnecessary stress on the gate oxide. All the measurements were carried out after a preconditioning procedure (a sweep from 0 V to 10 V with a 100 mV step without delay) that erases any remaining hysteresis. This is shown by the complete overlapping of the down-sweep traces, independently of V_{GS}^{Start}. The values shown in figure 2 where extracted for a drain current of I_D = 100 nA, from measurements carried out at several temperatures (25°C, 50°C, 100°C, 150°C). As can be seen from Fig. 2, the hysteresis is a function of off-state starting gate bias voltage and depends strongly on the operating temperature. The decrease of the hysteresis is a consequence of the acceleration of capture-emission mechanisms at higher temperature.

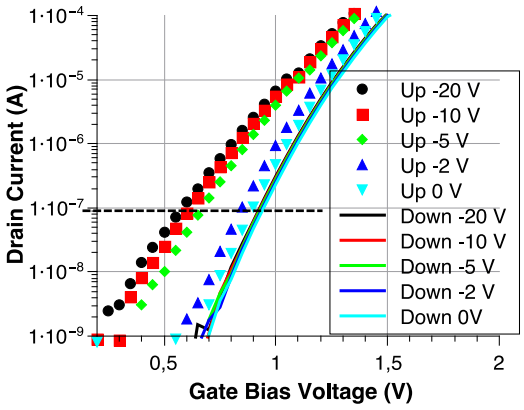

Fig. 1 – Drain current subthreshold hysteresis of commercial 900 V planar SiC MOSFET.

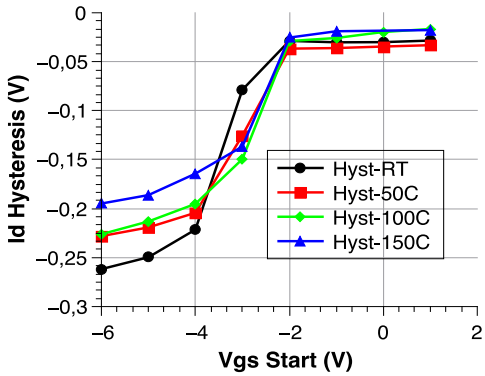

Fig. 2 – Temperature dependence of the drain current subthreshold hysteresis of 900 V SiC MOSFET extracted at 100 nA.

C(V) measurements were also carried out to study the effect of the hysteresis. The measurements were performed with very short periods of time in-between the heating ramp followed by a preconditioning sequence. The sweep was done from negative to positive with a step of 100mV and at 100 kHz with an AC amplitude of 25 mV. From C(V) measurement at different temperatures in Fig. 3, one can see that the V_{FB} is slightly shifted whereas the V_{TH} doesn't change. Since the occupancy of traps depends on the position of the Fermi level, one can predict the nature of traps, donors (hole) traps or acceptors (electron) traps, and the capture/emission mechanisms happening at the interface. In this case we can state that the traps are of donor type and that their energy levels are located near the valence band, since only the V_{FB} is affected by the increasing temperature. If acceptor traps were present at the oxide edge or at the interface, the V_{TH} would be shifted as well for different temperatures.

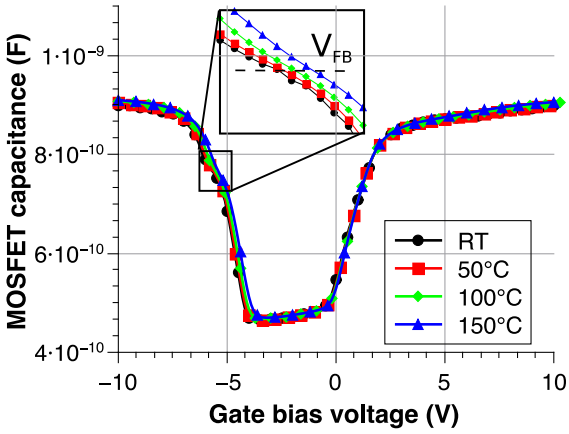

Fig. 3 – 4H-SiC planar MOSFET capacitance for different temperatures.

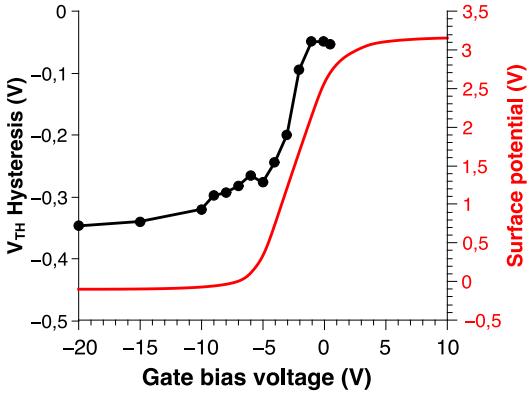

Fig. 4 – 4H-SiC planar MOSFET V_{TH} Hysteresis and the corresponding surface potential as a function of the gate bias voltage.

To validate this hypothesis, the technique presented in [9] was used to compute the dependence of the surface potential on the gate bias voltage from C(V) measurements. This technique allows for the computation of the surface potential without knowing the technical data of the device. The results are shown in figure 4 (red curve, right) along with the V_{TH} hysteresis at room temperature (black dotted curve, left). The extracted surface potential indicates a very low V_{FB} voltage which is due to the difference of the gate/oxide workfunctions and the positive fixed charge in the oxide. One interesting fact is the saturation of hysteresis between – 20 V and – 6 V, which in terms of traps means that all donor traps are filled, since the Fermi Level is just below the Valence Band. For V_{GS}^{Start} between – 5 V and 0 V the hysteresis shows a steep variation. This is related to the presence of traps energy levels found between E_V + 0.35 eV and E_V + 2.05 eV.

Above E_V + 2.05 eV there seems to be no traps with a dynamic behaviour that can affect the V_{TH} hysteresis. If there are any acceptor or donor traps between E_V + 2.05 eV and E_C, they are too fast to be measured by a transfer characteristic measurement.

Simulation of the interface trapped charge

For a better assessment of the role of the interface states in the hysteresis phenomenon, Sentaurus TCAD [10] simulations have been performed. The simulated structure was designed and optimised to fit the transfer characteristics, the output characteristics and the breakdown voltage of the measured device. The physical models which account for the modification of the channel mobility due to interface trapped charge, high electric field induced saturation, incomplete ionisation of the dopants, anisotropy of 4H-SiC depending on the crystal direction that were used for the accurate simulation of the device were taken from literature [11]. The AC coupled simulations of the C(V) characteristics are carried out on the same circuit used for the measurement. The Shorted Source and Drain configuration is used and two Gaussian distributions of traps are placed at the interface in order to asses their effect on the C(V) characteristics and compare with the measurements obtained for several temperatures. The distribution of energy levels of traps where chosen near the conductance and valence band to show the qualitative influence of donor and acceptor traps with identical characteristics would produce on the C(V) characteristics. Further studies are required to determine the actual energy levels of traps that affect directly the V_{TH} hysteresis and asses them in simulation. The details are resumed in Tab. 1.

Tab.1 – Traps characteristics employed in the FE simulation.

Type	Conc. (cm^{-2})	Energy Mid	Energy Sigma	e^- Crossection	h^+ Crossection
Acceptor	10^9	E_C – 0.3 eV	0.1 eV	1e-13	1e-15
	10^{12}				
Donor	10^9	E_V + 0.3 eV	0.1 eV	1e-15	1e-13
	10^{12}				
Fixed Charge	10^{12}	NA	NA	NA	NA

The interface of the simulated structure is shown in Fig. 5. The charge captured at the interface is computed at 10 V of V_{GS}. The captured charge modifies the C(V) characteristics of the device and shifts it either to the left in case of donor traps, or to the right in case of acceptor traps. This assumption is supported by the simulation results shown in Fig. 6, where the typical C(V) characteristics is shown for 4 different cases of interface traps. More interestingly, the simulation at different temperatures of the interface containing only donor traps (Fig. 7) shows the same tendency as the measurements results of Fig. 3, proving that the V_{TH} hysteresis is a phenomenon that happens as a result of captured holes at the interface and at the semiconductor side border of the oxide.

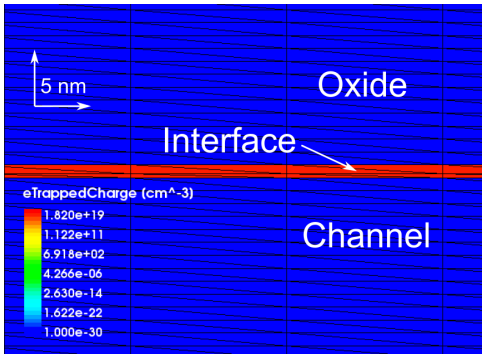

Fig. 5 – Simulation of the charge captured at the interface of a 4H-SiC planar MOSFET containing a concentration of 10^{12} donor and 10^{12} acceptor traps biased at V_{GS} =10 V.

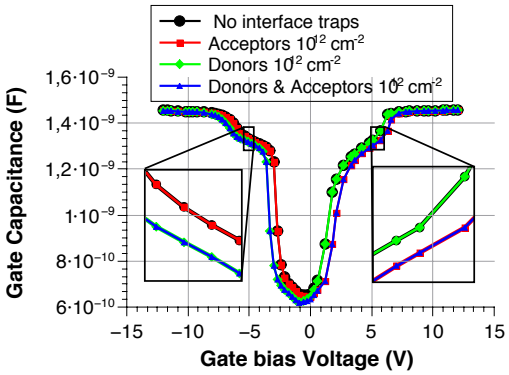

Fig. 6 – C(V) simulation of the effect of the interface traps in a planar 4H-SiC MOSFET.

Conclusions

The V_{TH} hysteresis is shown to be a result of the negative bias of the V_{GS}. The different temperature measurements show that its saturation value decreases with the increase of temperature. This behaviour is attributed to the traps at the interface and in the oxide next to the interface. Donor traps can be held responsible for the hysteresis behaviour since the phenomenon is recovered for V_{GS} higher than the V_{TH}. C(V) characteristics and simulations show that the V_{FB} decreases for increasing temperature when donor traps are introduced at the oxide semiconductor interface. This is a clear proof that the hysteresis is caused by trapped holes at the interface. Further investigations will be carried on to simulate the hysteresis as a function of the gate bias voltage of the previous state of the MOSFET.

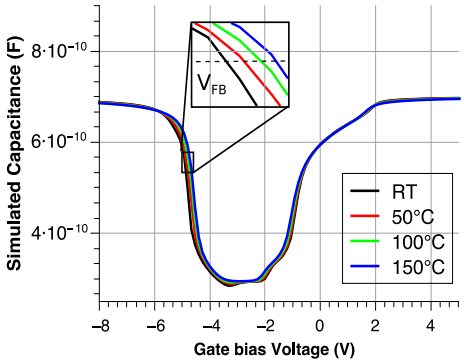

Fig. 7 – Simulation of the MOSFET capacitance for different temperatures.

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