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# High-Voltage SiC-JFET Fabrication and Full Characterization

B. Asllani<sup>1, a</sup>, P. Bevilacqua<sup>1, b</sup>, A. Zaoui<sup>1, c</sup>, G. Grosset<sup>2, d</sup>, D. Planson<sup>1, e</sup>  
and H. Morel<sup>1, f\*</sup>

<sup>1</sup> Univ Lyon, INSA Lyon, CNRS, Ampère, F-69621 Lyon, France

<sup>2</sup> ION BEAM SERVICES, F-13790 Peynier, France

<sup>a</sup> besar.asllani@gmail.com, <sup>b</sup> pascal.bevilacqua@insa-lyon.fr, <sup>c</sup> abderrahime.zaoui@insa-lyon.fr,

<sup>d</sup> gregory.grosset@ion-beam-services.com,

<sup>e</sup> dominique.planson@insa-lyon.fr, <sup>f</sup> herve.morel@insa-lyon.fr

**Keywords:** 4H-SiC JFET, device processing, high voltage device, device characterization, double-pulse switching

**Abstract.** 3.3 kV Power JFETs have been designed, fabricated and measured in the framework of the FilSiC project. The paper presents the main characterization results with classical static and dynamic measurements as well as double pulse tests for switching characterization. The study is completed by a data-sheet evaluation for the measured components and an evaluation of the associated safe operating area.

## Introduction

Silicon Carbide (SiC) enables to develop high-voltage devices. While most of studies concern Power MOSFETs [1][2], the present study focuses on JFETs because of its possible better robustness particularly in short-circuit operation [3]. The targeted JFET rating was selected to 3300 V, 20 A.

The possible applications could include high voltage DC-breakers [4] or Solid State Power Controllers (SSPC) [5] as well as all applications covered by SiC-MOSFETs.

## Device Processing

To reach the targeted characteristics a vertical structure with vertical and lateral channels were designed as shown in Fig. 1. The lateral channel enables an easy design with a low absolute value of the gate-source threshold voltage. It is easier to manufacture but yields a higher on-state resistance ( $R_{on}$ ) in comparison with a pure vertical channel. So, an optimization was achieved.

Devices were fabricated on a n-type epitaxial layer with a thickness of 32.7  $\mu\text{m}$  and a doping concentration of  $9.7 \times 10^{14} \text{ cm}^{-3}$ . 13 photolithography mask levels were used. A double gate structure was obtained through ion implantation for the buried gate and epitaxial regrowth for the surface gate. The edge termination of the JFETs includes a MESA structure and a junction termination extension (JTE). The front side and back side metalizations are in Ag. The second passivation uses polyimide.

Best dies were diced and packaged to enable high current measurements. The packaging was an optimization of Iso4 standard package made by DeepConcept Company as shown in Fig. 2. The size is the same but the internal design is optimized for SiC and for 3300 V voltage. The package can operate up to 200°C. In this case, the support is a metal one: (Cu, Al + termination Ni, Au, Ag).

## Standard Electrical Characteristics

The electrical characterization includes: standard static characteristics as the output characteristic (Fig. 3), the transfer characteristic, dynamic characteristics like  $C_{rss}$ ,  $C_{iss}$ . For such standard characterization a Keysight B1506A curve tracer was used. Some adapted procedures were developed to fit the normally-on electrical characterization of JFETs. Fig. 3 and 4 show some typical results. The gate threshold voltage is measured in the range -17.2 V to -18.5 V (See Table). As a complement,

an IWATSU CS-5400 curve tracer was used for measuring the on-resistance versus the temperature. Fig. 5 and 6 show the associated results.

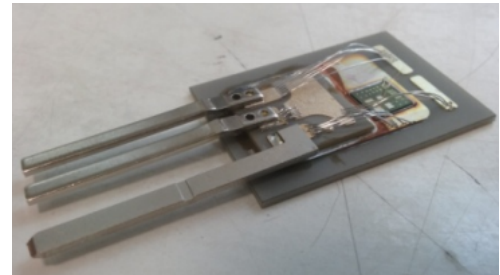
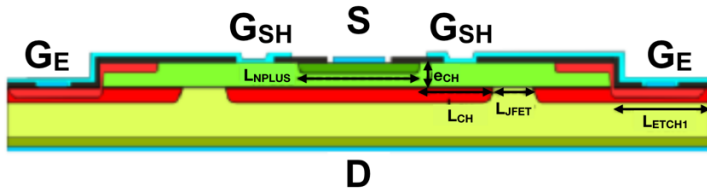


Fig. 1 – Schematic cross section of the JFET structure

Fig. 2 – A JFET die on its package

On-resistance varies from about 400 mΩ to 1.5 Ω in the range of 25 °C to 180 °C. The measurement temperature was limited to 180 °C because of the package limits, but the SiC-JFET die may operate at higher temperature [7]. The leakage current is shown in Fig. 7. The Drain-source breakdown voltage does not achieve the target value due to a higher dose of implantation of the peripheral protection compared to the aimed one. The capacitance measurements are given in Fig. 8.

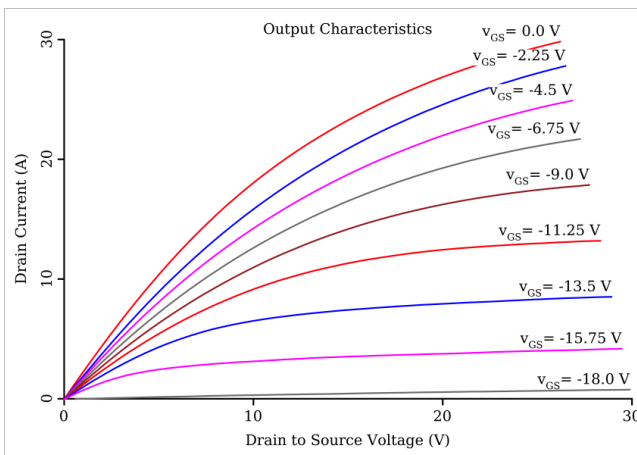


Fig. 3 – Output Characteristics @ 25 °C – 32-J4, B1506A

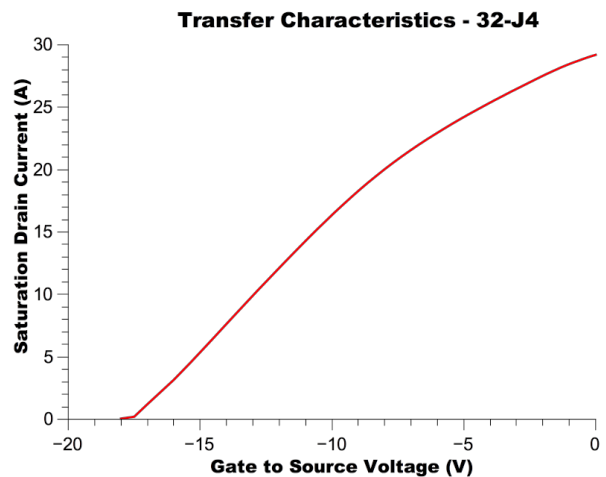


Fig. 4 – Transfer Characteristics @  $V_{DS}=30$  V,  $T_J=25$  °C, 32-J4, B1506A

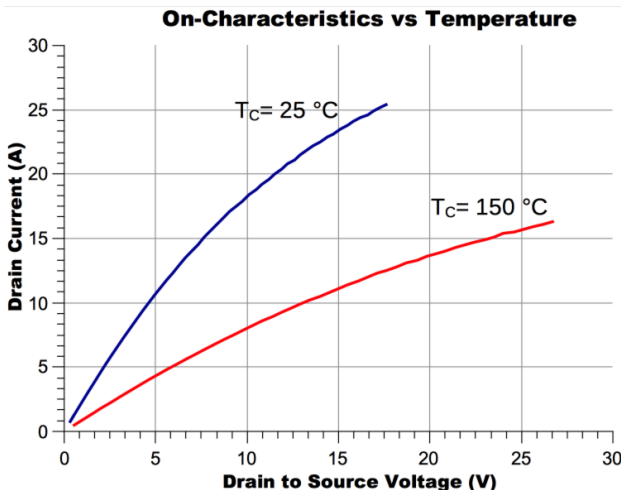


Fig. 5 – On Characteristics vs temperature @  $V_{GS}=0$  V, 32-J4, IWATSU.

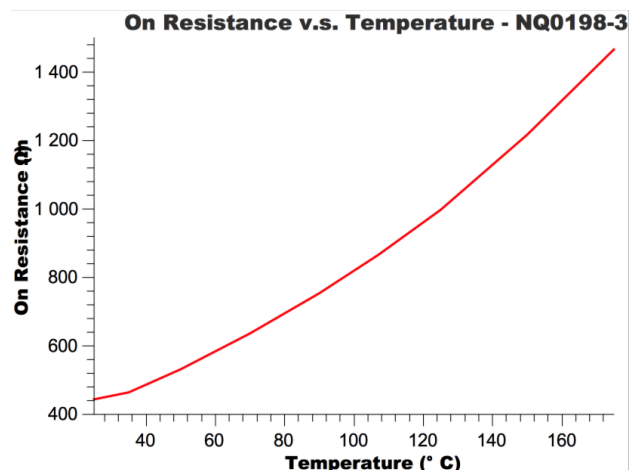


Fig. 6 – On resistance vs temperature @  $V_{DS}=30$  V,  $V_{GS}=0$  V, 32-J4, B1506A

## Switching Characteristics

To complete the measurement obtained by industrial characterization product (B1506 and IWATSU CS 1500) Double Pulse Tests (DPT) [8][9] have been achieved. The DPT circuit was adapted to high voltage switching. Some results are shown in Fig. 9 and 10.

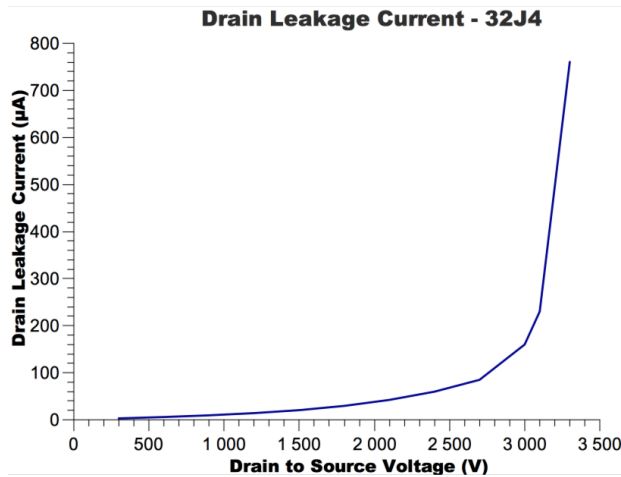


Fig. 7 – Measured leakage current v.s. the applied voltage @ 25 °C – 32-J4, B1506A

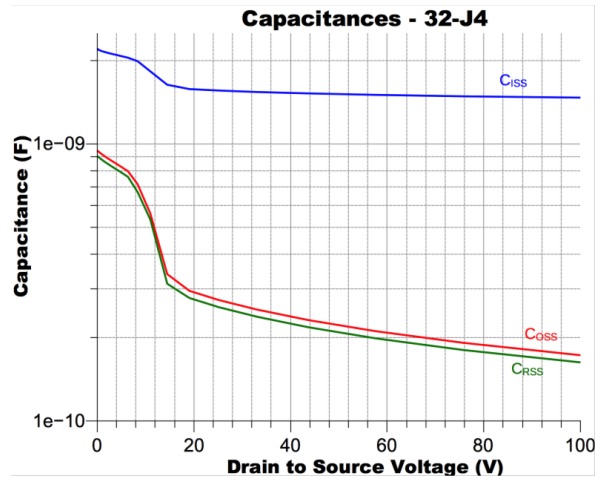


Fig. 8 – Capacitance measurements @  $T_J = 25\text{ °C}$ , 32-J4, B1506A

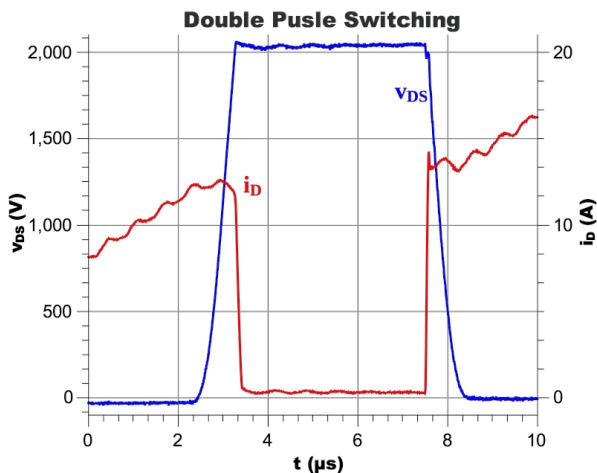


Fig. 9 – Double pulse test measurements,  $i_D$  and  $V_{DS}$  waveforms (12 A, 2 kV) @ 25 °C

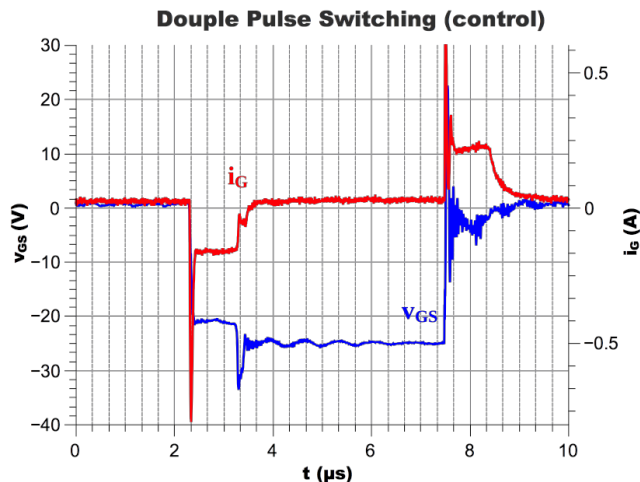


Fig. 10 – Double pulse test measurements,  $i_G$  and  $V_{GS}$  waveforms (12 A, 2 kV) @ 25 °C

## Data Sheet and Safe Operating Area

A data sheet table (Table) was built on the based on the 7 measured components. The Safe Operating Area (SOA) was estimated based on the obtained measurements and following a classical computation procedure [10]. The obtained result is shown in Fig. 11.

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## Summary

3.3 kV Power JFETs have been designed, fabricated and measured in the framework of the FilSiC project. Some satisfying results have been obtained. However, building demonstrators and converters need further devices and require another founding project.

Parameter	Symbol	Conditions	Min	Avr	Max	Units
Drain-source voltage	$V_{DS}$			2000		V
Gate-Source voltage	$V_{GS}$			-20 to 2		V
Continuous drain current	$i_D$	$T_J=150\text{ }^\circ\text{C}$		13		A
Drain-source breakdown voltage	$BV_{DS}$	$V_{GS}=-20\text{ V}$ , $T_J=25\text{ }^\circ\text{C}$ , $i_D=1\text{ mA}$	1950	2650	3300	V
Drain-source on-resistance	$R_{DS}^{ON}$	$V_{GS}=0\text{ V}$ , $T_J=25\text{ }^\circ\text{C}$ , $i_D=5\text{ A}$	0.49	0.52	0.58	$\Omega$
Gate threshold voltage	$V_{TH}$	$V_{DS}=20\text{ V}$ , $i_D=100\text{ mA}$	-18.5	-18	-17.2	V
Input capacitance	$C_{ISS}$	$V_{GS}=-20\text{ V}$ , $V_{DS}=100\text{ V}$ , $T_J=25\text{ }^\circ\text{C}$ ,		1470		pF
Output capacitance	$C_{OSS}$			170		pF
Reverse transfer capacitance	$C_{RSS}$			160		pF
Thermal resistance, junction-to-case	$R_{TH}^{JC}$	Estimated		0.26		$^\circ\text{C/W}$

Table 1: Data sheet like synthetic results for the packaged devices.

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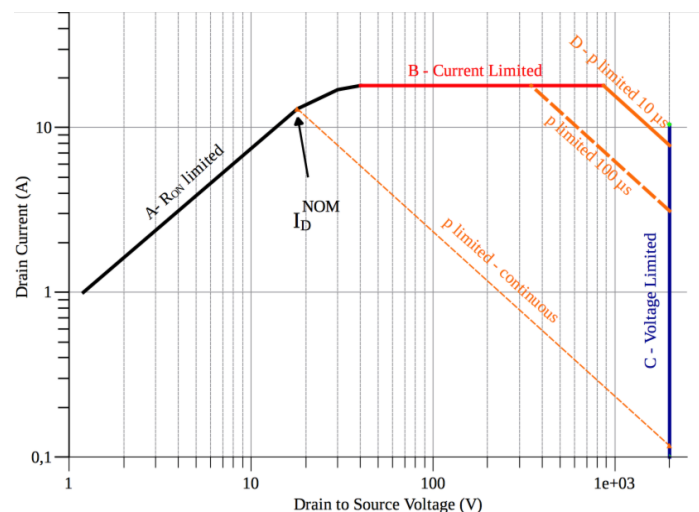


Fig. 11: Estimated Safe Operating Area of the fabricated JFETs