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A Comprehensive Compact Model for the Design of All-Spin-Logic based Circuits

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By relying on pure spin transmission, low-frequency charge-spin conversion, and neuron-like mechanism, All Spin Logic (ASL) has the potential to outperform CMOS technology in logic design and especially in neuromorphic computing, with improved fabrication process and material technology in the future. As ASL technology is gaining in maturity, compact models are needed to fill the gap between application requirements and circuit fabrication. However, defining such a model is a tedious task due to the numerous physical parameters to consider and the need for flexibility to explore design tradeoffs. In this paper, we propose an accurate, generic, scalable, and easy-to-use compact model for ASL devices. The model has been validated by comparing with experimental results, which allows investigating the impact of device characteristics such as channel length and channel width on the propagation delay. The model has been implemented in Cadence using in Verilog-A, which allows running transient simulations and comparing the implementations of 4-bit adder and multiplier circuits regarding the area, energy and delay metrics.

Index Terms—Spintronic, All Spin Logic, circuit design, compact model.

I. INTRODUCTION

SPINTRONIC devices have the potential to lower the power consumption of computing systems and to reach nanometer scales [1]–[3]. Indeed, All Spin Logic (ASL) devices [4]–[7] allow pure spin transmission and low-frequency charge-spin conversions, while CMOS technology relies on pure charge currents only. Moreover, combined with MTJs, the neuron-like mechanism of ASL devices will change the recent neuromorphic computing architectures [8]–[10]. The design of ASL device-based circuits leads to numerous challenges related to the heterogeneity they introduce and the large design space to explore. As the technology is gaining in maturity, compact models are needed to fill the gap between application requirements at the system level and circuit fabrication at the device level. In particular, accurate simulations of spin injection/detection effects are needed to estimate the magnetic tunnel junction (MTJ) [11], [12] switching time and spin diffusion delay according to materials properties. Furthermore, the models should be generic to allow exploring fabrication-related device parameters such as channel lengths and MTJ sizes. Such exploration should allow investigating not only performances tradeoffs [13] but should also help designers to prevent from device damages. For instance, an injection

current that is not properly calibrated can damage graphene [14], [15] (resp. metal)-based channels due to Joule heating (resp. electromigration) effects. Finally, a scalable approach is mandatory to investigate the design of complex, hierarchical circuits. It is worth noticing that, to be adopted by the designer community, the approach should be compliant with current standardized CMOS-based design techniques and should be implemented in an existing commercial environment.

Hence, there is a need for accurate, generic, scalable, and easy-to-use, i.e. comprehensive, compact models. However, to our knowledge, there is no such model in the literature. Indeed, models have been implemented in MatLab to execute transformed conductance matrix [16]. These approaches are not scalable and cannot be used for complex circuits design. Verilog-A model proposed in [17] implements ASL device as a single block, which avoids exploring the design space for its optimization and the hierarchical design. A circuit simulation environment relying on basic electrical circuit elements such as resistors, capacitors and current sources has been defined in [18] [19], and a scalable Verilog-A model is proposed in [20]. Both approaches do not integrate important characteristics such as spin diffusion delay and channel breakdown effects.

The following summarizes the contributions of the paper:

- Comprehensive ASL device compact model taking into account spin-transfer torque effect [21], spin diffusion delay [22], channel breakdown effect [23]–[27]. and the scaling effects [28].
- IP block-like organization of the model, which allows the independent design of injector, detector, channel and contact devices. This allows cross-layer optimization of ASL-based circuits and eases the design of hierarchical, complex circuits.

This paper is organized as follows. Section II introduces the ASL device-based circuit fundamental and related work. Section III presents the proposed compact model, which has been implemented in Cadence using Verilog-A. In Section IV, we investigate the design of hierarchical 4-bit adders and multipliers circuits. In Section V, we validate the model through comparisons with experimental results and Cadence simulations are carried to compare implementations. Section VI concludes the paper and gives perspectives to this work.

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TABLE I
ASL COMPACT MODELING COMPARISON.

Integrated effect	Srinivasan [16]	Bonhomme [18]	Calayir [20]	Verma [19]	Su [17], [23]	Our model
Language/software	MatLab	Circuit simulator	Verilog-A	OOMMF TCL	Verilog-A/Cadence	Verilog-A/Cadence
Scalability	low	low	high	low	little	high
Module	separated conduction matrix	separated electrical circuit element	separated conduction block	separated conduction block	one block	separated conduction block
STT effect	coupled with LLG equation (in-plan)	coupled with LLG equation	coupled with LLG equation (perpendicular)	coupled with LLG equation (perpendicular)	integrated the static and dynamic switching expressions (perpendicular)	integrated the static and dynamic switching expressions (perpendicular)
Channel breakdown effect	×	×	×	×	✓	✓
Channel diffusion time	×	×	×	✓	×	✓
Spin relaxation in FM	×	×	✓	×	×	✓
Fundamental theory	[32]	[31]	[32]	[32]	[31]	[31]

- Injector and detector:

$$I_F(0) = \frac{\pi W L_{Fi}}{4\rho_{Fi} t_{Fi}} \Delta\mu + \frac{\pi P_{Fi} W L_{Fi}}{4\rho_{Fi} L_{sFi}} \mu_{sFi}(0) \quad (1)$$

$$I_{sF}(0) = \frac{\pi P_{Fi} W L_{Fi}}{4\rho_{Fi} t_{Fi}} \Delta\mu + \frac{P_{Fi}^2 \pi W L_{Fi}}{4\rho_{Fi} L_{sFi}} \mu_{sFi}(0) \quad (2)$$

where W is the MTJ width, P_{Fi} is the ferromagnet spin conductivity polarization and t_{Fi} is the free layer thickness.

- Contacts:

$$I_{Ci} = \frac{\pi W L_{Fi}}{8RA_{Ci}} \Delta\mu + P_{Ci} \cdot \frac{\pi W L_{Fi}}{8RA_{Ci}} \Delta\mu_s \quad (3)$$

$$I_{sCi} = P_{Ci} \cdot \frac{\pi W L_{Fi}}{8RA_{Ci}} \Delta\mu + \frac{\pi W L_{Fi}}{8RA_{Ci}} \Delta\mu_s \quad (4)$$

where P_{Ci} is the spin resistance polarization of the contact and RA_{Ci} is the resistance area product of the contact. We assume two types of contacts: i) a simple FM-N contact with no material between the ferromagnet and the channel and ii) a more complex contact involving a Tunnel Barrier (TB) to improve the spin injection efficiency.

- Channel:

$$I_N = \frac{W t_N}{\rho_N L_N} \Delta\mu \quad (5)$$

$$I_{sN}(0/L_N) = \frac{W t_N}{\rho_N L_{sN}} \left[\frac{\mu_{sN}(L_N) - \mu_{sN}(0)}{\sinh(L_N/L_{sN})} \mp \frac{(\cosh(L_N/L_{sN}) - 1)\mu_{sN}(L_N)}{\sinh(L_N/L_{sN})} \right] \quad (6)$$

where L_N is the channel length.

- Ground:

$$I_G = \frac{L_{Fi} t_G}{2\rho_G L_G} \Delta\mu \quad (7)$$

$$I_{sG} = \frac{L_{Fi} t_G}{2\rho_G L_{sG}} \mu_{sG}(0) \quad (8)$$

b) Channel breakdown and diffusion delay:

- The average transit time of carriers through the interconnect proposed in [22] [37] is defined as:

$$t_{DIFF} = \frac{L_N^2}{2D} + \frac{L_N}{v_f} \quad (9)$$

where $L_N^2/2D$ is the diffusive time constant and L_N/v_f is the ballistic time constant. D is the electron diffusion coefficient, and v_f is the Fermi velocity of electrons.

- A channel is characterized by a breakdown current density J_{BD} . It corresponds to an upper limit a current density should not exceed to avoid channel destruction or malfunction. As detailed in [23]–[27], the physical phenomenon induced by the breakdown current depends on the channel material:

- For a metal material, a large current density leads to a high electromigration, which results in the breakdown of the channel. By considering the copper material, the Blech model [26], [27] allows defining the maximum current density $J_{BR,Cu}$ by:

$$J_{BR,Cu} \times L_N = \frac{\Omega \Delta\sigma}{Z^* e \rho_{Cu}} \quad (10)$$

where Ω , $\Delta\sigma$, Z^* are the atomic volume, normal stress difference between stripe ends and the effective valence of Cu, respectively; ρ is the resistivity and e is the electron charge.

- For semiconductor material, channel breakdown occurs when Joule heating effect leads to a temperature larger than the fusion point. For such a material, the maximum current density is defined by [24], [25]:

$$J_{BR} = \left[\frac{g(T_{BD} - T_0)}{\rho_N t_N W} \times \frac{\cosh(\frac{L_N}{2L_H}) + g L_H R_T \sinh(\frac{L_N}{2L_H})}{\cosh(\frac{L_N}{2L_H}) + g L_H R_T \sinh(\frac{L_N}{2L_H}) - 1} \right]^{1/2} \\ g^{-1} = \left\{ \frac{\pi k_{ox}}{\ln[6(t_{subox}/W + 1)]} + \frac{k_{ox}}{t_{subox}} W \right\}^{-1} \\ + \frac{R_{Cox}}{W} + \frac{1}{2k_{Si}} \left(\frac{L_N}{W + 2t_{subox}} \right)^{1/2} \\ R_T \approx L_{Hm} / [k_m t_m (W + 2L_{Hm})] \\ L_{Hm} = [k_m / (k_{ox} t_m t_{subox})]^{1/2} \quad (11)$$

Where T_{BD} and T_0 are the breakdown and room temperatures respectively; g is the contact thermal resistance per length unit, $L_H = \sqrt{k_g W t_N / g}$ is the thermal healing length, k_g is the thermal conductivity of channel material, k_{ox} and t_{subox} are the

TABLE II
ASL DEVICE PARAMETERS.

	Symbol	Parameter (unit)	Description	Default value	Range
Global		W (nm)	Device width	40	[25,50]
		T_0 (K)	Temperature	300	— ⁴
Injector		$TMR(0)^3$	TMR ratio with 0 V_{bias}	120%	[60,600]%
		α^3	Ferromagnetic damping factor	0.027	[0.007,0.027]
		H_k^3 (A/m)	Ferromagnetic anisotropy field	270×10^3 [11]	X^5
		M_s^3 (A/m)	Ferromagnetic saturation magnetization	1.1×10^6 [11]	X
		ρ_F ($\Omega \cdot m$)	Ferromagnetic resistivity	2.6×10^{-6}	—
		L_{sF} (nm)	Ferromagnetic spin diffusion length	0.2	—
Detector		P_F	Ferromagnetic spin polarization	0.5	[0,0.99]
		State	MTJ state representation	“0” (P) “1” (AP)	—
		L_F (nm)	MTJ length	40	[25,50]
		t_{ox}^3 (nm)	MTJ Oxide barrier height	0.85	[0.8,1.5]
		t_F (nm)	MTJ free layer height	1.3	—
		RA_F^3 ($\Omega\mu m^2$)	MTJ resistance area product	5	[5,15]
Contact		$Type_C$	Contact type selection	1 (with TB) 0 (without TB)	1, 0
		P_C	Contact spin resistance polarization	0.5	[0,0.99]
		RA_C ($\Omega\mu m^2$)	Contact resistance area product	100 (with TB) 8.79×10^{-4} (without TB)	X
Ground		L_G (μm)	Ground length	1	$\geq L_{sN}$
		t_m^1 (nm)	Metal electrode thickness	5 [24]	X
		k_m^1 ($Wm^{-1}K^{-1}$)	Metal electrode thermal conductivity	22 [24]	X
		k_{Si}^1 ($Wm^{-1}K^{-1}$)	Thermal conductivity of the highly doped Si substrate	100 [24]	—
		t_{subox}^1 (nm)	Substrate thickness	90 (SiO_2) [24]	X
		k_{ox}^1 ($Wm^{-1}K^{-1}$)	Substrate thermal conductivity	1.4 (SiO_2) [24]	—
		R_{Cox}^1 (m^2KW^{-1})	G/N-substrate interface thermal contact resistance	1×10^{-8} [24]	X
Channel		T_{BD}^1 (K)	G/N material breakdown temperature	875 [24]	X
		k_g^1 ($Wm^{-1}K^{-1}$)	G/N material thermal conductivity	100 (graphene) [24], [34]	X
		v_f^2 (m/s)	G/N material fermi velocity of electrons	0.8M (graphene)	X
		D^2 (m^2/s)	G/N material electron diffusion coefficient	0.02 (graphene)	X
		$t_{G/N}^3$ (nm)	G/N material thickness	“1” (graphene) ⁶	X
		$\rho_{G/N}$ (Ω^6)	G/N material resistivity	2.86×10^3 (graphene) ⁶	X
		$L_{sG/N}$ (μm)	G/N material spin diffusion length	1	X
		$Type_{G/N}$	G/N material selection	1 (semi), 0 (metal)	1, 0
		$\frac{\Omega\Delta\sigma}{Z^*e}$ (ΩA)	Metal G/N breakdown current density calculation factor	5.1×10^{-4} (copper) [23]	X
		L_N (nm)	Channel length	90	[$L_{dipolar}$, ⁷ $0.8L_{sN}$]

¹ Parameters used to calculate the breakdown current density for semiconductor material.

² Parameters used to calculate the spin diffusion time.

³ Parameters used to calculate MTJ spin transfer torque and TMR effects.

⁴ Parameters are fixed in this model.

⁵ Parameters depend on the material.

⁶ The unit of the graphene resistivity is [Ω] and the graphene resistance is calculated as $R = \rho_N \times \frac{L_N}{W}$ instead of $R = \rho_N \times \frac{L_N}{W \times t_N}$. We thus arbitrary set the graphene thickness to “1”. The resistivity unit of other materials is [Ωm]; the material thickness is thus set to the actual one.

⁷ $L_{dipolar}$ is the minimum value of the channel length considering the dipolar coupling between two magnets. It can be simulated by several softwares, such as OOMMF [35] [36].

thermal conductivity and thickness of the substrate, respectively; R_{Cox} is the contact thermal resistance between channel and substrate, K_{Si} is the thermal conductivity of the highly doped Si substrate, R_T is the contact thermal conductance, L_{Hm} is the thermal healing length of heat spreading into the contact, k_m and t_m are the thermal conductivity and thickness of the metal electrodes.

B. Verilog-A Implementation

The compact model has been implemented in Cadence using Verilog-A. Table II represents the 5 symbols corresponding to the following ASL devices and their parameters: *Injector* and *Detector*, contacts C_{TB} and C_{FM-N} (Tunnel barrier and FM-N interface), ground lead G and channel N . Each block

describes the current-voltage relations of the device, based on the equations previously described. *Injector* and *Detector* also take into account the spin torque switching effect and N integrates the spin diffusion and channel breakdown effects. The following details the 5 blocks:

- “*Injector*” integrates a resistance tunneling model, a STT model and a spin injection model. The state of an MTJ depends on the voltage source V_{write} connected to terminals “T1” and “T2”. The MTJ state is output on terminal S_{in} , taking into account the switching delay. The output is represented as a voltage signal: “V=0V” and “V=1V” correspond to parallel and anti-parallel state respectively. Once the MTJ state has been configured, an injection current I_{inj} is injected into the channel from the MTJ free layer through the terminal “ I_{inj} ”. This leads to

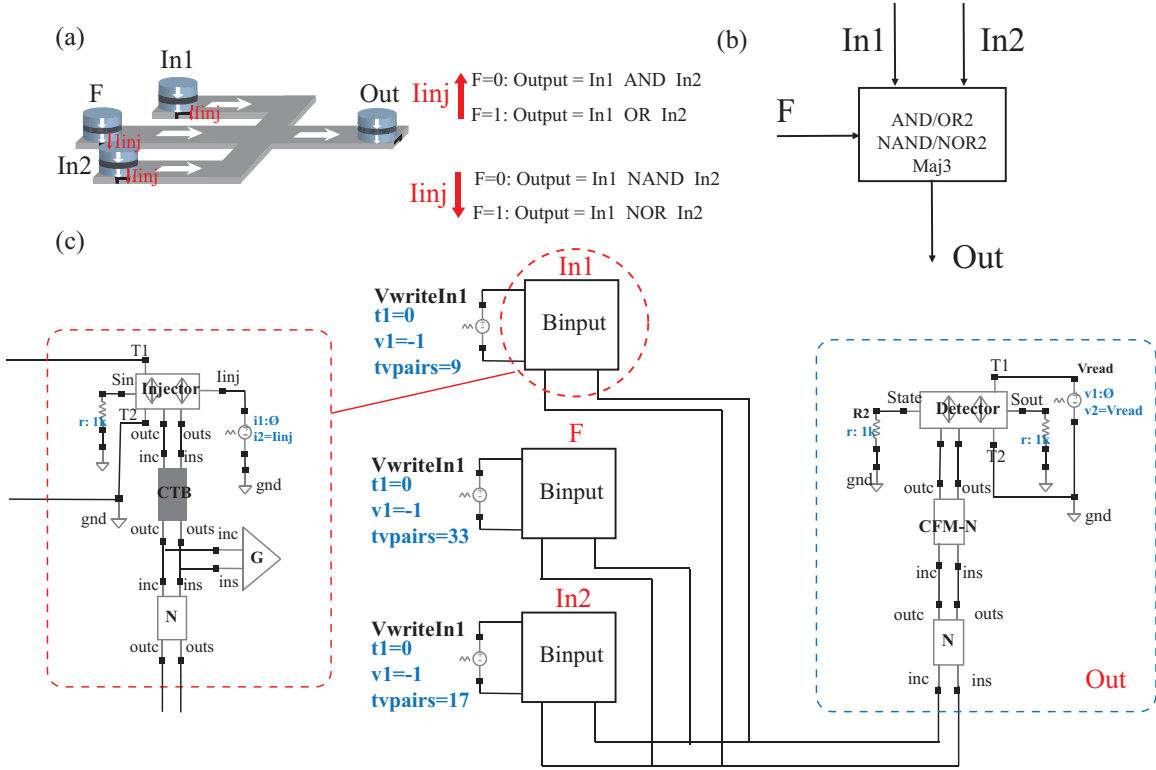


Fig. 2. (a) 3-input majority gate architecture: $In1$ and $In2$ as inputs, F as control terminal, Out as output. (b) Functional symbol of the 3-input majority gate. (c) Implementation in Cadence of ASL-based 3-input majority gate. $Injector/Detector$ are the input/output ferromagnet/MTJ blocks; CTB and $CFM-N$ are contact block with and without tunnel barrier respectively; G is ground lead block; N is channel block.

a charge current “ $outc$ ” and a spin current “ $outs$ ”.

- “ C ” corresponds to the contact model, which can be implemented with or without tunnel barrier (TB). The two input terminals “ inc ” and “ ins ” represent the input charge and spin currents. Terminals “ $outc$ ” and “ $outs$ ” represent the output charge and spin currents.
- “ G ” and “ N ” correspond to the ground and channel model respectively. Part of the charge and spin currents outputted by the contact flows into the ground while the remaining part flows into the channel, where it will propagate until reaching a detector.
- “ $Detector$ ” corresponds to block able to switch a MTJ state according to the current flowing through a contact. Above a threshold current, the “ $State$ ” terminal is switched to 1V (parallel) or 0V (anti-parallel) depending on the injection current polarity and the MTJ state input. The state can be read by applying a voltage source “ V_{read} ” to terminals “ $T1$ ” and “ $T2$ ” and is output to “ S_{out} ” terminal.

Fig. 2 illustrates a 3-input majority gate and its implementation in Cadence. It is composed of 2 input terminals to input data ($In1$ and $In2$), 1 control terminal (F), 1 output terminal (Out) and 4 channels. We assume a same channel length $L1$ between the channel crossing and the inputs. A length $L2$ characterizes the channel linking the crossing to the output MTJs. Depending on the state of F and the injection current polarity, AND/OR/NAND/NOR2 function is configured.

Obviously, the implementation in Cadence follows the same structure: the MTJs and the channels are represented by 4

components; CTB , $CFM-N$ and G correspond to the contact and the ground respectively. Each component is configured according to various parameters (e.g. channel lengths and injection currents). From such a model, one can design hierarchical circuits, run the simulation, and explore design parameters, as it will be shown in the result section.

IV. HIERARCHICAL CIRCUIT DESIGN

The aim of the proposed model is to allow designing realistic, hierarchical, ASL devices-based circuits. In this section, we investigate the design of two 4-bit adders and a 4-bit multiplier. Adders and multipliers play an important role in today’s digital signal processing and many other applications. Since they are designed according to multiple objectives (latency, power, layout regularity and area), it is important to explore the design space by taking into account physical properties of the devices.

A. 4-bit Adder

We investigate serial and parallel implementations described in the following. For both circuits, the operands are $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$.

1) Serial adder

The serial adder is implemented by cascading full-adders [38] (Fig. 3 (a)). A full adder requires to sum-up the spin current injected from three MTJs (A , B and C_{in}), which is achieved using the same channel crossing structure described for the 3-inputs majority gate (i.e. 4 channels are needed).

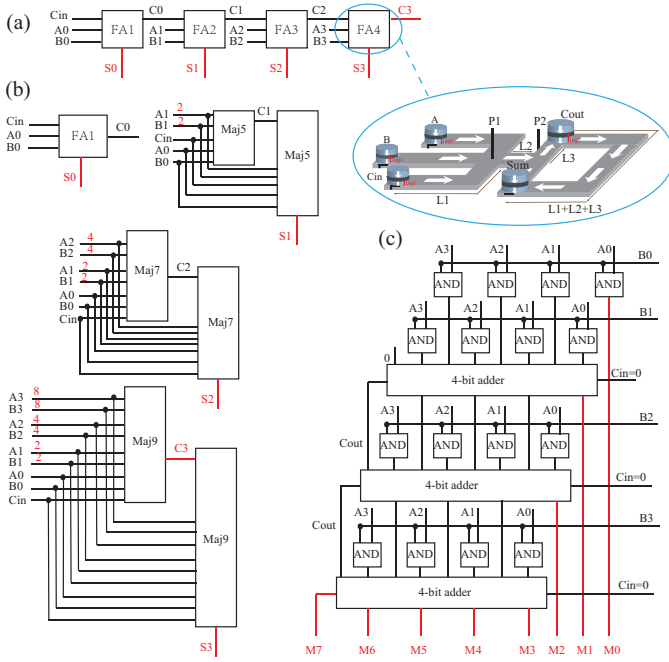


Fig. 3. (a) serial adder, (b) parallel adder and (c) multiplier. For the parallel adder, numbers on red correspond to the weights.

The resulting spin current then diffuses toward C_{out} and Sum MTJs: since C_{out} result is required to compute Sum , a fifth channel connects both MTJs. The length of this channel is $L3$.

Fig. 3 (a) illustrates the serial adder. The carry-out from a stage propagates to the next stage, hence introducing a delay in the computation. The total delay of the circuit is the sum of 4 contributions: i) the MTJ state writing time ($\times 1$ since all the inputs are injected simultaneously), ii) the time needed to change the state of intermediate signals ($\times 5$ on the critical path which includes 4 carry signals and 1 sum) and iii) the MTJ state reading time ($\times 1$ since all the results are read simultaneously). The implementation of the serial adder requires 20 MTJs.

2) Parallel adder

Replacement and duplication method leads to a parallel implementation of the adder. Compared to the serial adder, the parallel adder is expected to reduce the latency at the cost of extra resources and energy. For its implementation, input carry C_{i-1} of stage i is replaced with its primary inputs $A_{0/\dots/i-1}, B_{0/\dots/i-1}$ and the weights of the original inputs of this stage A_i, B_i are duplicated. Eq. 12 shows an example for C_1 .

$$\begin{aligned} C_1 &= Maj(A_1, B_1, C_0) \\ &= Maj(A_1, B_1, A_1, B_1, A_0, B_0, C_{in}) \end{aligned} \quad (12)$$

The number of inputs increases with the stage as follow: both C_i and S_i require $2^i A_i/B_i$, $2^{i-1} A_{i-1}/B_{i-1}$ and so on. As illustrated in Fig. 3 (b), the parallel adder is implemented using 3/5/7/9-inputs majority gates. Compared to the serial adder, the delay of the parallel adder is expected to decrease since there is no carry propagation. Indeed, in addition to MTJ state writing time ($\times 1$) and reading time ($\times 1$), critical path

delay includes the time to change the state carry signal ($\times 1$) and sum signal ($\times 1$).

B. 4-bit Multiplier

The considered 4-bit multiplier is illustrated in Fig. 3 (c). $A = A_3A_2A_1A_0$ and $B = B_3B_2B_1B_0$ are the multiplicator and the multiplicand respectively. A classical array structure is used: the first stage is the multiplication of A_i and $B_{0/1}$; results are transmitted to the second stage, where additions occur, etc. The multiplier is implemented using 16 AND gates (each AND gate corresponds to a 3-inputs majority gate configured for AND function) and three 4-bit adders, for which serial and parallel implementations are possible. The multiplier is thus a hierarchical circuit for which multiple design options are possible. In the results section, we will investigate delay-area design tradeoffs.

V. SIMULATION RESULTS

A. Model Validation

The STT and TMR effects integrated in this model are validated in [21]. For the spin injection/detection model we develop in this paper, in order to setup the simulation environment, we first tune the compact model in order to match with characterization results. For this purpose, we simulate the spin resistance ΔR_s , for which experimental data have been reported in the literature for Py/Mg (ferromagnet/channel) [39] and Py/Cu [40] materials. By adjusting the spin polarization to 0.58 (resp. 0.37) and the channel spin diffusion length to 205 nm (resp. 320 nm) for Py/Mg (Cu) material, the simulation results are well aligned with characterization results, as illustrated in Fig. 4.

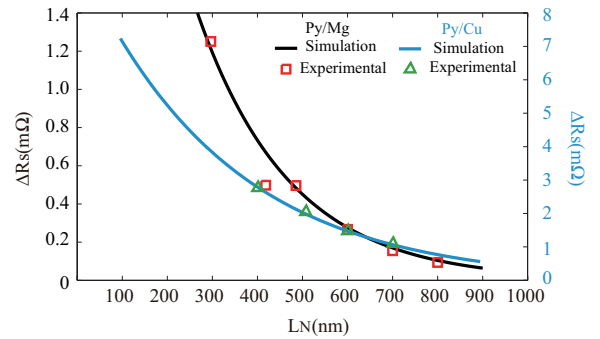


Fig. 4. Simulation and characterization results ΔR_s comparison for channels implemented with Mg and Cu materials.

B. Device Simulation

In the following, device level simulations are carried out in order to estimate the breakdown current and the delay. We assume a graphene channel, which leads to the use of the default values defined in Table II. Fig. 5 reports the estimated breakdown current according to the length and the width of the channel. The area located under a line corresponds to current density values leading to a channel working properly. The area located above a line corresponds to current density values exceeding the breakdown current, which are likely to damage the

channel due to Joule self-heating or electromigration damages effects (for semi-conductor and metal materials respectively). The larger the channel area, the smaller J_{BD} . This is due to the lateral 3D heat spreading into the substrate, the contacts and along the graphene channel. The heat transfer depends on the thermal conductance and hence on its length and width: a small channel length/width leads to high thermal conductance, which contributes to maintaining the heat spreading along the graphene and into the contacts [25]. However, if L_N is too small, a dipolar-coupling effects occurs [35], which reduces the spin current injection and increases the MTJ switching time. Hence, a minimal value for L_N needs to be assumed in order to ensure there is no dipolar coupling. Following the conclusions from the OOMMF [35] [36], we assume the minimum value L_N is $10 + W$ nm.

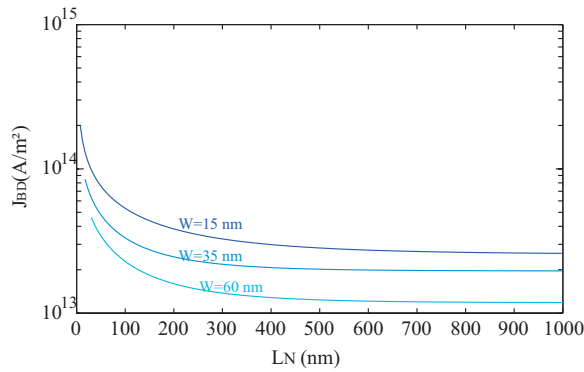


Fig. 5. Channel breakdown current density J_{BD} according to channel length L_N and channel width W .

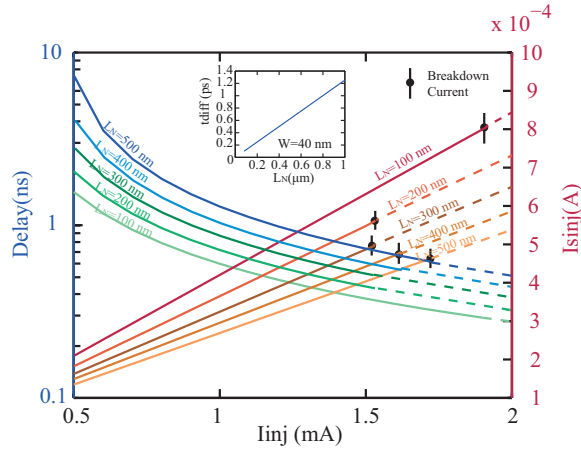


Fig. 6. Delay and channel spin current I_{sinj} according to the injection current I_{inj} and channel lengths L_N . For each channel length, the breakdown current is labeled on I_{sinj} curves. The following defines i) the maximum injection current, ii) the corresponding spin injection current and iii) the delay according to the channel length: (1.9 mA, $803 \mu A$, 0.292 ns) for 100 nm, (1.587 mA, $581 \mu A$, 0.4164 ns) for 200 nm, (1.565 mA, $509 \mu A$, 0.5039 ns) for 300 nm, (1.63 mA, $478 \mu A$, 0.5586 ns) for 400 nm, (1.72 mA, $463 \mu A$, 0.6108 ns) for 500 nm. Inset gives the spin diffusion delay t_{diff} according to L_N .

In the following, we assume the ASL device illustrated in Fig. 1 (a) and we investigate the impact of the injection current I_{inj} and the channel length L_N on the delay. Fig. 6 gives the evolution of the delay for I_{inj} ranging from

0.5 mA to 2 mA. As an example, for a 500 nm channel length, the delay decreases from 7.3 ns for $I_{inj} = 0.5$ mA to 1.27 ns for $I_{inj} = 1$ mA. We also plot the spin current I_{sinj} injected to a channel according to I_{inj} . The plain line corresponds to injection current value respecting the breakdown current constraints while dashed line represents cases for which channel is likely to be damaged. For instance, for $L_N = 100$ nm, the breakdown current is estimated to be $803 \mu A$, which corresponds to a maximum value of 1.9 mA for I_{inj} . The inset represents the spin diffusion delay t_{diff} according to L_N and for $W = 40$ nm. Results show that t_{diff} approximates 1 ps range, which can be neglected considering to the MTJ switching delay (100 ps to few ns for $W = 40$ nm). It is worth noticing that the diffusion delay is expected to play a significant role in the total delay as MTJ fabrication technology will gain in maturity.

In the following, we investigate the impact of the channel length on the delay of the 3-input majority gate illustrated in Fig. 2 (a). We define $L1$ (resp. $L2$) as the distance between the injector and the channel crossing (resp. the distance between the channel crossing and the detector). We consider $I_{inj} = 700 \mu A$, which allows keeping the current density below the breakdown current for the total channel sizes we assume (100 nm, 200 nm and 300 nm). As illustrated in Fig. 7, the delay decreases while $L1$ increases, which is due to the fact that the backflow current (e.g. current coming from $In1$ and going to $In2$ at the crossing point) decreases as $L1$ channel resistance increases. Hence, for a 3-input majority gate, the optimal solution is obtained for $L2 = 0$. From a layout point of view, this can be easily implemented by implementing the crossing structure below the detector. However, such a layout is not possible for more complex devices such as a 5-inputs majority gate, which can thus be optimized using channel length exploration.

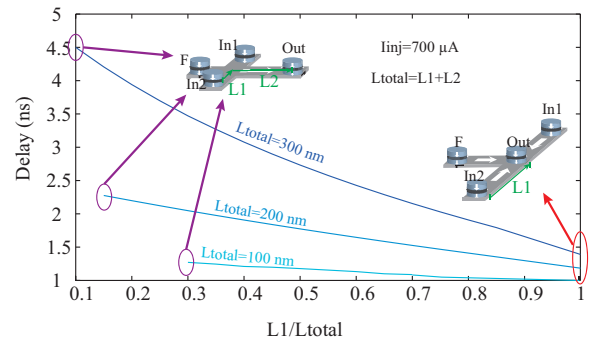


Fig. 7. Propagation delay (including switching and spin diffusion delays) for a 3-input majority gate.

C. Circuit Simulation

Based on the developed compact model, we use Cadence to run transient simulations for 4-bit adder and multiplier circuits. We consider 40 nm MTJs and 1 μm for the channel spin diffusion length. Regarding the 3-input majority gate illustrated in Fig. 2 (resp. Full-Adder illustrated in Fig. 3), we assume $L1 = 70$ nm and $L2 = 30$ nm (resp. $L1 = 50$ nm, $L2 = L3 = 25$ nm).

1) 3-input majority gate

Fig. 8 illustrates the simulation results of the 3-input majority gate considering $I_{inj} = 700 \mu A$. Simulation results validate the functional behaviors of the 3-input majority gates, which can implement the AND/OR/NAND/NOR functions depending on i) the state of the control terminal F and ii) the injection current polarities. The average delay of this gate is 0.9 ns.

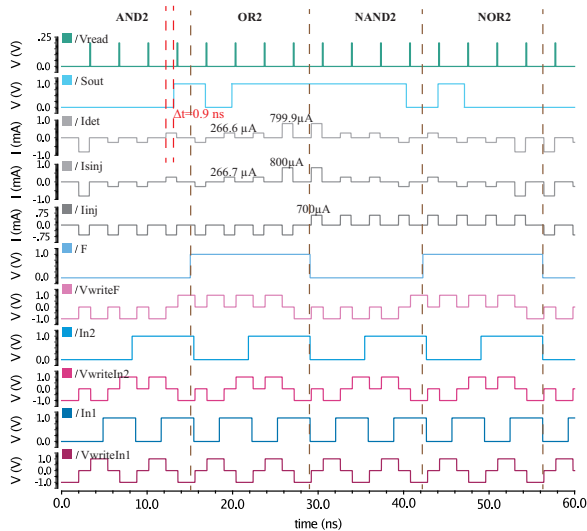


Fig. 8. Simulation results for a 3-input majority gate. V_{writei} is the MTJ write voltage source for the i terminal; $In1/In2/F$ are injector input terminals; I_{inj} is the injection current for all the input terminals; I_{sinj} is the spin current on the injector side; I_{det} is the spin current on the detector side; $Sout$ is the gate output state; V_{read} is the voltage source applied to the detector to read the state of the MTJ.

2) 4-bit adders

For the serial adder, we first set the injection current I_{inj1} to 1.07 mA, which leads to the maximum spin current allowed in the channel. Then, considering the length of the channels and the weights needed to compute Sum (the weight of C_{out} is twice the weight of A , B and C_{in}), I_{inj2} is set to 973 μA . We assume two values for the ferromagnetic damping factor: $\alpha = 0.027$ relies on a conservative technology while $\alpha = 0.007$ is a more aggressive technology leading to a lower MTJ threshold current. As reported in Table III, we obtain 13.1 ns (resp. 9.63 ns) for the average delay and 3.2 nJ (resp. 2.35 nJ) for the energy consumption for a conservative (resp. aggressive) technology. It is worth noticing that a design space exploration (e.g. on the channel lengths, device width) could be carried out to improve the performance of the circuit.

The same approach has been followed for the parallel adder. For $\alpha = 0.027$, the spin current received by the detector is too small to switch the MTJ state. Since a higher injection current will damage the channel, this circuit implementation is not realistic for a conservative technology. When implemented with a more aggressive ferromagnetic damping factor, the spin current can be detected, which leads to 5.8 ns delay and 3.3 nJ energy consumption (see Table III). Traditional design tradeoffs relying on area, power and delay can thus be investigated to compare serial and parallel implementations.

TABLE III
ADDERS AND MULTIPLIERS PERFORMANCE COMPARISON.

Circuit		Area (μm^2)	$\alpha = 0.027$		$\alpha = 0.007$	
			Energy (nJ)	Delay (ns)	Energy (nJ)	Delay (ns)
4-bit adder	Serial	0.32	3.2	13.1	2.35	9.63
	Parallel	0.84	N/A	N/A	3.3	5.8
4-bit Multiplier	Serial	1.6	11.1	39.8	8.35	29.3
	Parallel	3.16	N/A	N/A	11.2	17.8

3) 4-bit multiplier

In order to illustrate the **high scalability** of our model, we design and simulate 4-bit array multipliers relying on serial and parallel adders. Fig. 9 illustrates a simulation result and Table III summarizes the area, energy and delay for conservative and aggressive parameters. We conclude from this study that our model not only allows comparing circuits but also helps to identify, early in the design process, the limits induced by a given technology.

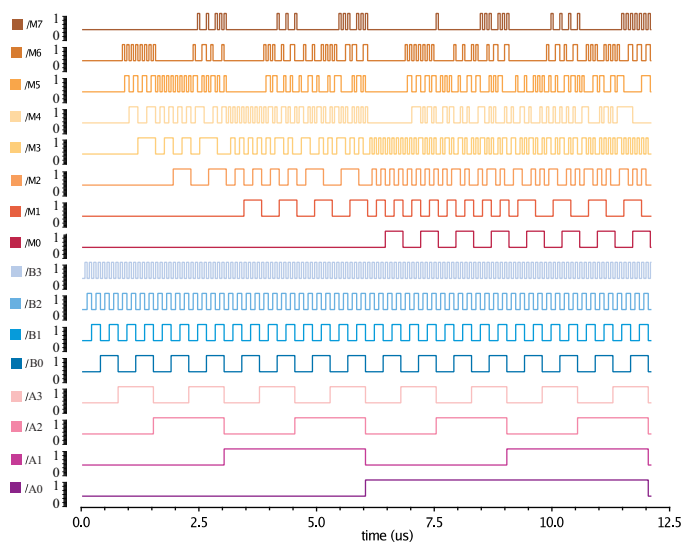


Fig. 9. Simulation results of a 4-bit array multiplier with serial adders. $A_3 \dots A_0$ and $B_3 \dots B_0$ are the operands; $M_7 \dots M_0$ are the outputs.

VI. CONCLUSION

In this paper, we propose a comprehensive compact model for ASL devices. The model relies on extended Maxwell's equations in the spin domain and allows taking into account both spin diffusion delay and channel current density breakdown. After validating the model by comparing with experimental results, we have investigated the impact of device characteristics such as channel length and channel width on the propagation delay. Furthermore, the model has been implemented with Verilog-A in Cadence, which allows running transient simulations and comparing the implementations of the 4-bit adders and multipliers circuits regarding the area, energy and delay metrics. In our future work, we will investigate design space exploration to optimize the circuits performances.

ACKNOWLEDGMENT

This paper is supported by the China Scholarship Council (CSC).

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STATEMENT TO REVIEWERS

Dear Editor,

We would like to thank editors and reviewers for their efforts and time on our manuscript. We really appreciate all the comments to improve the quality of our manuscript. We have considered all the questions and comments of reviewers in detail, and prepared a revised version of the manuscript that takes them carefully into consideration. These changes appear in blue in the revised manuscript so as to be located easily. Please find below our point-by-point responses to the reviewers' comments.

Sincerely,

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Response to the Comments of the Reviewer 1

1. Authors should highlight important contributions of their model and difference between the two basic approaches, i.e. [25] and [26]. The table given seems insufficient. The contribution of the authors seem to be insufficient.

Based on the summarization of the contributions in Section Introduction, firstly we present the fundamental equations of different modules and their Verilog-A implementations in Section III, which allows the independent design of different ASL devices. This is illustrated with the examples of a 4-bit adder and a 4-bit multiplier in Section IV. The effects of the spin diffusion delay, the channel breakdown and the scaling are demonstrated in Section V, with simulations of certain circuits. We have complemented and cleared these contributions in the manuscript. In addition, we have checked the references of different models in Table I.

2. Can the authors explain if the two approaches in [25] and [26] end up at the same result. Since they are derived from the same concept of spin diffusion.

Even though both these approaches are derived from the same concept, with different assumptions of boundary conditions and calculation methods, the results will be a little different. Our model uses the approach in [31] (original [25]), since we can easily deduced different modules based on the Kirchoff's Potential and Flow laws (KPL and KFL) with this approach.

[31] I. Zutic, J. Fabian, and S. Das Sarma, "Spintronics: Fundamentals and applications," *Rev. Mod. Phys.*, vol. 76, pp. 323410, Apr 2004.

3. Do we need MTJ only at the inputs. The intermediate inputs do not need an MTJ. Also if the control input in majority gate MTJ is not needed. A nano-magnet injector is sufficient.

Yes, you are right. In a simple logic circuit, a nano-magnet injector is sufficient, instead of MTJ, considering the energy consumption and the delay. However, in a large-scale circuit, MTJs are necessary for the interconnection like the latch. Also for the control input, if we want to use ASL in programmable/reconfigurable circuits for memory-in-logic computing, the MTJ is necessary. Furthermore, ASL-based circuits can also be used in neuromorphic circuits, where MTJs are needed.

4. What about the simulation time and convergence of the two approaches.

If I did not misunderstand, you mean the two approached in Table I. We have used MatLab to program these two approaches. We found that the simulation time of the two approaches were basically the same, in the case of a 4-bit adder. We think the comparison of the simulation time should be further done with a much larger circuit or system, like a neuromorphic circuit. The approach in ref[32] may

not converge in some cases, and we should properly set the injection current. The problem will be further studied for the approach in ref [31].

[31] I. Zutic, J. Fabian, and S. Das Sarma, "Spintronics: Fundamentals and applications," *Rev. Mod. Phys.*, vol. 76, pp. 323410, Apr 2004.

[32] A. Brataas, G. E. Bauer, and P. J. Kelly, "Non-collinear magnetoelectronics." *Physics Reports*, vol. 427, no. 4, pp. 157255, 2006

5. I would suggest that instead of MTJ an spin valve should be used as input interface if the supply tunnel interfaces are used (since corresponding supply voltage can be sufficiently reduced).

Thank you for your suggestions. To reduce the supply voltage, the energy and the switching delay, indeed a spin valve should be used instead of MTJ. However, in large-scale circuits, MTJ is necessary for the interconnections, like the latch. Furthermore, considering the applications of the memory-in-logic computing and the neuromorphic system, MTJ is used as the data storage memory and the weight memory.

6. Authors should also mention other contributions (in table I) as well that have the same concept as [25] but the approach is different .Some are as follows:

Shivam Verma, M. Satyanarayana Murthy, and Brajesh Kumar Kaushik, All Spin Logic (ASL): A Micromagnetic Perspective, *IEEE Trans. on Magnetics*, vol. 51, no. 10, pp. 3400710-13400710-7, 2015.

Cheng Li , Li Cai, Sen Wang, Xiaokuo Yang, Huanqing Cui, Bo Wei, Danna Dong, Chuang Li, Jiahao Liu, and Baojun Liu, Performance Optimization of All-Spin Logic Device Based on Silver Interconnects and Asymmetric Tunneling Layer, *IEEE Trans. on Magnetics*, vol. 54, no. 7, 2018.

Thank you for showing us these two articles. The first one is very helpful to understand the switching principle and the related parameters. It adopts the model of paper [16] and adds the STT-effect and the channel diffusion time. We added this paper in our comparison table. The second paper focused on the performance improvement of ASL device. We added it as a reference paper to demonstrate the need for a high-scalable model.

[16] S. Srinivasan, V. Diep, B. Behin-Aein, A. Sarkar, S. Datta, D. Awschalom, J. Nitta, and Y. Xu, "Modeling multi-magnet networks interacting via spin currents," arXiv preprint arXiv:1304.0742, 2013.

7. There are several typos and writing also needs improvement.

We have carefully re-checked the whole manuscript and corrected several typos.

Response to the Comments of the Reviewers 2

This paper proposes an accurate generic, scalable and easy-to-use compact model for ASL devices, aslo gives the essential physical parameters to explore design tradeoff, which is meaningful for ASL technology. This paper is well-organized and informative, however, there are still some suggestions to improve it.

Thank you for all the comments to improve this article. We have seriously considered all the comments for the references and the model scaling. We have checked all the references you mentioned and added all the references you suggested. Furthermore, we have complemented our article with the scaling effect considered in our model, and checked the whole manuscript carefully.

Firstly, there are some incorrect references used in this paper, such as the fundamental theory of ASL model, ref[26] has not been published formally, since we have already the same publication as following, "I. uti, J. Fabian, S. Das Sarma, Spintronics: Fundamentals and applications, *Rev. Mod. Phys.* 76 (2004) 323410. doi:10.1103/RevModPhys.76.323.", which is mentioned in the your ref[13]. Thus in your Table I, it is should be the above reference for Su's model instead of your ref[25]. Please check the refences correctly for your comparsion in the Table, which should be mentioned in their papers at least. Besides, the evaluation of the scalability of Su's model lacks of accuracy, that is possible with low or medium.

We have modified the original ref[26] to ref[31], as you suggested. Furthermore, we have carefully checked all the references for different models in the Table I, and modified them. The evaluation of the scalability of Su's model has been changed to "little", because it can only be used for a standard ASL model with one input, one channel and one output except modifying different parameters.

[31] I. Zutic, J. Fabian, and S. Das Sarma, "Spintronics: Fundamentals and applications," *Rev. Mod. Phys.*, vol. 76, pp. 323410, Apr 2004.

Second, with the correct refence, the equations (1)(2) are familiar to the reader and it is not used in your compact model, and it could be deleted in this part. It is enough to give the equations that containd in your Table II for the device model. Furthermore, besides of breakdown mechism, scaling effects on ASL has been investigated by Chang(S.-C. Chang, N. Kani, S. Manipatruni, D. Nikonov, I. Young, A. Naeemi, Scaling Limits on All-spin Logic, *IEEE Trans. Magn.* 9464 (2016) 11. doi:10.1109/TMAG.2016.2518702.) The authors have been considered that in your model or it is possible to be reflected that?

The equations (1) and (2) are necessary and the fundamentals of the equations in the Table II. So in the manuscript, we give the ref[33] in case readers want to look at in detail.

We have considered all the scaling effects mentioned by Chang. i) the dipole interaction limits the channel length and

we give the minimum channel length in Table II and the calculation in Section V.B; ii) to lower the influence of the leakage current, one method is to use an input terminal with a tunnel barrier and an output terminal without a tunnel barrier, since an adding tunnel barrier will enhance the spin injection, at the same time, will impede the leakage current. In our model, we have defined two different contact modules: with and without tunnel barrier, to allow different designs; iii) our model is based on the Kirchhoffs Potential and Flow laws. We consider the problem of shunt path as a problem of resistance difference. To lower this influence, the resistance (real and spin) of the ground should be larger than that of the channel. With separate “ground” and “channel” models, one can define different parameters for each model to evaluate this influence.

[33] J. Fabian and I. Zutic, “The standard model of spin injection,” arXiv preprint arXiv:0903.2500, 2009.

Lastly, the following references are necessary to be added, which is strongly related to this work, for example, compact model of reconfigurable spin logic.

H. Zhang, W. Kang, L. Wang, K. L. Wang and W. Zhao, “Stateful Reconfigurable Logic via a Single-Voltage-Gated Spin Hall-Effect Driven Magnetic Tunnel Junction in a Spintronic Memory,” in *IEEE Transactions on Electron Devices*, vol. 64, no. 10, pp. 4295-4301, Oct. 2017.

W. Kang, Y. Ran, Y. Zhang, W. Lv and W. Zhao, “Modeling and Exploration of the Voltage-Controlled Magnetic Anisotropy Effect for the Next-Generation Low-Power and High-Speed MRAM Applications,” in *IEEE Transactions on Nanotechnology*, vol. 16, no. 3, pp. 387-395, May 2017.

W. Kang, L. Zhang, J. O. Klein, Y. Zhang, D. R. Ravolosona, and W. Zhao, Reconfigurable Codesign of STT-MRAM under Process Variations in Deeply Scaled Technology, *IEEE Transactions on Electron Devices*, vol. 62, no. 6, pp. 1769-1777, Mar. 2015.

Thank you for giving these paper to improve the manuscript. We have added them in the manuscript.

Response to the Comments of the Reviewers 3

The authors have presented a comprehensive design scheme for ASL-based logic. I however have an issue:

1. All the prior works are based on the theory of non-collinear magnetization (ref[25]) which have been validated with experiments. This work interestingly is based on a different approach (ref[26]). Is this the first work which uses a different approach? The ref.[26] seems to be an arxiv paper, is there a peer-reviewed paper which you can refer to? The argument for using such a different approach needs to be made more explicitly with references drawn to experimental work showing such a different approach is indeed required.

The original ref. [26] has been changed to a published paper [31], which is used before in other articles. Additionally, we have carefully checked all the referenced papers of different models and their approaches, and corrected them in the Table I.

[31] I. Zutic, J. Fabian, and S. Das Sarma, “Spintronics: Fundamentals and applications,” *Rev. Mod. Phys.*, vol. 76, pp. 323410, Apr 2004.

Minor points:

2. The authors have loosely used the term “scalability”. For example, ref. [14] can be used to simulate large-scale circuits.

We have modified our model as “high-scalability” in the text. Since our model can not only allow the independent design of injector, channel, detector, but also integrates different effects, allowing the design of different ASL structures.

3. Fig. 2(c) needs to be clearer

We have modified this figure by replacing the three complex input blocks with one representative block, as shown in Fig. 2(c) now. The caption of this figure is modified accordingly.