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Impact of D-Flip-Flop Architectures and Designs on Single Event Upset Induced by Heavy Ions

L. Artola, G. Hubert, S. Ducret, J. Mekki, Ahmad Al Youssef, and N. Ricard

Abstract— This work highlights the impact of design on the single event upset (SEU) sensitivity of D-Flip-Flops used in a readout circuit (ROIC) under heavy ions. New experimental data obtained at University of Louvain for several designs are presented. The SEE prediction tool MUSCA SEP3 is used to investigate the failure occurrences at the circuit level as a function of the design. In some cases, design specificities allow for increasing in the SEU robustness of the DFF. However, it appeared that cryogenic temperatures limit the impact of the design on the SEU sensitivity of DFFs. The results show a very limited impact of the temperature on the SEU occurrence, independent of the layout. These results are consistent with experimental data presented in recent works regarding SET and SEFI. These results allow for performing irradiation tests of CMOS IR detector (ROIC) at room temperature instead of cooling down the device during the SEE measurements.

Index Terms— Single Event Upset, Flip-Flop, design, architecture, Readout circuit, CMOS, heavy ions

I. INTRODUCTION

THE use of CMOS (Complementary Metal Oxide Semiconductor) functions and their reliability are a major concern for very integrated technologies. CMOS technology is really interesting because it leads to integrate with an image sensor several electronic functions such as a raw decoder, machine state, registers, and D-Flip-Flops (DFF). However, digital CMOS functions of image sensors are known to be sensitive to single event effects (SEE), such as single event transient (SET) and single event upset SEU [1]. SETs can be induced by various ionizing particles, i.e., heavy ions, protons, electrons. SETs and SEU can become critical for image devices and integrated circuits (IC) on-board in flight.

D-Flip-Flops are widely used in digital and computing devices, but are also used in the readout circuit (ROIC) of CMOS image sensors (CIS) as shown in Fig. 1 [2] [3]. DFF are especially used for the digital function for the row counter, column counter and serial register. One of the challenges

during the development process of space CIS is the best trade-

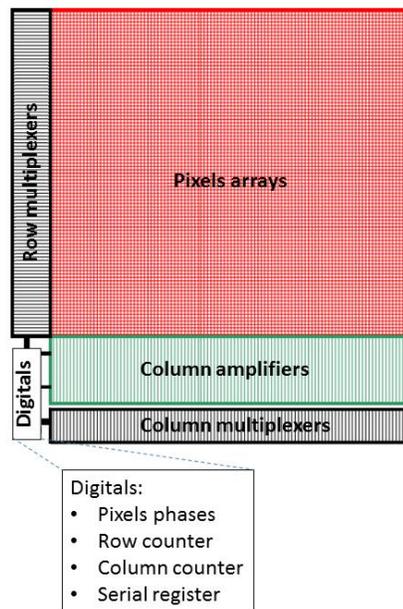


Fig. 1 Simplified schematic of the role of DFF in the digital function of ROIC

TABLE I
D- FLIP FLOPS ARCHITECTURES AND DESIGNS

ARCHITECTURE	DFF DESIGN	Number of n-MOS	Number of p-MOS	cell area norm.)	Input / Output
TEST-CHIP1 CLASSIC	DESIGN 1	17	12	1.04	3 / 2
TEST-CHIP1 CLASSIC	REF.	16	11	1	3 / 1
TEST-CHIP1 CLASSIC	DESIGN 3	17	12	1.1	3 / 2
TEST-CHIP1 CLASSIC	DESIGN 4	16	11	1.07	3 / 1
TEST-CHIP1 COMPLEX	DESIGN 5	21	16	1.83	5 / 2
TEST-CHIP1 COMPLEX	DESIGN 6	20	15	1.79	5 / 1
TEST-CHIP2 COMPLEX	DESIGN 7	21	21	1.59	5 / 2
TEST-CHIP2 COMPLEX	DESIGN 8	21	21	1.66	6 / 2
TEST-CHIP2 COMPLEX	DESIGN 9	19	19	1.52	6 / 1
TEST-CHIP2 COMPLEX	DESIGN 10	20	20	1.62	6 / 2
TEST-CHIP2 COMPLEX	DESIGN 11	19	19	1.59	6 / 1

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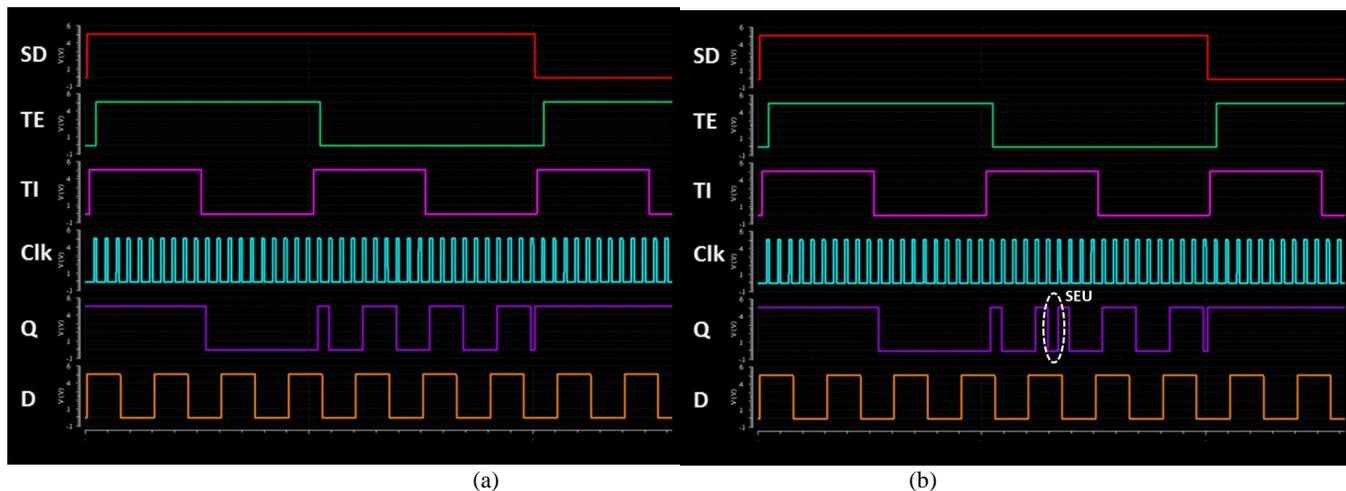


Fig. 2 Input and output signal of DFF6 under (a) its nominal behavior and (b) during a SEU occurrence (circled in white) on the output of the DFF

off between reliability and performance. The design and the architecture of these key digital cells are the main levers of this trade-off [4]. Several works investigated standard DFF, spatially-hardened FF, DICE FF or redundant-FF [5]-[8].

This work presents the impact of the design and the architecture of DFF on the SEU sensitivity under heavy ions at cryogenic temperatures. Table I summarizes the various designs and architectures of the DFFs tested during the irradiation test campaigns. The description of the reference DFF has been presented in L. Artola et al [3]. The differences in the DFFs in terms of designs and architecture are illustrated by the number of n-MOS and p-MOS transistors and the number of inputs and outputs respectively. For confidential reasons, no more details can be provided.

First, the irradiation test setup performed at University Catholic of Louvain (UCL) is presented. Second, the SEU cross sections for each architecture and design are presented and discussed.

In addition, the discussions are completed using a fault injection approach based on SPICE (Simulation Program with Integrated Circuit Emphasis) simulations and the SEE prediction tool, MUSCA SEP3. The soft error prediction tool is based on a Monte-Carlo approach. It performs a full flow of simulations from the interaction of the radiation particles with the device down to the occurrence of SET in the circuit. The circuit response is determined by SPICE simulations. The tool is used to investigate the failure occurrences at the circuit level as a function of the design. Finally, the effects of the supply voltage on the SEU sensitivity trends are analyzed.

II. EXPERIMENT SETUP AND SEU DETECTION IN D-FLIP-FLOP UNDER HEAVY IONS

A. Single Event Upset detection in DFF

As reported in Table I, the DFFs can be classified in two categories: DFFs with 3 input signals and DFFs with five or higher input signals. These two categories will be referenced as classic and complex DFFs respectively.

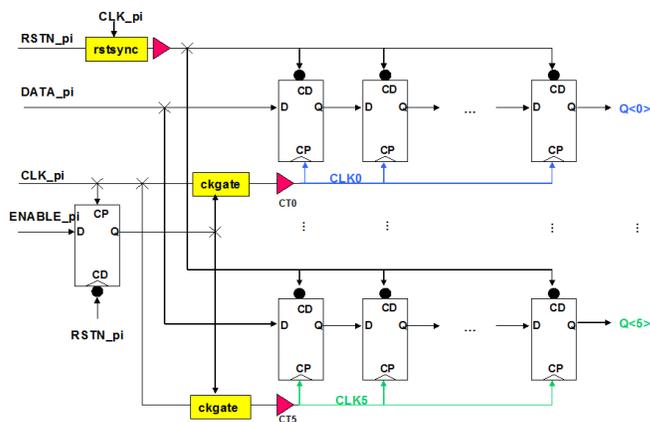


Fig. 3: Synoptic view of the 6 shift registers composed by 200 DFF cells designed by Sofradir for the two test vehicles

Fig. 2 (a) shows the nominal behavior of DFF5. The five input signals (SD , TE , TI , Clk , D) and the output signal, (Q), are presented. SD is the clear signal; TE is the selection signal of input data signals; D is the main input data signal; TI is the secondary input data signal; and Clk is the clock of the DFF; The DFF is synchronized on the rising edge of the clock signal. When TE is at low level, the DFF transfer the data of the D input to the Q output of the DFF; when TE is at high level, the DFF transfers the data of the secondary input signal, e.g. TI , on the output signal.

During the irradiation, a SEU has been considered when the output of the DFF chain changed from “1” to “0” or “0” to “1” depending on the stored logic state as illustrated in Fig. 2(b) by the white dashed circle.

B. Setup description SEU measurements

The devices under test (DUT) have been developed by Sofradir. The two test chips are designed with various DFF architecture chains as mentioned in [3]. Each of the DFF chain are composed of 200 DFF cells in order to maximize the SET capture during irradiation tests as depicted in Fig. 3. Each of the DFF chain shares the *Clock* (set at 20MHz), *Reset*, *Data*

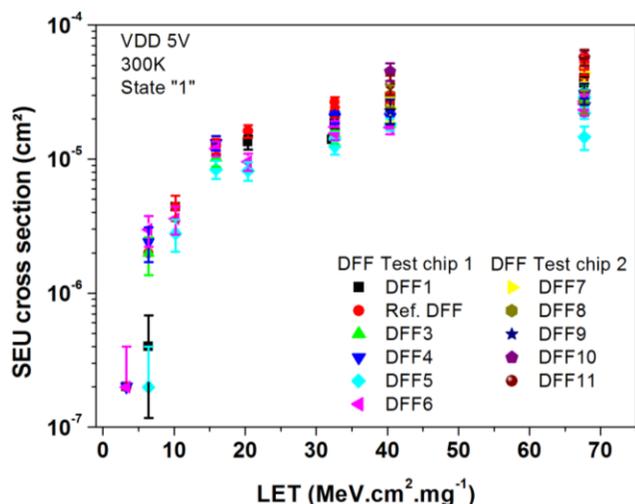


Fig. 4 SEU cross section of DFF with all architecture and design variations measured as a function of LET on the two test-chip at ambient temperature (300 K).

input and *Enable* signals. This minimizes the impact of the SEU over a unique and global clock tree.

The heavy ion tests were performed at the University Catholic of Louvain (UCL) for the two heavy ion cocktails. The CYCotron of Louvain la NEuve (CYCLONE) proposes different heavy ions species which are split in two "Ion cocktails", named $M/Q=5$ and $M/Q=3.3$. The heavy ion species have been presented in a previous work [3]. The chamber has the shape of a barrel stretched vertically; its internal dimensions are 71 cm in height, 54 cm in width and 76 cm in depth. One side flange is used to support the board frame (25×25 cm²) and user connectors. The chamber is equipped with a vacuum system. In the case of the campaign the DUT is in a cryostat connected to the vacuum chamber in order to allow for cooling the temperature of the chip during the irradiation test.

The temperature of the chip was monitored and regulated, by means of an instrument from CNES, to a range of temperatures from 77 K to 300 K [3]. The cooling system is based on a cryostat using liquid helium. The bias of the DFF chains was done in static and dynamic mode. In dynamic mode a fixed pattern was used (e.g. 01010101 ...). The frequency of the clock signal was 20MHz. In this work only the static mode is presented and discussed. The bias scaling dependence of the SEU sensitivity of the various DFF architectures will be discussed in the final section of the paper.

During each irradiation run, a delatcher system was used on the DUT's power in order to detect latchup occurrence. Two runs dedicated to latchup detection have been done. The runs were performed at room temperature (300 K) with a fluence of 1×10^7 cm⁻² at 67.7 MeV.cm².mg⁻¹. No single event latchup (SEL) was detected during the irradiation campaigns of the two test chips.

III. SINGLE EVENT UPSET IN DFFS UNDER HEAVY IONS

Fig. 4 shows the SEU cross section of DFFs with all architecture and design variations measured under heavy ions

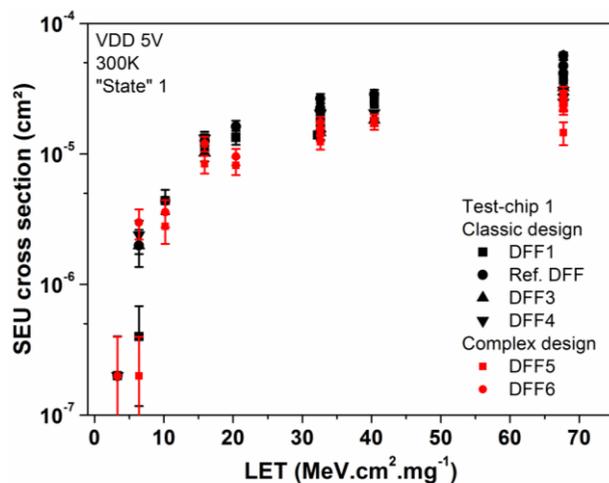


Fig. 5 SEU cross section of DFFs of test-chip 1 for simple (black symbols) and complex (red symbols) designs as a function of LET at room temperature (300 K)

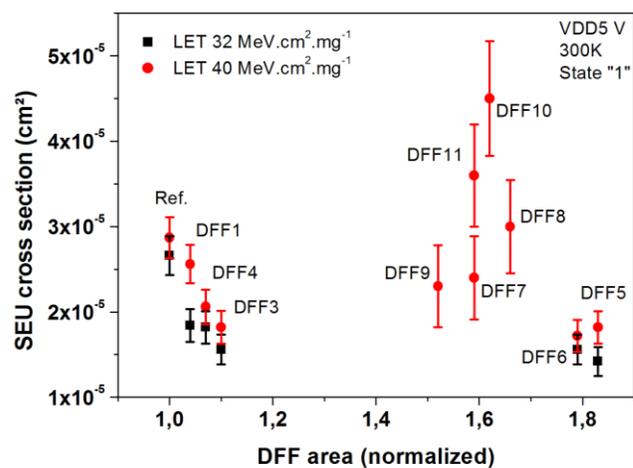


Fig. 6 SEU cross section of the eleven DFFs as a function of their area for two heavy ions with a LET of about 32 (black squares) and 40 (red dots) MeV.cm².mg⁻¹

at 300 K. The irradiation tests have been done across temperatures from 70 K up to at 300 K with a bias condition of 5V. Note that SEU data for test-chip 2 is only available for 40 and 67.7 MeV.cm².mg⁻¹. The wide variability of SEU cross section over 40 MeV.cm².mg⁻¹ is explained by the architecture and design variations of DFF. The impact of the architecture and design on the SEU sensitivity measured under heavy ions is investigated in the following section. A specificity of the design of the DFFs from test-chip 2 (DFF7 up to DFF11) is analyzed in the second part of the next sub-section.

A. Architecture and design dependence of the SEU sensitivity in D-Flip-Flops

Fig. 5 presents the SEU cross section measured on the four different designs of the two DFF categories: DFF1 (black squares), the reference DFF (black dots) as classic designs, DFF3 (black triangles) and DFF4 (black reversed triangles) as

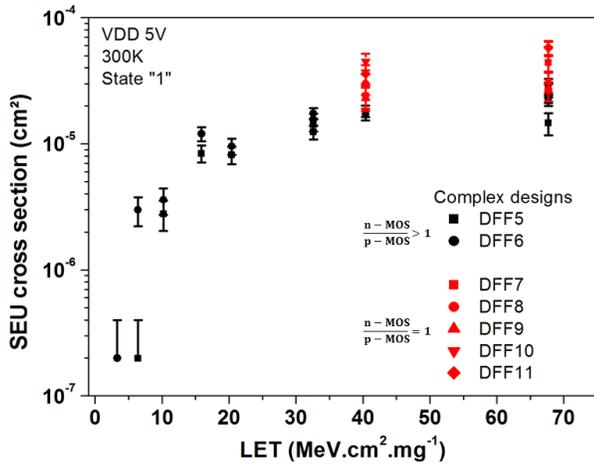


Fig. 7 SEU cross section of DFFs from test-chip2 as a function of the ratio between the number of n-MOS and p-MOS transistors.

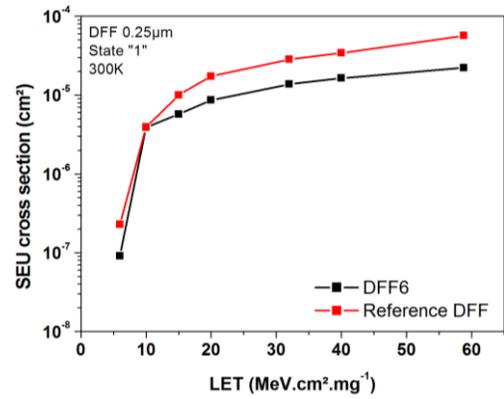
complex designs. The irradiation tests have been done at 300 K for a range of LETs from 3.3 MeV.cm².mg⁻¹ to 67.7 MeV.cm².mg⁻¹. The DFF stored the logic state "1" during the tests. Error bars represent the standard deviation. No real design dependence is observed of the SEU sensitivity for low LETs (under 20 MeV.cm².mg⁻¹). However, over 20 MeV.cm².mg⁻¹, test results suggest that DFFs with classic designs are more sensitive than the DFFs with complex designs of the test-chip1. This point can be moderated and completed by the analysis of the SEU sensitivity as a function of the DFF area.

Fig. 6 presents the SEU cross sections of eleven DFFs induced by heavy ions with a LET of about 32 and 40 MeV.cm².mg⁻¹. It appears that two SEU sensitivity trends can be identified. First, an increase in the DFF area induces a decrease in the SEU cross section, except for a group of five DFFs (DFF7 up to DFF11). This increase in cell area is partially due to wider transistors which induces a higher drive current. A higher drive current is known to improve the SEU robustness of CMOS gates [9]. This point should be confirmed in the next section by an analysis at circuit level.

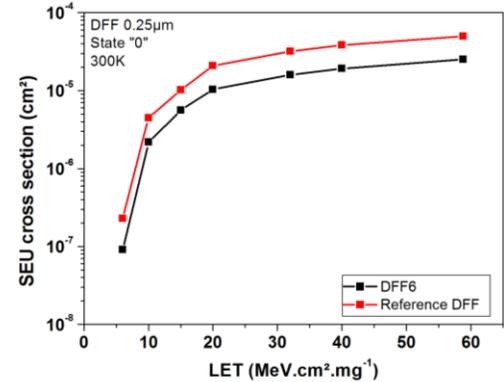
Second, the DFFs with areas between 1.5 and 1.7 use a different design rule. These designs are based on the same number of n-MOS and p-MOS transistors, as reported in Table I. This design specificity impacts the drive current of the floating nodes of the DFF. The floating nodes are known as potential critical areas for the occurrence of SEU in digital devices [3], [10], [11].

Fig. 7 presents the impact of the ratio between the number of n-MOS and p-MOS transistors on the SEU cross section of DFFs. The DFFs designed with a higher number of n-MOS transistors (black symbols) are less sensitive than the DFFs designed with the same number of n-MOS and p-MOS transistors (red symbols). This experimental data confirms the sensitivity trends observed in Fig. 6.

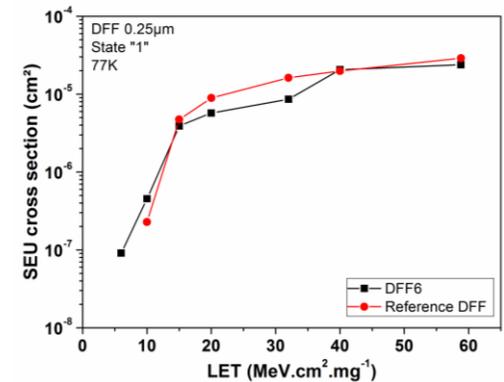
The analysis of the design effect on the SEU sensitivity will be completed at circuit level in the next section.



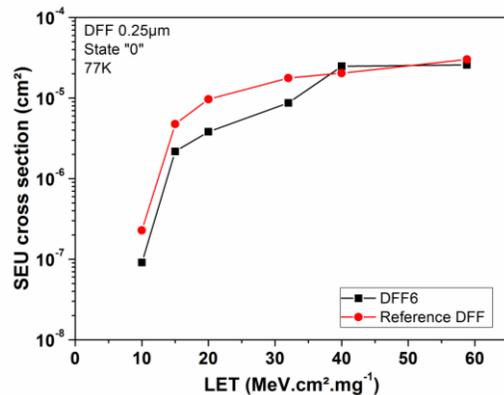
(a)



(b)



(c)



(d)

Fig. 8 Simulated SEU cross sections of DFFs for various complexities as a function of number of transistor n-MOS and p-MOS for various LET at 300 K and 70 K.

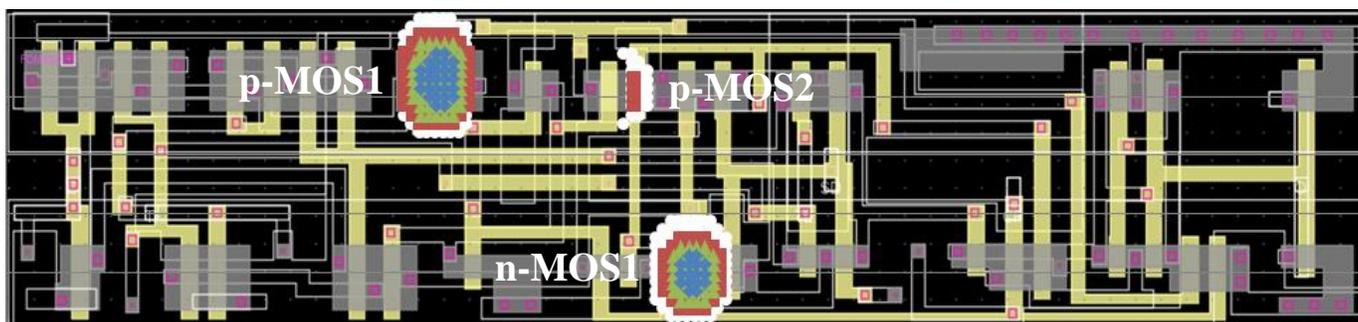


Fig. 9 SEU sensitivity mappings obtained by fault injection simulation representative of heavy ions with a LET of 10 (blue), 20 (green), 32 (red), 58.8 (white) $\text{MeV}\cdot\text{cm}^2\cdot\text{mg}^{-1}$ in the DFF6 (test-chip 1) at room temperature (300 K).

IV. FAILURE INVESTIGATION BY FAULT INJECTION SIMULATIONS

MUSCA SEP3 is a soft error prediction tool based on a Monte-Carlo approach, which performs a full flow of simulations from the interaction of the radiation particles with the device down to the occurrence of the soft error in the circuit (in this work DFF). The transport and collection mechanisms of generated charges in semiconductors (e.g. silicon) are simulated by 3-D analytical models. The complete description of the modeling and simulation flow is reported in previous works [10], [12], [13]. These fault injection simulations are based on physical simulations and electric simulations. A SET current database based on bias voltage, layout, and fabrication process was generated from the physical simulations. Next this SET currents database is used for fault injection simulations using a SPICE simulator with the aim to estimate the soft error response of the circuit. For this work, the n-MOS and p-MOS transistor models are provided by Sofradir.

The validation of the relevance of the SEU sensitivity modeling has been validated in previous work for the reference DFF and the DFF1 at room temperature (e.g. 300 K) and down to 70 K [3].

A. Effect of DFF design on SEU sensitivity trend

In order to confirm the global SEU sensitivity trend observed under heavy ion tests, SEU cross sections have been calculated at 300 K and 70 K.

Fig. 8 (a) presents the SEU cross sections calculated by the SEE prediction tool for two DFFs: the reference DFF (red dots) and DFF6 (black squares) under heavy ions. The SEU prediction tool emphasizes a higher SEU sensitivity for the classic design of the reference DFF than the complex DFF6, as observed with the experimental tests in Fig. 5. The same trend has been obtained for the DFF1 and DFF5. Fig. 8 (b) presents the same comparison of SEU cross section but with the logical state “0” stored in DFF6 and the reference DFF. The same comparison has been performed at 70 K as illustrated in Fig. 8(c) and Fig. 8(d) for the logical state “1” and “0” respectively. At 70 K, the effect of DFF design is very limited, especially at saturation of the cross section. It seems that

cryogenic temperatures limit the impact of the design on the SEU sensitivity of DFFs.

B. Failure analysis at layout level at nominal voltage

A failure analysis at layout level has been performed on the DFF6 with the aim to show the specificities of critical transistors which allow a stronger SEU robustness. Fig. 9 presents the SEU sensitivity mappings obtained by simulations representative of heavy ions with various LETs in DFF6 at room temperature. Each colored symbol indicates the SEU sensitivity of DFF6 if a heavy ion strikes the layout at the corresponding location. After the simulations by the SET fault injection, three sensitive transistors have been identified on the design of DFF6, as shown in Fig. 9. The three critical transistors (2 p-MOS and 1 n-MOS) are linked to floating nodes: as well for the Source and the Drain electrodes. Moreover, the criticality of these transistors is highlighted because one of them controls the propagation of the clock signal in the DFF circuitry.

A comparison between the design of the reference DFF and DFF6/DFF5 reveals a critical point: the critical transistor which controls the clock signal is designed with a drive current higher by a factor of 2 in comparison to the reference DFF. A higher drive current is known to improve the SEU robustness of a CMOS gate [9]. Then, this design specificity of the DFF6 which increases in the cell area explains the lower sensitivity of DFF6 in comparison to the reference DFF.

C. Temperature effects on SEU occurrence

Recent works reported the limited impact of the cryogenic temperatures on the SEU sensitivity in the reference design of DFF [3]. Fig. 10 presents the experimental measurements of SEU cross section of the DFF6 as a function of temperature for two values of LET. The results show a very limited impact of the SEU occurrence in the DFFs. The trend has been confirmed by simulation by the mean of MUSCA SEP3 tool coupled to SPECTRE simulations as shown in Fig. 11.

These results are consistent with experimental data presented in recent works regarding SET and Single Event Functional Interrupt (SEFI) [14] [15].

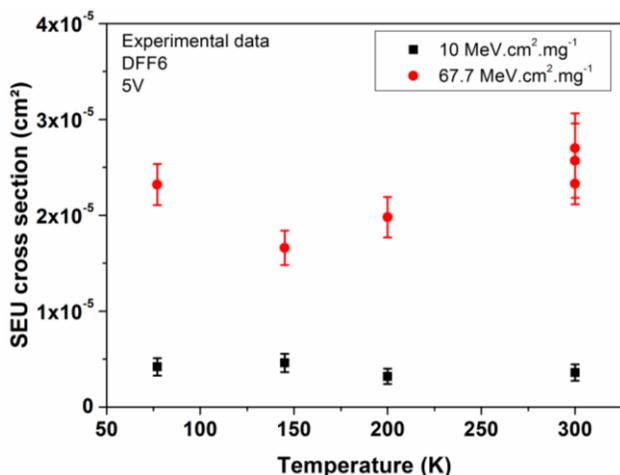


Fig. 10 Experimental measurements of the SEU cross section of DFF6 as a function of temperature for two LETs, $10 \text{ MeV.cm}^2.\text{mg}^{-1}$ (black squares) and $67.7 \text{ MeV.cm}^2.\text{mg}^{-1}$ (red dots)

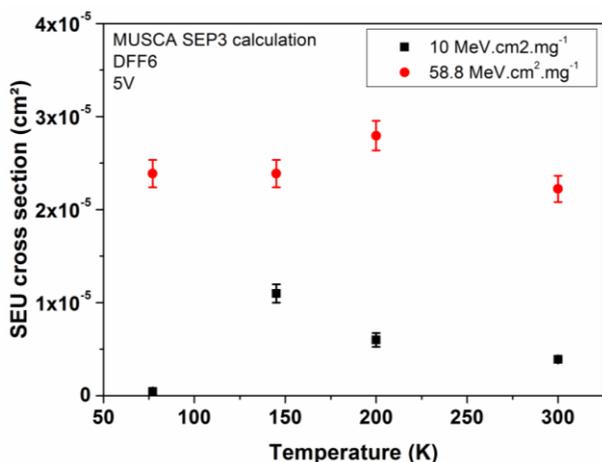


Fig. 11 Simulations of the SEU cross section of DFF6 as a function of temperature for two LETs, $10 \text{ MeV.cm}^2.\text{mg}^{-1}$ (black squares) and $67.7 \text{ MeV.cm}^2.\text{mg}^{-1}$ (red dots)

D. Prospective evaluation of the impact of the supply voltage reduction

It has been shown that a decrease in the supply voltage leads to an increase in the SEU sensitivity, independent of the technology's digital function [9] - [16]. For this technology, Sofradir has the opportunity to tweak the supply voltage of the D-Flip-Flop down to 3.3 V. However, it is interesting to note that the best trade-off performance has been obtained around 4.5 V. Fig. 12 presents the relative increase in SEU cross section depending on the core voltage SEU for a range of LET from $10 \text{ MeV.cm}^2.\text{mg}^{-1}$ up to $58.8 \text{ MeV.cm}^2.\text{mg}^{-1}$ for the DFF6 at state "1" at 300 K. An increase in the SEU cross section by a factor of two has been estimated for heavy ions with a LET range between 10 and $30 \text{ MeV.cm}^2.\text{mg}^{-1}$. On the other hand, the increase in the SEU cross section at saturation (over $50 \text{ MeV.cm}^2.\text{mg}^{-1}$) is very limited: lower than 6% even at 3.3 V. Finally, an important point is the limited increase (lower than 30%) in the SEU cross section for the optimal supply voltage (4.5 V).

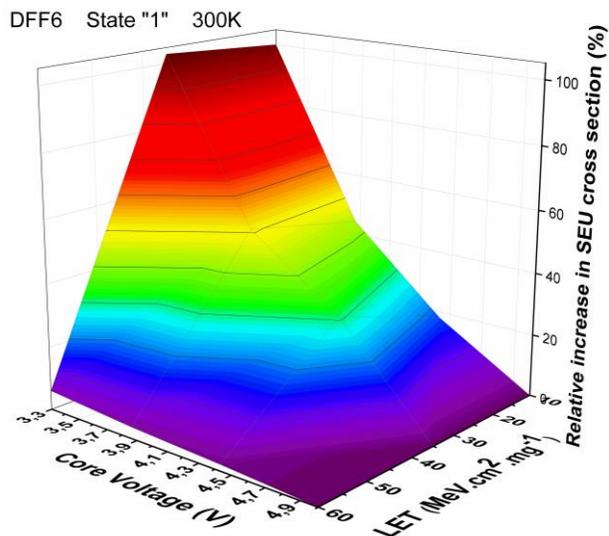


Fig. 12 Relative increase in SEU cross section depending on the core voltage SEU for a range of LET from $10 \text{ MeV.cm}^2.\text{mg}^{-1}$ up to $58.8 \text{ MeV.cm}^2.\text{mg}^{-1}$ for DFF6 at state "1" at 300 K

V. CONCLUSION

This work highlights the impact of design on the SEU sensitivity of D-Flip-Flips of a ROIC under heavy ions. New experimental data obtained at University of Louvain for several design and architectures are presented. The SEU sensitivity trends are discussed as a function of the DFF area, the design complexity and the number of n-MOS and p-MOS transistors. The analyses of the experimental measurements have been completed by a study at circuit level with the use of a fault injection tool. The simulations confirm the interest of wide transistor (2X drive current) which controls the clock signal. This wide transistor connected to the floating nodes of critical transistors improves the SEU robustness. This design specificity allows for increasing in the SEU robustness of the DFF. However, it appeared that cryogenic temperatures limit the impact of the design on the SEU sensitivity of DFFs. The results show a very limited impact of the temperature on the SEU occurrence, independent of the layout. The trend has been confirmed by simulation. These results are consistent with experimental data presented in recent works regarding SET and SEFI. These results allow for performing irradiation tests of CMOS IR detector (ROIC) at room temperature instead of cooling down the device during the SEE measurements.

Finally, a prospective evaluation of the effect of the supply voltage reduction has been done. It highlighted the relevant choice of Sofradir about the supply voltage used for their digital functions in the ROIC. In future works, the analyses of these six designs could be extended to the other DFF designs and architectures in order to generalize the highlighted mechanisms.

VI. ACKNOWLEDGMENT

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