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InAs/GaSb thin layers directly grown on nominal (001)-Si substrate by MOVPE for the fabrication of InAs FINFET

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Abstract:

We demonstrated the fabrication of a densely packed InAs fins network for nanoelectronic applications. High crystalline quality GaSb/InAs layers have been grown directly on 300 mm nominal (001)-Si substrate. The InAs was then processed by etching step using a lithographic mask based on block copolymer to obtain sub-20nm width fins. This block copolymer has been optimized to self-assemble into lamellar structure with a period of 30nm, standing perpendicular to the substrate thanks to a neutral layer. STEM-HAADF characterization displays vertical sidewalls InAs fins with a width as low as 15nm spaced by almost 10nm. Early electrical characterizations exhibit a current flow through the connected fins.

Keywords: A3 Organometallic vapor phase epitaxy, B2 Semiconducting III-V materials, B3 High electron mobility transistors, B3 Field effect transistors, A1 Etching

Introduction

The semiconductor industry has evolved to produce increasingly efficient transistors with the introduction of 3D architecture (FinFET) and continues to evolve with ongoing materials optimization. High mobility III-V semiconductors remain among the candidates to replace silicon as conduction channel and must be successfully integrated on nominal 300mm Silicon substrate to go further. This III-V growth on Si substrate remains very challenging due to the polarity change and lattice mismatch

between these two materials which are responsible of antiphase boundaries and dislocations formation. Usually a thick layer is used to packed these defects and get access to better quality top layers.

In this work we proposed the growth on GaSb/InAs layers directly on Silicon substrate for the fabrication of a multi-wires InAs FinFET. To achieve sub-20nm InAs fins an etching mask will be made from a block-copolymer (BCP) self-aligned layer.

Experimental set up

The III-V epitaxy has been carried out in a 300 mm Applied Materials MOCVD reactor using triethylantimony TESb and tertiarybutylarsine TBAs as group-V precursors and trimethylgallium TMGa and trimethylindium TMIn as group III-precursors. Ultra-pure hydrogen was used as carrier gas. The growth of GaSb layer was performed on (001)-Si substrate with an offcut angle of 0.11° along [110] direction. The substrates were first deoxidized in a SiconiTM preclean chamber under an NF₃/NH₃ remote plasma. Prior to the growth, the substrates were heated above 800 °C under H₂ atmosphere in the growth chamber to promote the silicon surface structuration and then exposed to TBAs precursors. We then pursued with the GaSb growth without introducing any transition between the GaSb growth and the InAs growth. After the GaSb growth, TESb and TMGa fluxes are turn off, the growth temperature is lower to 350°C and the pressure to 5 Torr. When InAs growth parameters are stabilized, the TMIn and TBAs precursors are introduced in the growth chamber.

Block copolymers etching mask conception goes through two steps: neutral layer made from PS-*r*-PMMA solution deposition and grafting onto the InAs followed by the block copolymer PS-*b*-PMMA deposition and self-assembly. The PS-*r*-PMMA solution was spin-coated on a 2 cm X 2 cm sample and then annealed at 200°C during 75sec. The non-grafted polymeric chains were removed by a PGMEA rinse afterward, then the PS-*b*-PMMA solution was spin-coated and annealed at 250°C during 5min for a total thickness of 40nm.

Etching step of the PMMA block was carried out on a 200mm inductive coupled plasma reactor. The fins patterning was performed using an Oxford Plasma Lab 100 ICP-RIE equipment with a heated chuck and backside He cooling.

Structural characterization was performed with a scanning electron microscopy (SEM) in cross-section view and top-view using a ZEISS ULTRA microscope. For lower resolution images, the structural properties were characterized with scanning transmission electron microscopy (STEM) using a field-emission-gun (FEG) electron source in cross-section and plan views. To perform this characterization, thin lamellas were prepared with a focused ion beam scanning electron microscope (Helios NanoLab 450S from FEI) combining focused ion and electron beams. High-angular annular dark field STEM (HAADF-STEM) images were realized using a probe-corrected FEI Titan (Ultimate) S/TEM operated

at 300 kV with a semi-convergence angle of the probe of 23.5 mrad (a probe size of ~ 0.7 Å) and a HAADF detector range of 60–366 mrad. High-angular annular dark field STEM (HAADF-STEM) image and EDX elemental maps of the Figure 1 were realized using a probe-corrected FEI Titan Themis S/TEM operated at 200 kV with a semi-convergence angle of the probe of 17.6 mrad (with a probe size of ~ 0.9 Å) and a HAADF detector range of 69–200 mrad.

Results and discussion

First of all, we grew a two-step thick GaSb layer to address the dislocations and antiphase boundaries (APBs) nucleation at the GaSb/(001)-Si interface. The GaSb growth is detailed elsewhere[1]. Dislocations formation are restrained by introducing a periodic Lomer array at the interface GaSb/Si with proper growth parameters, while APBs are managed by a two-way approach, with in the first place the control of the (001)-Si surface reconstruction in bi-atomic steps[2] and secondly, by introducing a surface pre-treatment before the GaSb growth. This pre-treatment consists of exposing the (001)-Si substrate surface to TBAs at low temperature. The temperature variation in a range of 100°C has no impact on the GaSb nucleation that follows in the process. An As-stabilized surface favors the growth of a low roughness and high crystalline quality GaSb layer whereas, TESb and TMGa do not. Similar results have been obtained in GaP growth on Si with an AsH₃ exposure[3]. AFM characterizations display a RMS roughness of 1.4 nm for a 200 nm thick GaSb layer with TBAs pre-exposure which increases up to 8 nm for other precursors pre-treatments. Further characterizations show that arsenic atoms spread into the GaSb nucleation layer to form a GaAs prenucleation 3D layer. HAADF-STEM images coupled with EDX (Figure 1) exhibit 5nm high and 15 nm wide GaAs islands. They arise at the GaSb/Si interface and can impact the subsequent 2D GaSb growth, as AlSb islands-forming nucleation layer for MBE growth of GaSb on Si substrate[4][5][6][7][8][9][10][11][12]. These islands may act in favor of the Lomer dislocations array formation which has been evidenced for GaSb/GaAs materials[13][14].

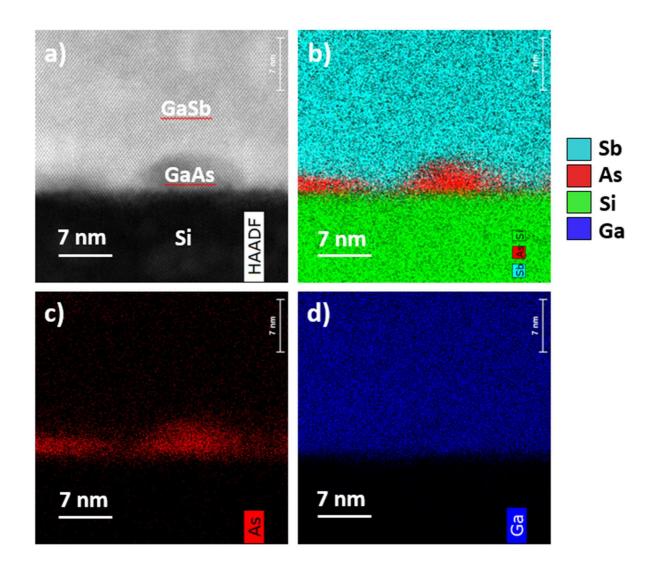


Figure 1: a) HAADF-STEM image of GaSb/Si interface and b,c,d) corresponding EDX elemental mapping images

On top of this GaSb/Si stack, a thin InAs layer has been grown in order to access the high electron mobility of InAs. The InAs epitaxy onto GaSb layer raised problems correlated with the nature of the interface InAs/GaSb. State of the art predicts the formation of an unintentionally GaAs-like or InSb-like interfacial layer[15][16] which can affect the electrical properties of the InAs layer. We experimentally faced the formation of an InSb-like interfacial layer between the InAs/GaSb layers which melts for InAs epitaxial temperature above 470°C. This melting is responsible for a high InAs layer roughness and imperfections at the interface GaSb/InAs (Figure 2). The formation of these defects gradually decreases while decreasing the temperature below the subthreshold of 500°C, which is very close to the InSb melting point and can therefore be linked to it.

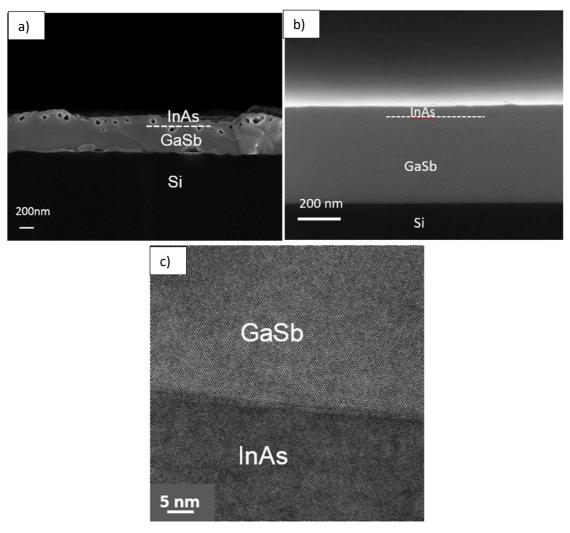


Figure 1: Cross-sectional views of InAs/GaSb interface for an InAs growth at a) high temperature (SEM image) and b,c) low temperature (SEM and TEM image)

TOF-SIMS characterizations (not shown) have been performed to identify the intermixing between these two layers after a low temperature InAs growth. The profile of the interface is asymmetric which can testify that interdiffusion occurs. However we cannot access the depth of the interdiffusion.

The transition from an island-forming InAs growth to a 2D InAs growth can be obtained by a low pressure and low temperature growth, which matches the growth parameters of an InAs layer directly on Si published by Alcotte et al[17]. In this set-up, a 50 nm thick InAs layer with a RMS roughness of 0.9 nm and sharp GaSb/InAs interface can be reached[18]. The presence of an InSb-like interfacial layer could not be confirmed by TEM image.

A lithography mask has been designed with lamellar block copolymer over the InAs layer in order to pattern InAs fins in a width range of 15 nm. To fulfill these dimensions specifications, we selected an experimental blend of PolyStyrene-*block*-Poly(methylmethacrylate) (Ps-*b*-PMMA) with a period of 30 nm. This blend allows for a better self-assembly kinetic and defectivity than the ones observed for a pure block copolymer within the same dimensions range[19]. The self-assembly period is defined by

the length of both PMMA domain and PS domain. These domains can stand parallel to the InAs surface depending on preferential interactions between either PS/InAs or PMMA/InAs, or perpendicular to the InAs surface in the case of a balanced ("neutral") interaction of both PS and PMMA blocks with the surface material. In the case of BCP used as a lithographic mask, a perpendicular phase is desired to etch a block selectively to the other one and then transfer line patterns into InAs. To access this orientation, the InAs interface must be neutralized by the deposition and grafting of a random layer PS-r-PMMA onto the substrate.

The PMMA blocks are then selectively etched relative to the PS blocks under an Ar/O₂ plasma. With a PS blocks etch rate of 3.5nm/sec, which is twice lower than PMMA blocks etch rate, the value of the resulting selectivity is 2.1. The Ar/O₂ plasma has the capability to open the neutral layer PS-*r*-PMMA, and thus fully reveals the InAs surface. Hereafter the PS blocks with a remaining height of 20 nm act as an etch mask for a BCl₃/SiCl₄/Ar 15/5/20 plasma that etches the InAs layer. This plasma, first studied on InGaAs[20], gives access to an InAs etching rate of 1.6nm/sec. InCl_x etching byproducts are not volatile at ambient temperature, thus high temperatures are used to promote their desorption. The obtained InAs fins have verticals sidewalls with low roughness, at their top the remaining PS thickness is about 15nm (Figure 3). Furthermore, PS blocks resistance to the rise in temperature beyond its glass transition temperature must be ensured by crosslinking under electron beam before the bake. Without this cross-linking step, PS domains melt and reflow, thus they no longer fulfill their role as an etching mask.

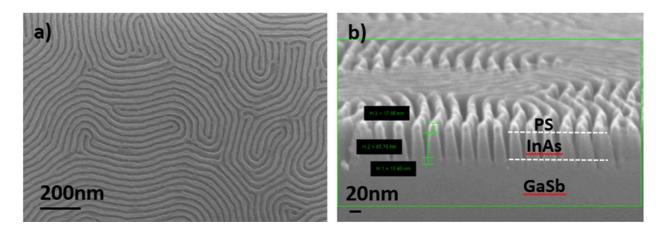


Figure 3: a) top-view and b) cross-section SEM images of lamellar PS-b-PMMA on top of InAs layer after InAs etch

STEM characterization (Figure 4) reveals some residual traces of PS on the sidewalls of InAs fins, which imply a PS pulverization during InAs etch and a further redeposition on the sidewalls. This PS redeposition appears white on the STEM image, and can appear light grey when InAs fins locally collapse. InAs fins are thereby well etched but locally touch along the 100nm thin lamella preparation. They can reach a width of 15 nm and a height of 20nm with a constant spacing of 10 nm. The

dimensions are well controlled and constant all over the lamella. Otherwise, fin sidewalls are almost vertical.

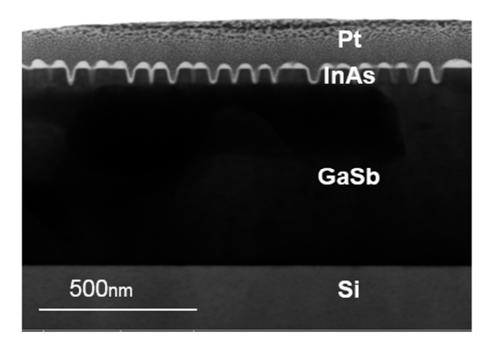


Figure 2: STEM image of InAs fins

To pursue with electrical characterization, 33 InAs fins have been connected by source and drain gold contacts. Uncertainties remain about the actual number and size of the fins because of the collapse of some fins. Electrical measurements show a drain current of $70\mu A$ for 100nm long InAs fins (Figure 5a) and $2\mu A$ for 200nm long InAs fins (Figure 5b). To date, the conduction in InAs fins is assumed and must be confirmed by other characterizations.

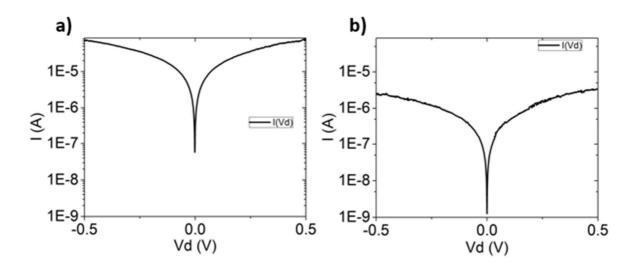


Figure 5: I(V) characterizations for 33 InAs fins connected a) 100nm long b) 200nm long

Conclusion

We demonstrated the high crystalline quality growth of GaSb/InAs layers directly on nominal (001)-Si substrate by MOCVD. GaAs islands have been evidenced by HAADF-STEM EDX characterizations at the GaSb/Si interface. They can act in favor of the Lomer dislocations array formation. The InAs growth on GaSb layer requires low growth temperature to avoid the melting point of InSb interfacial layer. The InAs layer was then etched using a block copolymer lithographic mask which allows to obtain 15 nm wide InAs fins. The InAs layer has thus been successfully processed to produce a densely packed InAs fins network for early electrical characterization. A current of 70 μ A flows through the 33 contacted 100 nm long InAs fins for a Vd= 0.5 V.

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