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Ultra-Low-Jitter Fully Tunable Baseband Pulse Generator for UWB Applications

Marco Garbati, *Student Member*, IEEE, Romain Siragusa, Christophe Halopé
and Etienne Perret, *Senior Member*, IEEE,

Abstract— This paper presents a fully tunable baseband ultra-wideband (UWB) pulse generator, realized with commercial off-the-shelf components (COTS). It is made of high speed logic gates and comparators, and it is compliant with current mode logic (CML) digital standard. The pulse emitted power and bandwidth are tunable with pulse-width and amplitude variation, which shows high flexibility. This advantage simplifies the design of the downstream shaping network, as so to be compliant with international regulations. A differential output with very low jitter, and high pulse repetition frequency (PRF) is demonstrated.

Index Terms— Jitter, radar, radar applications, ultra-wideband communication, ultra-wideband radar, impulse generator.

I. INTRODUCTION

ULTRA-wideband (UWB) technology is exploited in a variety of applications, from radar for tracking and localization, to short pulse communication [1]. An UWB radar transmits a train of UWB pulses in the direction of a target, and then measures the backscattered signals. These sources of information can be used to recover the target position and shape. For short pulse communication applications, time or frequency-division multiplexing algorithms are used. Both are real-time implementation [1], and usually adopt diode based receivers, such as a frequency converter, to get the data in baseband. In this type of systems, because of the receiver characteristics, a high reproducibility of the transmitting UWB pulse is not required. Therefore, a time-gated oscillator is generally employed as UWB pulse generator [1].

In [2] a pulse generator based on voltage controlled oscillator (VCO) with tunable central frequency is proposed. Besides pulse position modulation (PPM), it is possible to use pulse amplitude modulation (PAM) where the pulse generator output amplitude is attenuated depending on the transmitting binary code [3].

In order to decrease fabrication costs, most UWB radars are based on equivalent-time algorithms, which can still achieve time resolution in the order of picoseconds [4]. With equivalent time approach, the reproducibility of the UWB

transmitting pulse is a key parameter, and therefore the pulse generator cannot be a simple time-gated oscillator. In an equivalent time system, different pulses are transmitted for each acquisition process, in order to reconstruct the target signature. It assumes besides the stationarity of the target in relation with the radar acquisition time, also the reproducibility of the transmitting signal. At this scope, a baseband UWB pulse generator, hereafter B-UWB-PG, is most employed with equivalent time systems. It is able of generating a Gaussian pulse that may be derived in time domain of different orders, with a dedicated downstream circuit. A trigger input allows for its generation. The derivative circuit can be formed of only the antenna thanks to its time derivative property [5].

According to the application, B-UWB-PGs differ in characteristics [6]. Most are designed with step recovery diode (SRD) and bipolar transistors driven in avalanche mode to generate Gaussian baseband pulse [7]. Due to the voltage and frequency output characteristics, SRD solution is the most widespread in a variety of applications, from UWB communications to system characterization [8-9]. The pulse is sub-nanosecond with high slew rate, i.e. low pulse rise and fall time. The B-UWB-PG is composed of two different circuits in series: a driver and a pulser [10-11]. The driver is able to generate a pulse waveform with duration of several nanoseconds. The pulser exploits the junction impedance transition of the diode to generate the UWB pulse. This solution can provide a pulse repetition frequency (PRF) in the order of few MHz. The bipolar transistor driven in avalanche mode solution [12] provides a high voltage output pulse at the expense of a limited PRF, and it requires the use of a high voltage supply (around 200 V). It is ideal for long distance radar utilizations.

Different diode and transistor families may be used within the same pulse generator to customize some pulse characteristics. For instance, in [13] a SRD and a PIN diode are combined in the same circuit to generate a UWB pulse, which is either Gaussian or Monocycle.

In [14], the reproducibility of a step recovery diode (SRD) based pulse generator output is studied through its jitter modeling. It shows how defects in the pulse reproducibility negatively affect more equivalent time sampler systems rather than real time. The jitter of the complete device (which represents the statistical variation of its propagation delay) depends most on the shot-noise of the diode. The statistical jitter standard deviation can be in the order of tens of

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picoseconds.

Emerging technologies, such as chipless UWB radio frequency identification (RFID), are suitable for equivalent-time receivers thanks to their stationary nature. The pulse generator is expected to have low jitter, and also low cost [15-16]. It ensures an affordable and reliable reader.

It is also possible to design a B-UWB-PG with logic gates where wideband glitches are created. Almost all of them are integrated solutions [17-18], based on sharpened trigger input signals, with limited flexibility in terms of pulse-width, amplitude, and with single ended output. Recently notable integrated configurations have been proposed to add a certain amount of flexibility in these solutions. In [19], a CMOS pulse generator with flexibility in terms of amplitude is proposed. To modulate the pulse amplitude, the pulse generator exploits the variation of the duty cycle of the input signal that defines the bit pattern. In [20], an all-digital pulse generator that supports a DB-BPSK modulation is presented. It allows for pulse position modulation, and output channel selection in between the range of 3.4-4.8 GHz, with three channels of 500 MHz. It is a digital implementation and needs external shaping pulse filter, and pulse generator at the input. In [21], a configurable pulse generator in terms of pulse width and position is presented. In [22], a pulse width tunable triangular UWB PG is proposed. A new technology based on Libove gate architecture is proposed in [23]. It ensures high repeatable synthesis which is needed in equivalent time applications such as chipless RFID. It also allows for high PRF, in the order of GHz, and a pulse width as low as 20 ps when integrated in GaAs technology.

In [24] a UWB pulse generator using commercial off-the-shelf components (COTS) components is proposed. Its architecture is based on an inverter and an *OR* gate, its maximum PRF is of about 100 MHz, the pulse-width is fixed to 500 ps, and it does not have any flexibility in terms of pulse-width and output amplitude. Thereby, the design of the pulse shaping network, to be compliant with international regulations, can be cumbersome. The regulations limit the UWB power emitted according to Federal Communications Commission (FCC) and European Telecommunications Standards Institute (ETSI) [25-26]. Finally, because of its high pulse-width, the signal energy at higher frequency can be too low for applications such as Chipless RFID. In [27], a pulse generator realized with COTS components is also proposed. It has three comparators and an any logic gate. The output is a Gaussian pulse with fixed pulse width of 820 ps, a -10 dB bandwidth of 2.8 GHz, a PRF of 20 MHz, and an amplitude over 50 Ω of less than 0.2 V.

This work proposes a B-UWB-PG, realized with high frequency discrete logic. Indeed nowadays, commercial discrete digital devices, with clock frequencies over 10 GHz, are available for applications such as RF test-equipment, and serial data transmission. The proposed solution does not require any input trigger with a sharp rising edge. This feature is a relevant advantage in practical applications because the pulse generator can be integrated with low-speed transistor-transistor logic (TTL) and complementary metal-oxide

semiconductor (CMOS) technologies based system [28]. The B-UWB-PG also presents a tunable pulse-width and amplitude feature. This flexibility can be exploited for modulation purposes, and also for reducing the complexity of the downstream circuit design. The circuit was intentionally designed with COTS components to be easily reproduced and customized around diverse projects requirement. In fact an ASIC design is generally expensive and time consuming.

The paper is structured as follows. Section II describes the pulse generator architecture. Section III introduces the simulation model and results. In IV measurement are proposed. In Section V the B-UWB-PG outputs are manipulated with further stages to presents potentially regulation compliant configurations. Finally some conclusions are drawn.

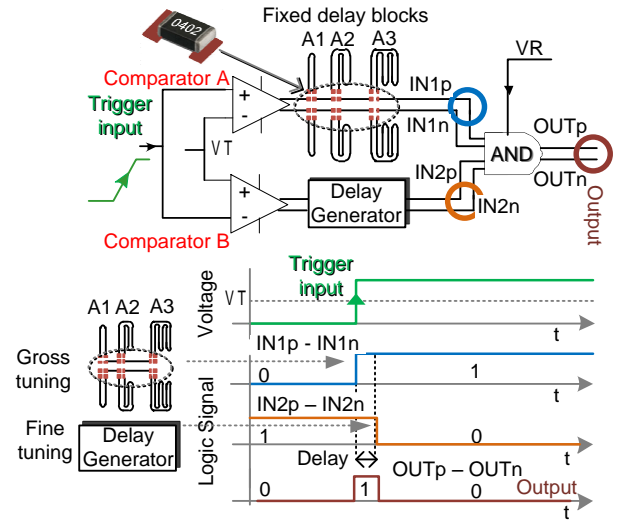


Fig. 1. B-UWB-PG principle schematic. After a trigger event (rising edge), the comparator A switches from 0 to 1, the comparator B from 1 to 0. With the delay generator, the AND gate presents two inputs with the same logical value 1 for a short period of time. It creates a glitch, i.e. a baseband UWB pulse. The amplitude of the pulse is varied with the dedicated pin VR.

II. PULSE GENERATOR ARCHITECTURE

The schematic of the proposed device is shown in Fig. 1. It is mainly composed of two high performance comparators, A and B, a variable delay generator, and an AND gate. According to current-mode logic (CML) standard, the connections between these devices are balanced. The connection between the comparator A and the IN1 input of the AND gate has a tunable length by soldering 0402 0 Ω surface-mount resistors. It is possible to add three different additional transmission lengths, called A1-A2-A3, where $A2 = 2A1$, and $A3 = 2A2$ with A1 equal to 16 mm. The positive input of A and the negative input of B are connected to the trigger input. The other two inputs of the comparators are connected to the positive threshold voltage VT (see Fig. 1).

When the trigger input crosses the threshold, the two comparators switch at the same time, but in opposite digital directions. While the trigger input is at 0, i.e. lower than the threshold, the output of A is 0 and of B is 1. Therefore, the output of the AND gate is 0. When the trigger crosses VT

during its rising edge, the output of A will go to 1 and that of B to 0. However, the inputs of the AND gate do not switch simultaneously. The time employed to the signals to go from the output pins of the corresponding comparator to the input pins of the AND gate is variable. It depends on the fixed delay blocks length A1-A2-A3 for IN1, if employed, and on the delay generator for IN2. Modifying these parameters allow the two inputs of the AND gate to have the same logical value 1 for a tunable and short period of time. It produces a glitch at the gate output, which is the generated pulse.

The AND gate presents a pin called VR that is able to modulate continuously output amplitude. Its absolute variation was experimentally found between 0.6 V to a minimum of 0.03 V for VR = 0.4 V and -1.2 V respectively. The evaluation board of the pulse generator proposed is shown in Fig. 2. Its size is 8.5 cm × 7 cm and it was manufactured on a low-cost FR4 substrate.

The selected comparator was from the Analog Devices HMC675LP3E. It can deliver an output signal with rise and fall times of 27 ps and 18 ps respectively. It has a deterministic jitter of 2 ps, a random jitter of only 0.2 ps, and a balanced output compatible with the CML digital standard. The delay generator was from the Analog Devices HMC856LC5 with a rise and fall time of 20 ps and 18 ps, respectively, it is compatible with the CML standard and has a balanced input and output. Its propagation delay is of 255 ps with an additional digitally controlled delay ranging from 0 to 93 ps, with 3 ps of resolution. The AND gate was from the Analog Devices HMC722LCRC, its output rise and fall time is of 19 ps and 18 ps, it has a deterministic jitter of 2 ps and a random jitter of 0.2 ps. All the components were selected for their performances in terms of jitter and output rise and fall time (high slew-rate).

The balanced interconnections on the PCB were realized with differential parallel grounded coplanar waveguide (CPW) transmission lines. The glitch signal, i.e. the output of the B-UWB-PG, is required to have a rise and fall time, and a pulse-width of tens of picoseconds in order to have large -10dB bandwidth on UWB (3.1–10.6 GHz). This is ensured by the sharp response of all the main components employed, and the tunability of the output pulse-width. The two comparators have a cost of about 35€ each, the delay generator of about 184€ and the AND of about 127€ (Digikey).

From the chronogram of Fig. 1, the rising edge of the generated pulse is settled by the length of the blocks A1-A2-A3, while the falling edge by the delay of the delay generator. Longer length of the blocks A1-A2-A3 corresponds to a lower pulse width (the pulse rising edge is delayed). For higher delay of the delay generator chip a higher pulse width (the pulse falling edge is delayed) is obtained. The pulse width therefore may be settled with a gross and a fine tuning. The gross tuning is settled by the blocks A1-A2-A3, where the smaller length is 16 mm, which corresponds to a transmission delay of about 100 ps on FR4. The fine tuning is represented by the delay generator chip with a minimum delay of 3 ps.

Playing with the blocks A1-A2-A3 for the connection between comparator A and AND gate, and the delay

generator, it is possible to obtain a pulse with a full width at half maximum (FWHM) (pulse-width) ranging from 60 ps to 325 ps with a resolution as low as 3 ps. The delay added with the blocks A1-A2-A3 is of about 100 ps, 200 ps and 400 ps. The small pulse width of 60 ps was obtained using the block A2 and setting the delay generator internal delay at 30 ps. The larger pulse width of 325 ns was obtained without using any of the delay blocks A1-A2-A3, and by setting the delay generator internal delay at the maximum (93 ps). The PRF is limited only from the pulse-width and the input bandwidth of the comparator. The input bandwidth is of 10 GHz while the maximum pulse-width is of 325 ps. In case the input trigger has a duty-cycle of 50 % the PRF is approximately,

$$PRF = \min(10 \text{ GHz}, \frac{1}{2PW}) \quad (1)$$

where PW is the pulse-width. For PW = 325 ps the PRF is of 1.53 GHz, and for 60 ps it is of 8.3 GHz. It is also possible increase these figures having a trigger signal with higher duty-cycle.

The B-UWB-PG is composed of high performance components, which required different and precise alimentation values. The AND gate and the delay generator are supplied with a voltage of -3.3 V, while the comparators required -3 V and 3.3 V. The B-UWB-IG power consumption is of 1,040 mW, which is compatible with UWB 3.0 using two units for alimentation purpose. Most of the energy is absorbed into the delay generator (610 mW).

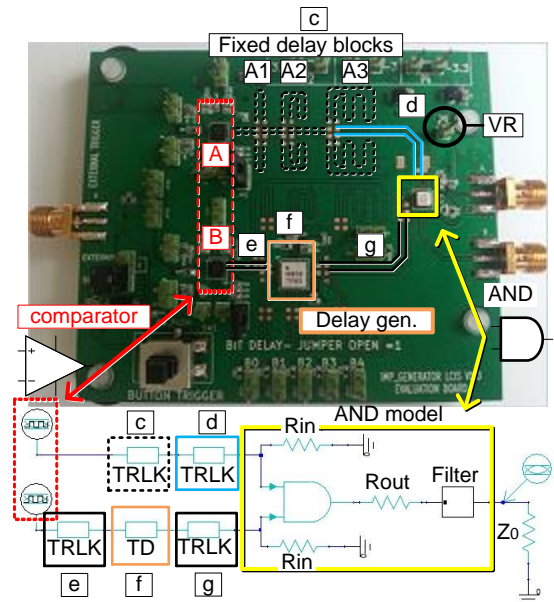


Fig. 2. B-UWB-PG evaluation board. This 4-layer FR4 PCB presents three different external alimentation points, 3 V, -3 V and -3.3 V. Through a jumper, the trigger could be external or entrusted on a push button. The delay of the delay generator is imposed by five jumpers. The output is balance and once DC coupled, it is capable to generate two differential output pulses. The pin called VR is used to modulate the output amplitude.

III. SIMULATION MODEL

A. Block Description

The simulation model of the pulse generator prototype was

realized using Ansys Electromagnetic suite 17.0, and is shown in Fig. 2. The output of the two high performance comparators was emulated using two eye sources capable of generating two trains of pulse, with rise and fall time equal to the comparator specification. A source of jitter with Gaussian probability density function (PDF) has also been added. The chosen standard deviation was of 2 ps, it is higher than the value reported in the data sheet of the comparators. Albeit, this choice can be justified thinking of real applications, where many factors such as environmental conditions, impedance mismatching and crosstalk could increase the effective device random and deterministic jitter [29].

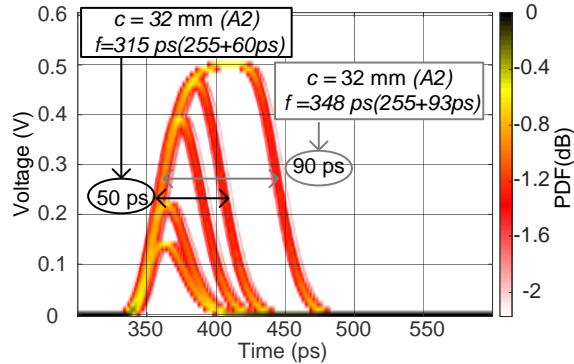


Fig. 3. Eye diagram of the simulation model in Fig. 2 tuning the variable which models the delay generator. It was realized over 300 of pulse realizations with Matlab, where the jitter of the AND gate output was added from the Ansys transient simulation results. The variable c was fixed at 32 mm (A2) and the variable f was sweeping between 279 ps (255 ps + 24 ps), 285 ps (255 ps + 30 ps), 300 ps (255 ps + 45 ps), 315 ps (255 ps + 60 ps), and 348 ps (255 ps + 93 ps).

The transmission lines between the comparators output and the AND inputs were modeled with TRLK blocks, where all the fundamental parameters are supposed not dispersive. A TRLK is a non-dispersive transmission line where parameters such as the length or even the characteristic impedance can be settled by the user. A variable called c takes into consideration the total length of blocks A1-A2-A3. The TRLK of 53.04 mm called d takes into account the length of the line that connects the comparator A and the corresponding AND gate input, after the blocks A1-A2-A3. The connection between the output of B and the input of the delay generator is represented with the TRLK block e , with a length of 12.23 mm. The block g of 35.5 mm is for the output of delay generator and the other input of AND gate. Another variable f counts for the delay generator propagation and tunable delay, and is implemented using a TD block, which is a non-dispersive transmission line defined through its impedance characteristics and its time delay.

The AND gate was modeled using an ideal threshold model written in Verilog-AMS, with 50Ω resistors for input and output impedances. Finally a 5th order Gaussian low pass filter with bandwidth of 10.84 GHz was added. This figure was obtained exploiting the well-known relationship between filter output rise time at ideal step input (0 ps rise time), and filter bandwidth [30]. The output rise time was the one of the AND gate data sheet multiplied for a factor of 1.6 to be converted from 20-80 % to 10-90 %. In Fig. 2 Z_0 represents an ideal

50Ω load. The AND gate output jitter was added in post processing using Matlab, with a Gaussian PDF with 2 ps standard deviation from the Ansys transient simulation result. For simplicity all the connections between the different components were single instead of balanced.

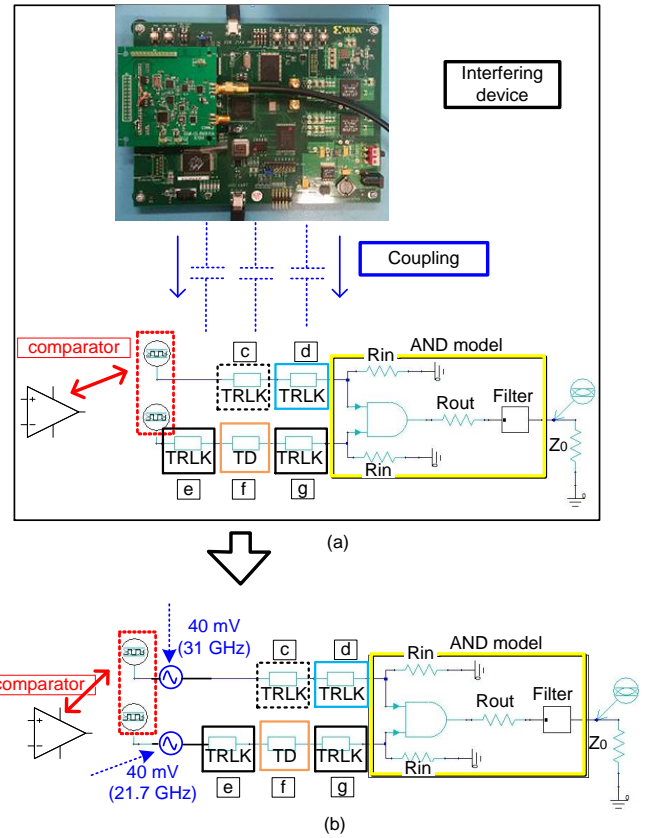


Fig. 4. Crosstalk Analysis. (a) Illustration of the crosstalk between the B-UWB-PG and an external device due to the presence of the transmission lines. Model used for simulating the crosstalk effects at different comparator rise and fall time. Two sinusoidal generators were inserted at the output of the eye sources (comparators) to emulate the induced tension on the B-UWB-PG transmission lines from crosstalk.

The eye diagram of the simulation model output tuning the variable f , which model the delay generator, is shown in Fig. 3. The colorbar represents the vertical histogram results of the eye diagram, in logarithmic scale. It was realized over 300 of pulse repetitions.

The variable c was fixed at 32 mm (A2) while the variable representing the delay generator (f) was sweeping between: 279 ps (255 ps + 24 ps), 285 ps (255 ps + 30 ps), 300 ps (255 ps + 45 ps), 315 ps (255 ps + 60 ps), and 348 ps (255 ps + 93 ps). The smaller pulse-width of Fig. 3 (about 30 ps) corresponds to the minimum delay imposed of 279 ps and the bigger of about 90 ps for the maximum delay of 348 ps.

In the simulation model the effect of the output amplitude variation, using the pin VR (see Fig. Fig. 1), was implemented. It only modifies linearly the output amplitude without affecting the system performance. From Fig. 3 for the signals with a pulse-width lower than 50 ps, the pulse amplitude also decreases. Thus, if the B-UWB-PG is used with a PAM scheme, the information coded on the output pulse amplitude is lower for smaller pulse-width.

B. Crosstalk Analysis

The use of high performance comparators in terms of low rise and fall time is indispensable in practical applications. This is because the digital logic devices employed do not have hysteresis capability. Therefore, their input-output characteristics are a static non-linear function, where the dynamic variations are only due to parasitic effects. One assumption is that AND gate input signals with small slew-rate (higher rise and fall time) will contribute to a small B-UWB-PG rejection against crosstalk effects produced by external devices. Indeed, the proposed B-UWB-PG is composed of two high performant comparators and the following study consists in showing the interest of using such a component.

A crosstalk phenomenon has been modeled in simulation with the circuit shown in Fig. 4. The B-UWB-PG was simulated with a fixed configuration, corresponding to a pulse-width of approximately 90 ps. Two sinusoidal generators were added at the output of the two eye sources to emulate the crosstalk effects. These signals have amplitude of 40 mV, and a frequency of 31 GHz for the upper generator and of 21.7 GHz for the other (see Fig. 4). To show the effect of the comparator output slew rate variation on the output AND gate signal due to crosstalk noise rejection, the simulation was carried out acting on the eye sources rise and fall time which are used to emulate the two comparators. First corresponding with the characteristics of the two actual comparators employed given in the datasheet, a rise and fall time of 27 and 18 ps respectively have been considered. Then these two values have been set up to 1ns, which can correspond to a rise and fall time of TTL and CMOS devices. In Fig. 5, the B-UWB-PG output eye diagram for the two cases is shown. The effect of crosstalk on pulse distortion is evident for the case of higher rise and fall time (1 ns). For lower frequency value, and amplitude of the two sinusoidal generators in Fig. 4, no significant distortion has been observed from simulation results. Thus, the use of fast comparators (low rise and fall time) increases the B-UWB-PG crosstalk rejection effect.

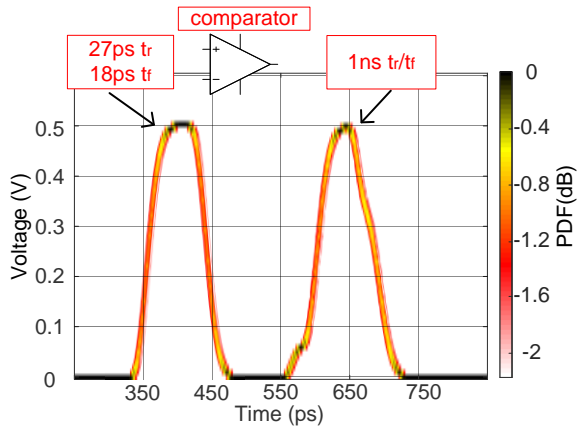


Fig. 5. Eye diagram of the simulation model in Fig. 4 (b). The two sinusoidal sources emulate crosstalk effects due to external devices. The simulation was performed for different comparator rise and fall time.

IV. MEASUREMENT RESULT

A. B-UWB-PG Output Characterization

As the B-UWB-PG presents a balanced output, two pulses with inverted polarity can be generated. According to the CML digital standard, the DC component of the two output pins is not equal. It is of 0 V for the negative single output and of -0.4 V for the positive output, when no pulse is created. However, it is possible to AC couple the outputs to force the DC component to 0 V.

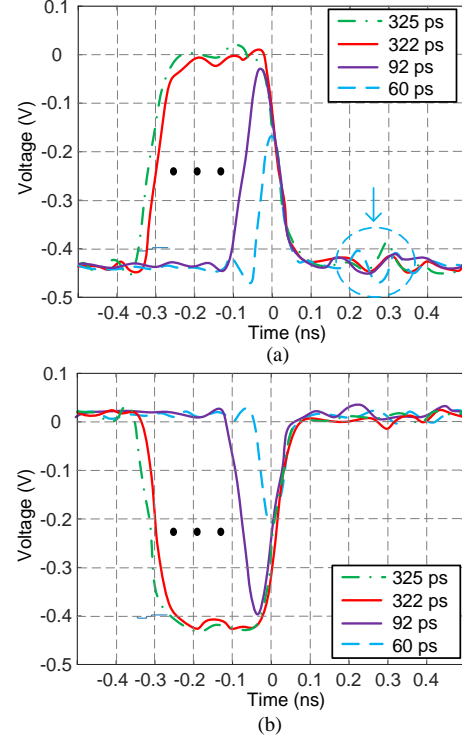


Fig. 6. Single output of the B-UWB-PG evaluation board measured for different delay generator configuration, and transmission line length (A1-A2-A3) with VR equal to 0 V. In (a) and (b) the measured of the positive and negative balanced output of the AND gate respectively, both referred to ground.

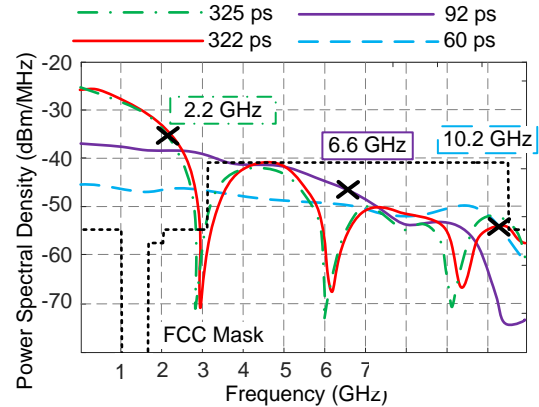


Fig. 7. Calculated PSD over MHz of the signals plotted in Fig. 6 (a) with a PRF of 50 MHz. The FCC mask for indoor application is also shown.

The measurement of the positive (a) and the negative (b) output voltages of the pulse generator, with different FWHM and with VR at 0 V, are shown in Fig. 6. Differently from

simulation results of Fig. 3, the variation of pulse amplitude with pulse-width is starting from a higher FWHM of around 90 ps, while it was of 50 ps from simulation. To explain this dissimilarity between simulation and realization, different simulations have been performed. Finally, in the B-UWB-PG model of Fig. 2, the bandwidth of the Gaussian filter at the output of the AND gate was reduced from 10.84 GHz to 7 GHz. A better similarity between simulation and measurement results has been obtained. This filtering effect is due to the impedance mismatching, at higher frequency, between the AND gate output pin and the B-UWB-PG PCB. Thus, the performance of the B-UWB-PG may be increased reducing this mismatching with an enhanced PCB layout.

The calculated power spectral density (PSD) over MHz of the positive output voltage (Fig. 6 (a)) is shown in Fig. Fig. 7 for a PRF of 50 MHz. Its absolute values can be increased of a maximum of 2.5 dB varying VR from 0 to the maximum value of 0.4 V. As expected, the maximum response is at 0 Hz, independently from the pulse-width [31]. The -10 dB bandwidth for the 60 ps is of about 10 GHz. To modulate the position of peaks and the valleys along with the frequency range, it is essential to derivate in time the response of the pulse generator. At 50 MHz of PRF corresponds a period of 20 ns which is compatible with short range communications and identification applications such as chipless RFID tag applications [16].

From Fig. 6 the shape of the pulses can be approximated with a rectangular function for bigger FWHM, while Gaussian for smaller FWHM. The module of the spectrum of a rectangle of width ΔT and amplitude A is,

$$|G(f)| = |A\Delta T \text{sinc}\pi(f\Delta T)|, \quad (2)$$

and its -10dB bandwidth is approximately,

$$f_{-10dB} = \frac{0.73}{\Delta T} \quad (3)$$

From Fig. Fig. 6 (a) the higher FWHM pulse of 325 ps, according to (2), should present a -10 dB bandwidth of 2.25 GHz. As plotted in Fig. 7, from measurement a smaller bandwidth of 2.2 GHz is obtained. The error respect to 2.25 GHz is of only 2.2 %, which validate the rectangular pulse assumption. As mentioned, the narrower pulse shapes can be approximated by Gaussian pulses with the following expression,

$$V(t) = \frac{A}{\sqrt{2\pi\sigma^2}} e^{(-\frac{t^2}{2\sigma^2})}, \quad (4)$$

where A is the maximum of the pulse, and σ is the shape factor (standard deviation). For simplicity we suppose the curve centered in 0 s. The module of its spectrum is,

$$|G(f)| = \left| A e^{(-\frac{(2\pi f\sigma)^2}{2})} \right|, \quad (5)$$

and its -10dB bandwidth is,

$$f_{-10dB} = \frac{\sqrt{2.303}}{2\pi\sigma}. \quad (6)$$

For Gaussian pulse the relationship between FWHM and shape factor is,

$$FWHM = 2\sqrt{2\ln 2}\sigma \approx 2.3548\sigma. \quad (7)$$

therefore combining (6) and (8) we obtain,

$$f_{-10dB} = \frac{0.5687}{FWHM}. \quad (8)$$

From Fig. 6 (a) the minimum FWHM is of about 60 ps, using (6) the -10 dB bandwidth is of about 9.48 GHz. Meanwhile, from measurement, a value of 10.2 GHz is obtained (the error is of only 5.5% respect to 9.48 GHz). It can be demonstrated that this error is due to the ringing effect underlined in Fig. 6 (a). For the FWHM pulse of 92 ps, from (6) the -10 dB bandwidth is of 6.18 GHz, it is of 6 GHz from measurement results (Fig. 7). The error is negligible and it is due to the almost absence of ringing for that case [32].

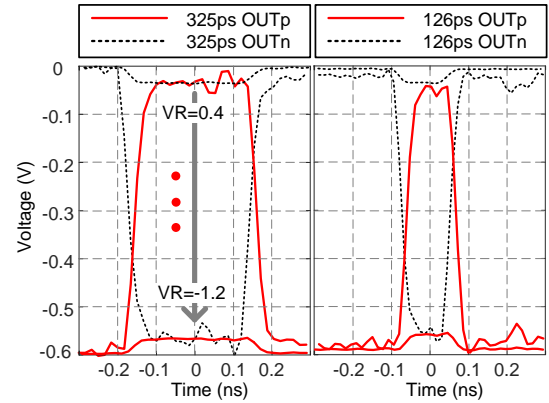


Fig. 8. measurement results for the negative (black dashed curves) and positive (red curves) outputs of the proposed B-UWB-PG, for two FWHM configurations, respectively 235 ps and 126 ps varying linearly the tension applied to the pin VR from 0.4 V and -1.2 V.

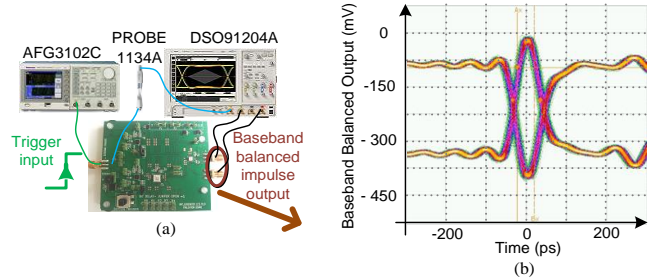


Fig. 9. Random period jitter measurement with eye diagram using the 12 GHz Agilent DSO91204A, and the 7 GHz Agilent 1134A probe as trigger reference for the oscilloscope.

To show the effect of the pin VR (amplitude modulation), the B-UWB-PG output for two configuration of FWHM was measured varying the tension applied to VR. The FWHM were settled to 235 ps and 126 ps respectively, and the VR voltage was varied linearly from 0.4 V to -1.2 V. The measurement results are shown in Fig. 8. Black dashed line is the B-UWB-PG negative output pulse, and the red line is the output positive pulse. Fig. 8 shows a dynamic variation for each B-UWB-PG output port from 0.6 V to 0.03 V, these results can also be exploited for on-off keying (OOK) modulation without playing with the triggering signal. With

the FWHM variation capability, a pulse-width modulation (PWM) could also be implemented to increment the information carried on by each pulse.

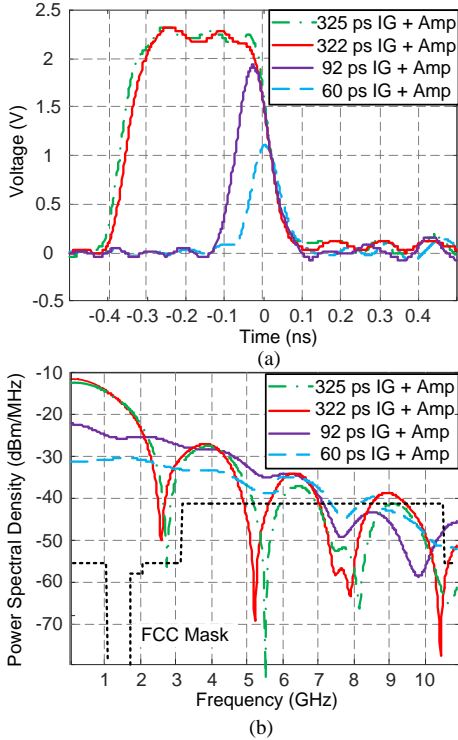


Fig. 11. Measurement results of the B-UWB-IG with the gain block amplifier (see Fig. 10) expressed in time (measured) (a) and in frequency ((calculated) (b) with a PRF of 50 MHz.

B. B-UWB-PG Jitter Characterization

The jitter of the pulse generator was measured using the bench shown in Fig. 9 (a). It is composed of the digital signal oscilloscope (DSO) Agilent DSO91204A (with 12 GHz bandwidth and 40 GSa/s sampling rate), the Agilent 1134A high performance probe, and an arbitrary function generator (AFG) AFG3102C from Tektronix. The AFG is used to trigger the pulse generator using a periodic square signal of 10 MHz. The probe was placed at the input of the comparator A, and used as a trigger for the DSO, which is connected to the pulse generator outputs. The eye diagram for a pulse with a FWHM around 60 ps over 1 k pulses is shown in Fig. 9 (b). The pulse-width duration presents a standard deviation of 1.6 ps and peak-to-peak of 8.33 ps. The fall and rise time (20-80 %) standard deviation is of 1 ps and 0.8 ps respectively. These values are in accordance with the jitter specifications of the high performance components employed. In order to compare with a commercial solution, the same jitter measurement was performed on a Novelda NVA-R640 radar kit, using as clock reference its own clock output for external triggering. In this case, a deterministic standard deviation of about 25 ps was obtained.

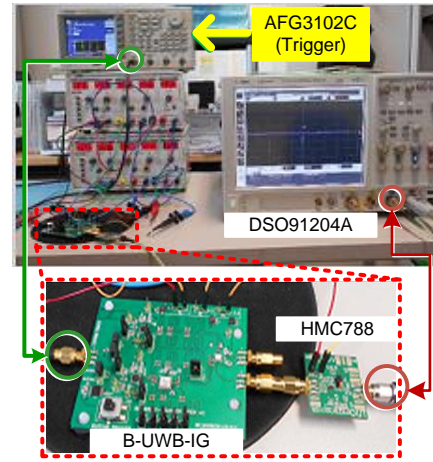


Fig. 10. Measurement setup of a single output of the B-UWB-IG amplified with the evaluation board for the HMC788 gain block amplifier.

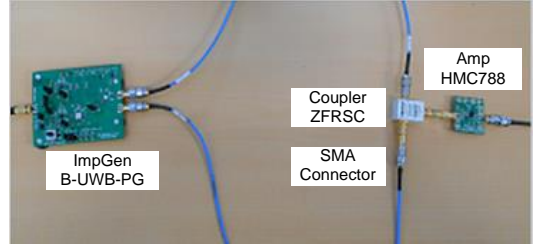
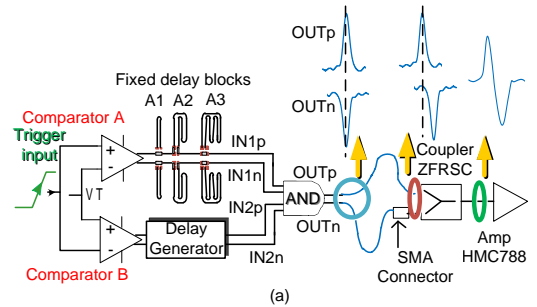


Fig. 12. (a) Schematic and (b) photograph of the monocycle pulse generator obtained from the combination of the balanced outputs of the proposed B-UWB-IG using a power combiner and a short delay line.

V. OUTPUT STAGE CONSIDERATION

A. Output Power Improvement

The maximum PSD/MHz of each single B-UWB-IG output, with VR equal to 0 V depends also of the PRF. If a lower PRF of 50 MHz is required, it is possible to increase the B-UWB-IG output power. The Analog Devices HMC788 gain block amplifier was used as a final stage of the proposed B-UWB-IG. It is characterized by an operative band from DC to 10 GHz, a gain of 14 dB, an input compression point of 6 dBm, and a noise figure (NF) of 7 dB. An evaluation board for the amplifier was fabricated on the same FR4 substrate of the pulse generator. The measurement setup is shown in Fig. 10 where the amplifier was connected in cascade with one output of the B-UWB-PG. The measured output voltage and the calculated output power spectral densities are shown in Fig. 11 (a) and (b), respectively. The PRF was retained constant to 50 MHz with respect to the case without the amplifier (Fig. 7) to show the increment of power output. The proposed solution

shows output amplitude peak to peak ranging from 1.1 V to 2.3 V, with VR yet equal to 0 V.

The use of the amplifier as final stage has degraded the jitter of the pulse generator. The same jitter measurement of Fig. 9 has been performed with the use of the amplifier at the B-UWB-PG output as shown in Fig. 10. The pulse generator was settled with a pulse width of 60 ps. The random period jitter standard deviation was increased to 2.18 ps with a peak-to-peak period variation of 13.35 ps over more than 1 k cycles. The increment with respect to the case without pulse generator (1.6 ps, 8.33 ps) is due to the PCB layout of the amplifier evaluation board [33], and also to the amplifier noise figure. The PCB was made of low cost FR4, and its layout was not optimized with electromagnetic simulations for matching the impedance of the amplifier at higher frequency.

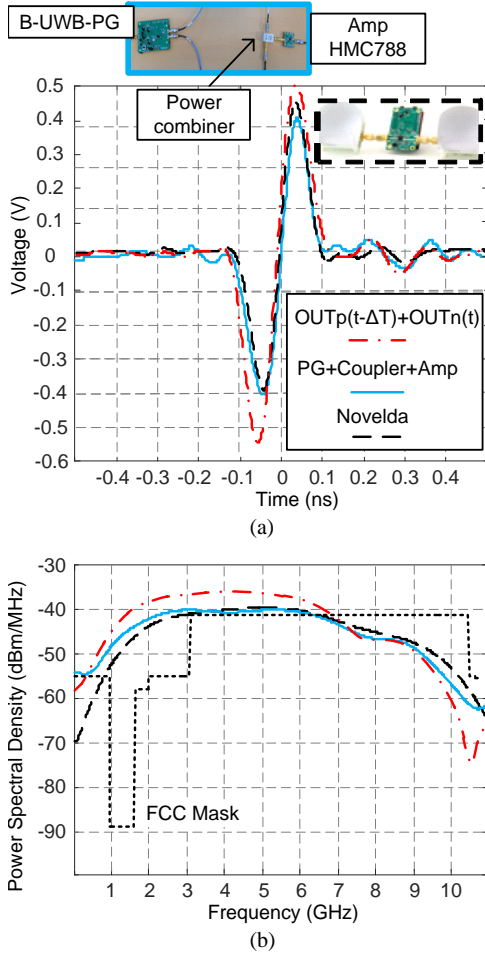


Fig. 13. In blue measurement of the proposed pulse generator with the wideband coupler ZFRSC-123 from Mini-Circuit, and the HMC788 amplifier (see Fig. 12) with VR equal to 0 V. In red dash dot line, the distinct single output measurement from the B-UWB-PG, called OUT_P and OUT_N from Fig. 12 (a), and summed in post processing with a delay of 14 ps executed with VR equal to 0.4 V. Finally in black dashed the Novelda NVA-R640 development kit pulse output: all in time (a) and in frequency (calculated) (b). The PRF was of 48 MHz equal to that of the NVA-R640.

B. UWB Shaping Network

To be compliant with FCC regulation in terms of power mask, the output of the proposed B-UWB-IG needs to be shaped [26]. In the regulation, the reported value of PSD/MHz, is a measure of equivalent isotropic radiated power

(EIRP), and therefore the characteristics of the transmitting antenna have to be taken into account. Outside of the 3.1-10.6 GHz band, the allowed PSD is strictly limited, especially between 1 and 2 GHz.

The UWB antenna itself can be used to shape the pulse [34]. It is also possible to use the antenna in combination with a band pass filter [32]. The design of this final stage can be complex. Indeed, usually commercial pulse generators do not present flexibility in terms of pulse-width, and they have a single output.

A typical Monocycle pulse, which is the first derivation of a Gaussian pulse, is commonly present at the transmitting port of commercial radars (such as the NVA-R640 kit from Section IV.B) The PSD maximum for a monocycle pulse is not located at zero frequency. By combining the balanced outputs of the proposed B-UWB-PG pulse generator, it is possible to generate a monocycle Gaussian pulse. In this way, the B-UWB-IG can be used with most commercial UWB antennas while respecting regulation.

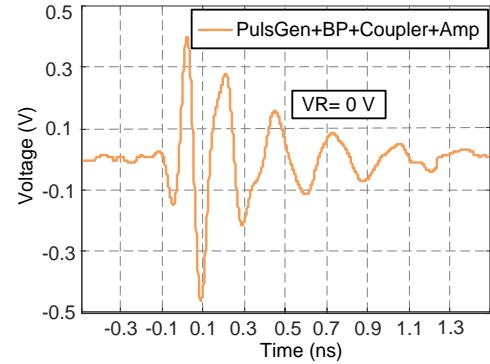


Fig. 14. Measurement in time domain of the setup of Fig. 12 with the ZFSC-2-9G+ band pass coupler.

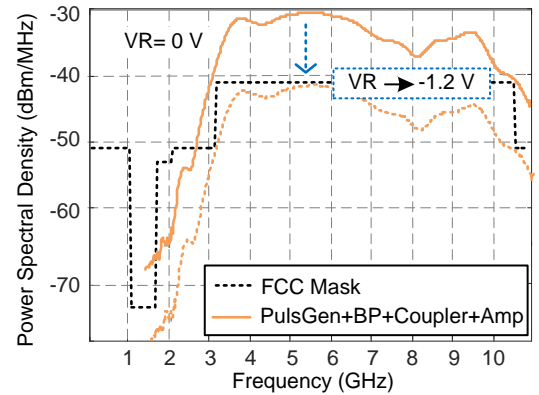


Fig. 15. Calculated PSD/MHz of measurement in Fig. 14 taking into account the gain of the Satimo QH2000 antenna, and FCC mask for UWB indoor applications. The PRF was of 50 MHz, a reduction of PRF and/or reducing the VR pin voltage allows for FCC regulation compliant.

A schematic of the combination process is shown In Fig. 12 (a). The Monocycle is obtained by doing the summation of two Gaussian pulses: one positive and one negative; the latter being slightly delayed in time. The wideband coupler Mini-Circuits ZFRSC-123 was used to perform the summation. The time shift between the two pulses was done using two cables with two different overall lengths. In this case, a 21 mm

TABLE I
MAIN PARAMETERS B-UWB-IG

Model/Characteristics	[14]	[29]	[30]	[31]	[32]	[16]	[34]	This work
Technology	CMOS 90 nm	CMOS 180 nm	CMOS 65 nm	CMOS 130 nm	CMOS 40 nm	COTS	COTS	COTS
Modulation	OOK	OOK	PPM + DB-BPSK	OOK	-	OOK	OOK	OOK + PAM + PWM
Pulse Output	Gaussian	Monocycle	Gaussian	Gaussian	Triangle	Gaussian	Gaussian	Gaussian
Pulse Width (ps)	[50 - 135]	-	200	[2,000 - 25,000]	[660 – 3,800]	500	820	[60 - 325]
Pulse Amplitude over 50 Ω (V)	Variable	-	-	1	[0.640 – 0.560]	0.5	-	[0.03 – 0.6]
PRF (MHz)	200	[100 - 1000]	200	250	100	100	20	8,300 (Pulse width of 60 ps)
Bandwidth – 10 dB (GHz)	-	[3.2 – 8.2] – [4 – 9] ^a	3 channels in [3.1 – 4.6] of 0.5	-	-	-	[0 – 2.8]	[0 – 10.2] – [0 – 2.2]
Energy/Pulse (pJ)	-	[2.6 – 0.76] ^a	30	[30 - 48]	6.2	-	-	-
Power/Consumption (mW)	12	[0.26 – 0.76] ^a	-	-	-	-	-	1,040
Area	0.008 mm ²	0.09 mm ²	0.182 mm ²	0.027 mm ²	8,200 μ m ²	-	-	8.5 cm \times 7 cm

^a Simulation

coaxial connector adds a small delay to the bottom chain (see Fig. 13 (b)). To compensate the insertion loss of the coupler, which is of about 10 dB, the same HMC788 amplifier (see Section V.A) was employed as a final amplification stage. In Fig. 13 the result in blue is compared with the NVA-R640 commercial radar pulse output in black dashed line. Both responses are similar, showing that the B-UWB-IG can be easily tuned to provide Monocycle output. In case of our prototype, the pin VR was at 0 V and therefore the output amplitude could be yet increased using the maximum value of 0.4 V. The PRF was of 48 MHz, equal to that one of the NVA-R640 radar.

The coupler presents a high insertion loss due to its large band, from DC to 12 GHz. With a lower insertion loss coupler, and using 0.4 V for VR, it would be possible to eliminate the final amplifier.

In Fig. 13 is also shown the distinct single output measurement from the B-UWB-PG (red dash dot line), called OUT_P and OUT_N from Fig. 12 (a) summed with a delay of 14 ps. They were obtained for a VR tension of 0.4 V. The signal in time and frequency presents almost the same performance as the case with the amplifier (blue curve). Therefore if a low insertion loss coupler is used the amplifier is not mandatory. With the similarity between B-UWB-PG and novelda NVA-R640 measured curves, this B-UWB-PG configuration may readily respect the FCC mask if the same sinus UWB antenna of the novelda NVA-R640 are used. Indeed in Fig. 13 (b) the gain of the antenna has to be added to estimate the EIRP, and the NVA-R640 claims to be compliant with the FCC mask.

As final example, the Satimo dual polarized open boundary quad-ridge horn QH2000 antenna, which has a frequency range between 2 and 32 GHz, was employed as transmitting antenna. The same configuration of Fig. 12 (a) was used, where the coupler was substituted with the Mini-Circuits ZFSC-2-9G+ band pass coupler. It has a bandwidth between 3.5 and 9 GHz, and therefore attenuates the part of the signal lower than 3.5 GHz helping to respect the FCC UWB mean power mask for indoor application. The filtering effect of the

new coupler is clearly visible in Fig. 14. The response in frequency domain (calculated), where the gain of the antenna was taken into account for the EIRP estimation, is shown in Fig. 15. The PRF was retained at 50 MHz, and the FCC mask is also shown in dashed black line. As it can be observed, to be compliant with regulations the voltage at VR pin may be tuned. It is also possible to decrease the PRF.

The main characteristics of the proposed pulse generator are summarized in table 1, and put in relation with similar realizations available in literature. Some realizations are based on integrated solutions while the others on COTS components. Our pulse generator showcases higher performances compared with the others COTS realizations, while for integrated solutions a higher flexibility is obtained. Its power consumption is higher respect to integrated solutions due to the use of high performance lumped components.

VI. CONCLUSION

This paper has presented a potentially ultra-low-jitter fully tunable baseband pulse generator for real and equivalent-time UWB applications. COTS components and low-cost FR4 substrate have been used for cost and flexibility reasons. The generator is based on high frequency logic gates and two comparators. It can be triggered by a low-frequency TTL-CMOS digital signal. A delay generator and variable length transmission lines permit to tune the pulse-width from 325 ps to 60 ps. A pin on the AND gate allow for amplitude modulation (VR). The measured random period jitter over 1k cycles is in the order of 2 ps. The generator outputs two independent balanced pulses. By combining the pulses, it has been shown that a commonly used monocycle pulse can be obtained. The proposed solution is flexible and permits to design a shaping network with off-the-shelf components to respect regulations. For some applications, the use of COTS component is a huge advantage compared to an integrated solution, because its implementation, modification, and redesign is easy and low-cost. Also it can be integrated in large onset UWB systems. The actual design can be improved using digitally controlled RF switches instead of 0 Ω resistors

to select between A1-A2-A3. Higher permittivity substrate, with better performance at higher frequency, can be used to reduce the B-UWB-IG dimensions, the transmission loss, and the jitter. The reduction of the AND gate output mismatching with PCB layout helps to increase B-UWB-IG performances at higher frequency.

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