HAL
open science

Parasitic elements modeling and experimental identification in a gan hemt based power module

Xiao Shan Liu, Bertrand Revol, François Costa

To cite this version:

Xiao Shan Liu, Bertrand Revol, François Costa. Parasitic elements modeling and experimental identification in a gan hemt based power module. 19 ème Colloque International et Exposition sur la Compatibilité ÉlectroMagnétique (CEM 2018), Jul 2018, Paris, France. hal-02051418

HAL Id: hal-02051418

https://hal.science/hal-02051418v1

Submitted on 27 Feb 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

PARASITIC ELEMENTS MODELING AND EXPERIMENTAL IDENTIFICATION IN A GAN HEMT BASED POWER MODULE

X. Liu[1], B. Revol[1], F. Costa[1,2]

[1]Laboratoire SATIE, ENS Paris Saclay, Fr-94235 Cachan
[2]Université Paris-Est Créteil, Fr-94000 Créteil

Abstract. In this paper, the parasitic elements of a GaN based power module are investigated. Because the very high-speed switching of GaN high electron mobility transistors leads to overvoltage, conducted and radiated emissions, it is crucial to manage accurately the routing of the power module in order to minimize parasitic capacitances and inductances. The paper focuses on the prediction of these parasitic effects and their comparisons to measurements. In this approach, the difficulty lies in the determination of very small values of the parasitic elements which requires specific operating for calibration and measurements.

I. INTRODUCTION

The emergence of wide bandgap GaN high electron mobility transistors (HEMT) is promising for power electronics performances if their packaging is matched to their very high switching speed **[1], [2]**. Actually, only discrete components can be found out of-the-shelve with low-inductance packaging (PQFN or similar), but no power module are already available. Our purpose is to study such a new type of module exhibiting low parasitic elements and including capacitors for HF differential and common mode decoupling, in order to get the best performances as possible and to limit conducted high frequency emissions **[3]**. For this objective, we have realized a prototype of power module using discrete HEMT's as dies (GaN System GS66508P) in order to develop our simulation and characterization methodologies. The first part of the paper will describe the bare module and how to calculate and measure the parasitic capacitances and inductances. In particular, it will be shown how to extract the module parasitic capacitances even if the dies are soldered in. Comparisons will be presented that validate the methodology. The second part will present the electrical model of the module including decoupling ceramic capacitors and how it is used for EMI simulation of the CM current issued of the module.

II. BARE MODULE MODELING

A bare module of a GaN-based switching cell was designed in the lab with neither in-module multilayer ceramic capacitors (MLCC) nor semiconductor devices. Its layout is presented in Fig. 1, it is modeled as the circuit in Fig. 2. C_{M+}, C_{M-} and C_{MA} are the main parasitic capacitances and L_{M+}, L_{M-} are the equivalent parasitic inductances of the copper tracks of the DC bus. The parasitic elements can be either calculated by a numerical approach (3D PEEC method) such as ANSYS Q3D (c.f. II.1-A) or be measured directly by an impedance analyzer with proper protocol. It should be noted that both methods lead to some error. However, results-matching between the two methods makes a tendency to a good estimation. Last but not the least, their values will be finally evaluated by comparison between circuit simulation and measurement in a real test bench.

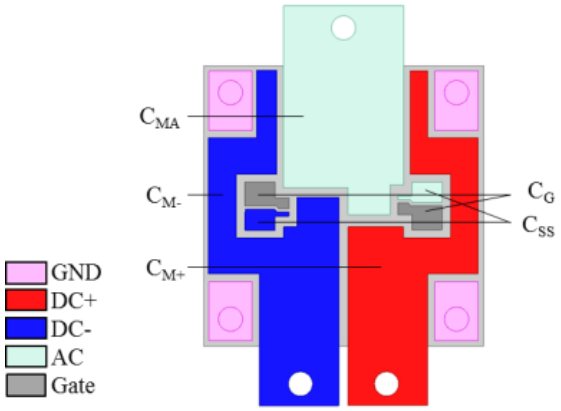


Fig. 1: Layout of our power module (4 x 4 cm), capacitances to be calculated in Q3D.

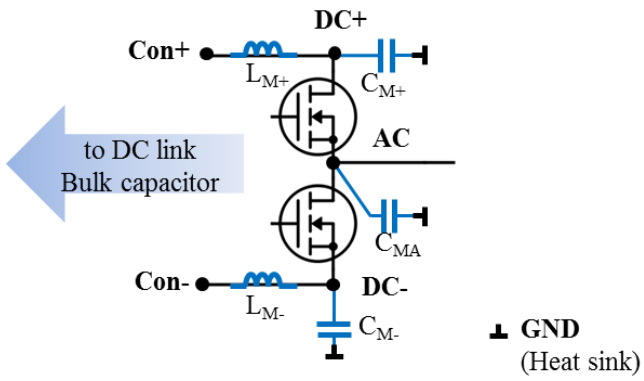


Fig. 2: Parasitic model of our prototype module.

II.1. Parasitic capacitances calculation – C_{M+}, C_{M-} and C_{MA}

a - Numerical extraction

ANSYS Q3D Extractor takes into account the 2D or 3D structure of electronic packaging or PCB and the related insulation materials' properties, uses PEEC method, to compute the partial inductive (partial self-inductance and mutual one) and capacitive elements. The module's layout can be imported from the PCB design software EagleCAD to ANSYS Q3D in proper way. The relative permittivity ε_r of FR4 epoxy is calculated by the measurement of capacitance of a PCB with a known surface and its value is estimated as 5.6 for our prototype module. Fig. 1 and Fig. 1 show all parasitic capacitances to be extracted in Q3D. Their values are shown in Tab. 1. Dielectric losses have been ignored all over this study due to their low influence in the considered frequency range.

The capacitances between different copper pads on top layer are too tiny and therefore they will be ignored. It should be noted that C_{SS} (capacitance between the kelvin source pad and GND) should be added with C_{M-} and C_{MA} respectively since they are connected inside the power device's package.

Tab. 1: Q3D extraction of parasitic capacitances in our bare module (unit: pF)

C_{M+}=38.2	C_{M-}=41.7	C_{MA}=34.9	C_G=2.5	C_{SS}=2.0

b - Impedance measurement

The parasitic capacitances can be directly measured one by one in the bare module without any semiconductor power chip. However, the bare module (only layout and interconnections, no semiconductors) is not often achievable. The measurement approach below provides the capability to measure parasitic capacitances directly in a completed module including semiconductors. In a first place the two GaN devices should be short-circuited between the gate and the HEMT kelvin source so that each device is equivalent to a capacitance between drain and source with a value of C_{OSS} (C_{DS}+C_{GD}) at low V_{DS} voltage (~ 500 pF for GS66508P). Therefore there are 5 unknown (C_{M+}, C_{M-} and C_{MA}) or roughly known (C_{OSS} of high-side and low-side devices) capacitances between the DC+, DC-, AC and GND potentials (Fig. 3).

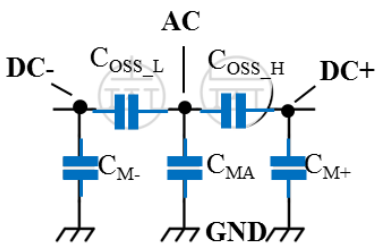
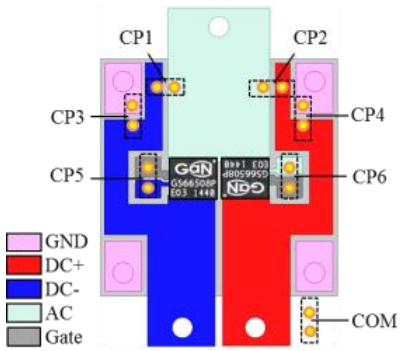


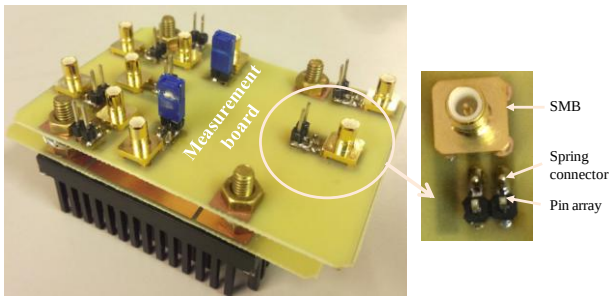
Fig. 3: Capacitances between different terminals.

Since the error of several pF between the C_{OSS} of high-side device and the low-side one (mostly due to the manufacturing process) can make a difference compared to the values of C_{M+}, C_{M-} and C_{MA} (according to the Q3D calculations), it is advised for precision purpose to treat the two C_{OSS} as two unknown coefficients – C_{OSS_H} and C_{OSS_L}. Finally 5 capacitance measurements with proper short- or open-circuit operations should be done in order to determine the 5 unknown capacitances between terminals, as discussed hereafter.

In order to measure the capacitances of the module mentioned above without any soldering, a specific board has been realized. It consists of 2×1 spring loaded connector arrays used to take contacts on different terminal areas on the top layer of the module. Each pair of those connectors allows to measure or to short-circuit the capacitance between two terminals. All contact points are shown in Fig. 4a. Each pair of the spring connectors is in parallel with a SMB adaptor for impedance measurement and a 2×1 pin array for short-circuits convenience by a jumper. All the connectors are configured in a PCB which is fixed above the power module via four screws (Fig. 4b). It should be noted that COM contact points (Fig. 4a) are used for the measurement of the stray capacitance in the spring connector together with the SMB connector, which should be compensated (subtracted) from the measurement results.



(a)



(b)

Fig. 4: Contact points for capacitances' measurement (a) and measurement board (b).

II.2. Preparation & Measurement method choosing

The measurement procedure is presented hereunder. The contact points CP5 (gate and kelvin source for low-side GaN device) and CP6 (gate and kelvin source for high-side GaN device) are short-circuited before all

measurement; in addition, since the "to be measured" capacitances' value is hundreds of pF, corresponding to very high impedance at the frequency range up to 30MHz, the "GP series" impedance measurement configuration (Gain-phase with series-through) will be used with our network analyzer (Keysight 5601).

a - Calibration & Compensation:

After O/S/L calibration to the end of the cable, at least an "OPEN" compensation should be done at the COM contact point, in order to eliminate the test fixture stray capacitance between two spring connectors and the SMB connector. The value is measured as 2.0 pF.

Measurement 1:

Short-circuiting CP1 (DC- to AC) and CP2 (DC+ to AC); measuring capacitance of CP3 or CP4 (DC+ to GND or DC- to GND).

$$C_{M+}+C_{M-}+C_{MA}=126.0pF \quad (1)$$

Measurement 2:

Short-circuiting CP2 (DC+ to AC) and CP3 (DC- to GND); measuring capacitance of CP4 (DC+ to GND).

$$C_{OSS_L}+C_{MA}+C_{M+}=565.4pF \quad (2)$$

Measurement 3:

Short-circuiting CP1 (DC- to AC) and CP4 (DC+ to GND); measuring capacitance of CP3 (DC- to GND).

$$C_{OSS_H}+C_{MA}+C_{M-}=571.2pF \quad (3)$$

Measurement 4:

Short-circuiting CP1 (DC- to AC) and CP3 (DC- to GND); measuring capacitance of CP4 (DC+ to GND).

$$C_{OSS_H}+C_{M+}=525.9pF \quad (4)$$

Measurement 5:

Short-circuiting CP2 (DC+ to AC) and CP4 (DC+ to GND); measuring capacitance of CP3 (DC- to GND).

$$C_{OSS_L}+C_{M-}=534.4pF \quad (5)$$

Solving equations (1) to (5), the results are shown in Tab. 2.

Tab. 2: Measured parasitic capacitances in our module (unit: pF)

C_{M+}=40.3	C_{M-}=47.5	C_{MA}=38.2	C_{OSS_H}=485.6	C_{OSS_L}=486.9

It should be noted that the measured results of C_{M-} and C_{MA} have included not only the C_{SS} but also the C_G mentioned in the Q3D modeling part. Therefore, their values should be compared with the sum of C_{M-}/C_{MA}, C_G and C_{SS} calculated in Q3D. Tab. 3 shows the comparison results. The errors are totally acceptable.

Tab. 3: Comparison of module parasitic capacitances by Q3D and by measurements

	$C_{M-}+C_G+C_{SS}$	$C_{MA}+C_G+C_{SS}$	C_{M+}
Q3D extraction	46.2pF	39.4pF	38.2pF
Measured	47.5pF	38.2pF	40.3pF

II.3. Parasitic inductances calculation – L_{M+} and L_{M-}

a - Numerical extraction

The partial inductances of the copper tracks L_{M+} and L_{M-} are illustrated in Fig.5 and their values can be calculated in Q3D as 11 nH for each.

Tab. 0-4: Q3D calculated L_{M+} and L_{M-} values

L_{M+}=11 nH	L_{M-}=11 nH

b - Impedance measurement

There is no easy way to measure directly the aforementioned inductances. However, L_{M+} and L_{M-}'s values can be verified indirectly after adding the bulk capacitor C_{buk}. Two test points are set as TP+ and TP- as shown in Fig. 5a. The impedance between the two test points should be the paralleling of the impedance on the left side and the one on the right side, thus $L_{P1}+C_{OSS}/2$ in parallel with $L_{P2}+L_{C+}+L_{C-}+L_{C0}+C_{BUK}$ as shown in Fig. 5b, where $L_{P1}+L_{P2}=L_{M+}+L_M$. Since $L_{C+}+L_{C-}+L_{C0}+C_{BUK}$ and C_{OSS} are already known, $L_{P1}+L_{P2}$ should be able to be deduced.

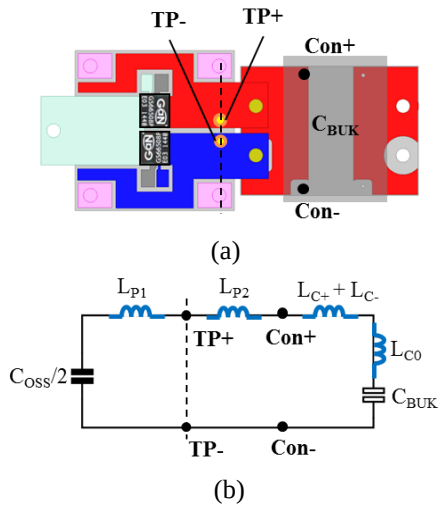


Fig. 5: L_{M+}/L_{M-} measurement test points setup (a) and the equivalent circuit (b).

The measurement result and the fitted model are shown in Fig. 6. The first magnitude valley is due to the resonance between the C_{BUK} (30µF) and the $L_{C+}+L_{C-}+L_{C0}+L_{P2}$; the second one is due to the resonance between the $C_{OSS}/2$ (30pF) and the L_{P1}.

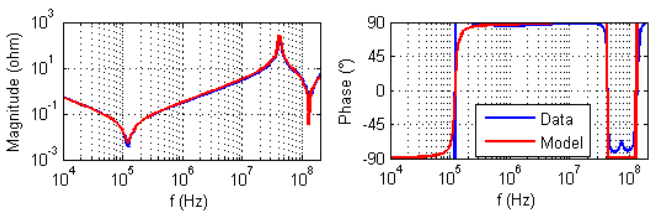


Fig. 6: Comparison between the fitted model and impedance measurement between TP+ and TP-.

L_{P1} and L_{P2} are found as 6 nH and 15 nH respectively. The sum of these two measured inductances (21 nH) is compared with the Q3D calculated ones, as show in Tab. 5.

Tab. 5: Comparison of calculated and measured $L_{M+}+L_{M-}$

	Q3D extraction	Measurement
$L_{M+}+L_{M-}$	22 nH	21 nH

II.4. Final model of the bare module with DC link bulk capacitor

The final module's model together with the DC link capacitor is presented in Fig. 7. There is an extremely large power loop inductance (over 60 nH) in which the bulk capacitor and the power module terminals (including the capacitor supporting PCB board and the interconnection screws) contribute respectively around 35~40 nH and 22 nH.

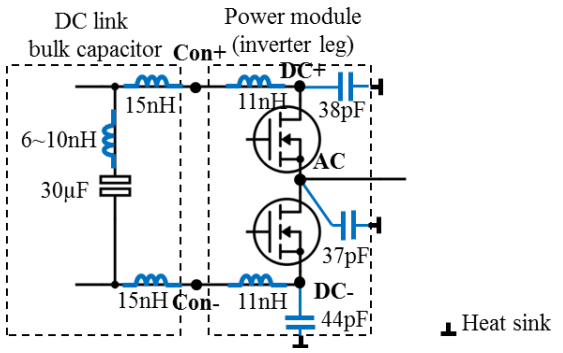


Fig. 7: Values of main parasitic elements in bare module with the DC link capacitor.

III. IN-MODULE CAPACITORS MODELING

As previously exposed, it may be efficient to include a first stage of HF decoupling directly inside the module in order to limit overvoltage on the DC bus and to partially filter CM currents. This CM and DM filtering is shown in fig. 8a: three C_X capacitors in 2220 package are in parallel on the DC bus while two C_Y capacitors in 1206 package are connected between each DC side and the backside ground.

a - Capacitors C_X

Three C_X capacitors – C_{X1}, C_{X2} and C_{X3} – and the GaN devices are modeled in Q3D as shown in Fig. 8a. The GaN devices are short-circuited. The parasitic inductances between A+ and A- / B+ and B- / C+ and C- are calculated respectively as 2.5 nH, 3.4 nH and 4.3 nH. These three values should be added with the GS66508P GaN devices' package parasitic inductance which is 0.5 nH. Therefore, the three power loops can be modeled as distributed partial inductances as shown in Fig. 8b. ESL is the equivalent series inductance of the 2220 package of the C_X capacitor. According to **[3]** it can be estimated reasonably as 0.5nH.

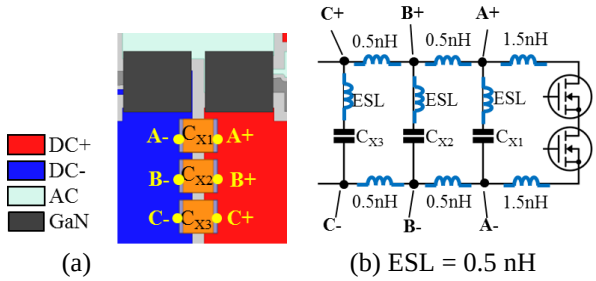


Fig. 8: Power loop for different C_X capacitors (a) and the equivalent circuit (b).

b - Capacitors C_Y

The loop inductance formed by the two C_Y capacitors and the GaN devices and the backside of the power module (GND) is illustrated in Fig. 9. This loop (in yellow dashed line) inductance is calculated by Q3D as 5.5 nH. Being added with 0.5 nH from the two GS66508P packages and with 2 nH **[AVX]** from the 1206 package of two C_Y capacitors, the total loop inductance is 8 nH. Therefore, each C_Y capacitor's partial inductance is distributed equally as 4 nF as shown in the equivalent model of Fig. 10.

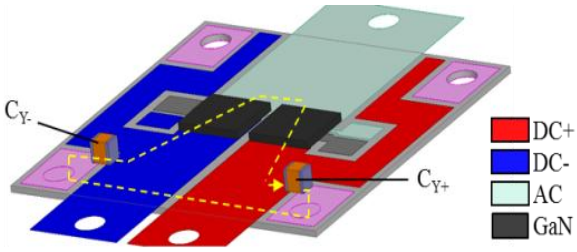


Fig. 9: Illustration of the inductive loop of C_{Y+}/C_{Y-} capacitors.

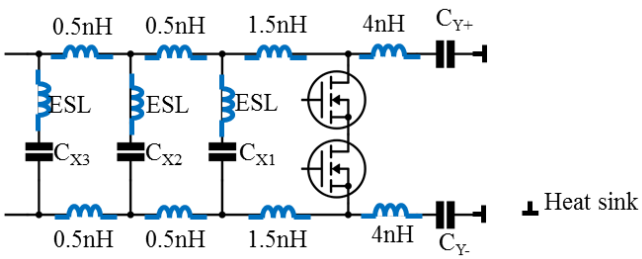


Fig. 10: Parasitic inductance with C_X and C_Y in our module.

III.2. Final model of the module with in-module ceramic capacitors

At last, the full circuit model of the module including C_X and C_Y capacitors with DC link bulk capacitor is shown in Fig. 11, with parasitic elements in blue color and discrete components in black color.

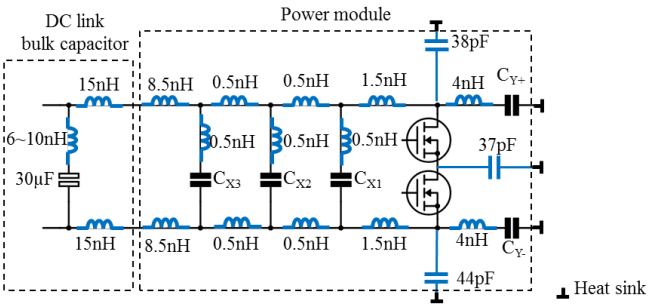


Fig. 11: Full model of SATIE module with in-module capacitors.

This full model can be used now to simulate any kind of electrical quantities regarding the working of the module and/or EMI aspects [5]. A specific behavioral model of the GaN components was previously developed in [5]. For example, Fig. 12a presents a comparison of the simulated and measured spectra of the CM current issued of the module without any decoupling capacitor. Fig. 12b shows the impacts on the first spectrum of the C_Y decoupling capacitors for two different values.

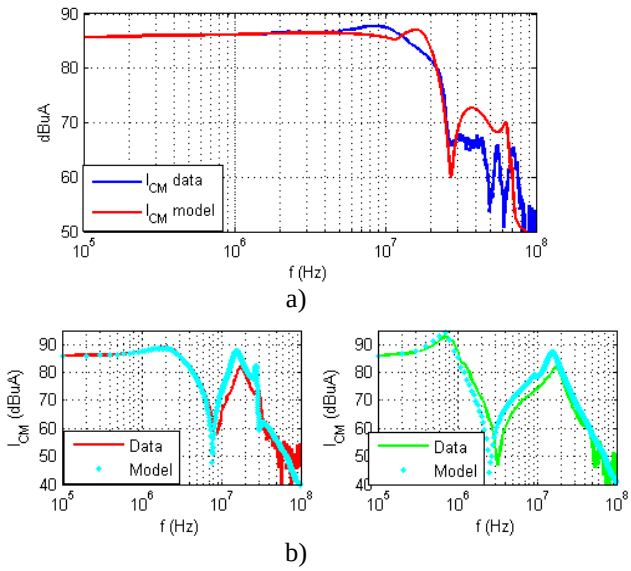


Fig. 12: Spectra of the module CM current,

a) module without any local decoupling, blue: measurement, red: simulation.
b) left : C_y=0.7 nF, right C_y = 7 nF.

These curves show good agreements between the predictions and the measurements in a very large bandwidth up to 100 MHz which is the limit fixed for circuit modeling of this study. Over this frequency, modeling would require to take into account other effects not taken into account here over like propagation and radiating effects.

IV. CONCLUSION

In this paper, an experimental method to extract the parasitic elements of a GaN based power module has been presented. This specific method is achieved while power dies are already soldered in the module, requiring an adequate calibration setup specifically dedicated to the module under study. The values of the measured elements have been compared to the ones extracted by a numerical tool; good matching's have been observed. Moreover, the electrical model obtained with these techniques enable very accurate simulations of any electrical or EMI quantities issued of the module over a large frequency range. At last, the method presented hereunder can be extended to other circuits different from power modules but including semiconductors.

ACKNOWLEDGMENTS

This work has been supported by the PIA MEGaN.

REFERENCES

[1] Z. Zhang et al., "*Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration*," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 2534-2541.

[2] D. Reusch and J. Strydom, "*Understanding the Effect of PCB Layout on Circuit Performance in a High-Frequency Gallium-Nitride-Based Point of Load Converter*," in IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 2008-2015, April 2014.

[3] E. Wolfgang, "*A race towards the lowest inductive power module*", report on the conference CIPS 2014.

[4] Jeffrey. Gain, "*Parasitic inductance of multilayer ceramic capacitors*", Technical information, AVX Corporation.

[5] Xiaoshan Liu, "*Methodology for EMC Analysis in a GaN Based Power Module*", PhD thesis, Université Paris Saclay, dec. 2017.