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Fast active cycling power test bench using dedicated modules assemblies for studying wire bond ageing

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Abstract

This paper presents the design of specific samples dedicated to the test of power bond wires (300 μm diameter). The aim is to totally control the test conditions on each bond wire while reducing drastically the power consumption. The samples are integrated in a particular test bench that allows conducting easily ageing tests with an on-line monitoring. The main idea is to solder Power MOSFET dies used as heating sources on an Integrated Metallic Substrate having a high thermal impedance. First, the paper describes the design process, aided by Finite Element simulations. A second part focuses on the realization of the samples and of the test bench. Finally, the first ageing results are presented.

1 Motivations for the development of specific power-cycling test samples

The general context of works presented here is the ageing of Al bond wires in semiconductor power modules operating under thermal power cycling conditions. The experimental apparatus described below constitutes the experimental support of a general study concerning the thermo-visco-elasto-plastic behavior of the bond wire with a final target that is the introduction of degradation modelling [1]. Such a thermo-mechanical study requires to get experimental data for the adjustment of the modelling parameters. Therefore, power-cycling tests have to be carried out in a realistic range of die temperature variation ΔT_J (10°C to 50°C). That can lead to very long test duration to observe degradations. To reduce the test duration, the increase of the power cycling frequency can be considered [2][3] if the ageing behavior observed in real conditions (low frequencies) is preserved.

Several types of power cycling benches have been build and used for 10 years to test IGBT power modules in realistic operating conditions [4][5][6]. Unfortunately, this test approach is expensive and time consuming. Despite operation in back-to-back mode [5], the power consumption remains high and increases with the power cycling for a given ΔT_J . This is due to the low thermal impedance of

the industrial power modules (low die/base-plate thermal resistance and base-plate thermal capacity) that are logically designed to minimize the temperature increase and variation.

Nevertheless, these test benches have allowed obtaining many results in various conditions of power cycling. **Fig. 1** shows a summary corresponding to ageing of the same power module with different cycling frequencies, for a ΔT_J of 50°C. In all cases, the degradations only concern the bond feet. It can be observed that the lifetime increases from frequencies higher than 1Hz. This probably means that the degradation process changes when the dynamic of temperature variation changes, sign of a viscous contribution in the thermo-mechanical behavior.

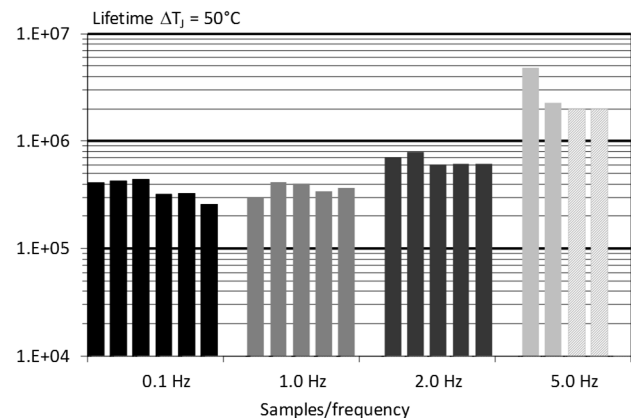


Fig. 1: Lifetime vs power cycling frequency

If these previous results gives interesting information on the bond wire ageing, they are not sufficient for the thermo-mechanical study mentioned above. Therefore, numerous additional results are needed. Considering the complexity of power cycling test with industrial power modules, it had been decided to design a new and simplest test bench using specific test samples.

2 Design of a specific power cycling test sample

The main idea leading to the design of the specific samples is the increase of the thermal impedance under the dies that support the bond wires to be tested. This makes it possible to conduct the test with a very low energy consumption ($P = 12\text{W}/\text{die}$ for $\Delta T_J = 50^\circ\text{C}$ and cycling frequency $F_c = 5\text{Hz}$ whereas the test of power module would require $125\text{W}/\text{chip}$ under the same conditions). The dies constitute the sources heating the bond wires while the mechanical nature of the bond foot is preserved. Only one main bond wire is connected to each die, what allows following its ageing by an appropriate monitoring.

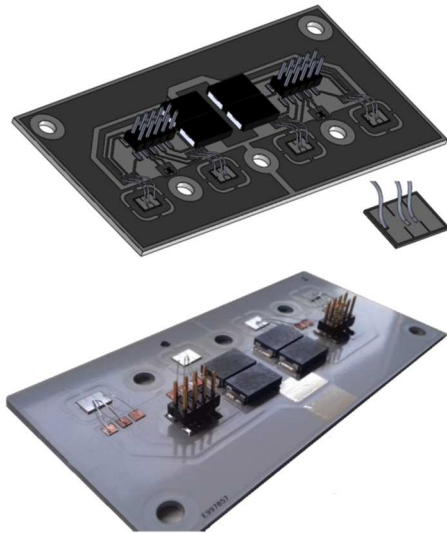


Fig. 2: Views of the Insulated Metal Substrate (IMS)

In this approach, the die technology does not matter : MOSFET dies have been chosen due to their control simplicity. Four dies are soldered on an Insulated Metal Substrate (IMS) including a $35\mu\text{m}$ copper layer, a $100\mu\text{m}$ FR4 insulation and a 2mm aluminum base plate (see **Fig. 2**). This common technology makes very easy the fabrication of specific laboratory samples.

Due to the low IMS FR4 thermal conductivity, the thermal impedance is high as expected to reduce the power consumption required by the power cycling.

To obtain the desired junction temperature profile, the power injected in the dies is controlled while the substrate temperature is regulated by an air-flow cooling system using a PT 1000 sensor located on the top of the SMI.

Finite Element electro-thermal simulations have been used to precisely define the implementation of the dies on the SMI. These simulations are based on the following heat diffusion equation :

$$\rho C \frac{\partial \theta}{\partial t} - k \Delta \theta = S \quad (1)$$

where ρ , C , θ are respectively the density in $[\text{kg} \cdot \text{m}^{-3}]$, the heat capacity $[\text{J} \cdot \text{kg}^{-1} \cdot \text{K}^{-1}]$ and the temperature variation in $[\text{C}]$.

S is the sum of the heat sources per unit volume. Here the only source is the die losses due to Joule effect in R_{dson} .

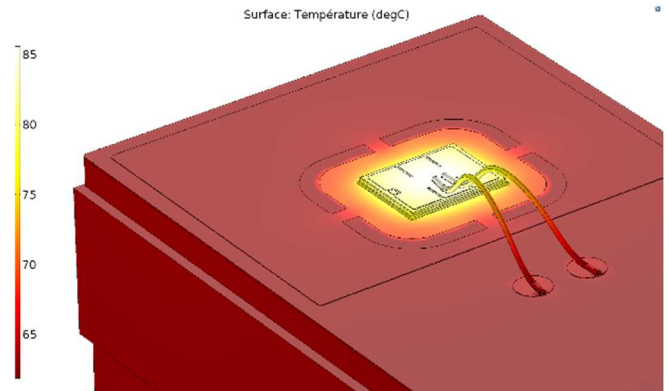


Fig. 3: EF electrothermal simulation for one MOSFET die

Thanks to the help of EF simulation, trenches have been placed and sized in the copper zone under each die to reduce the thermal coupling between the four dies. By limiting in this way, the side thermal diffusion, the temperature profile of each die is not affected by the heating of the other dies. This property is important for the future tests because the possible failure of one die should not affect the test of the other dies. The **Fig. 3** shows a simulation result that confirms the good thermal insulation induced by the trenches.

In addition, the EF simulation are used to define the electrical stresses to be applied for obtaining a given junction temperature profile.

The image of **Fig. 4** shows an IR thermal imaging of the sample realized under the specifications defined by the previous simulations. The four dies are here permanently heated by a DC current. This view confirms the good thermal insulation of the dies.

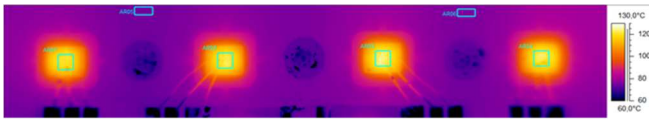


Fig. 4: Thermal image of the test sample

Then, different preliminary tests have been performed to identify the electrical parameters associated to a given junction temperature profile.

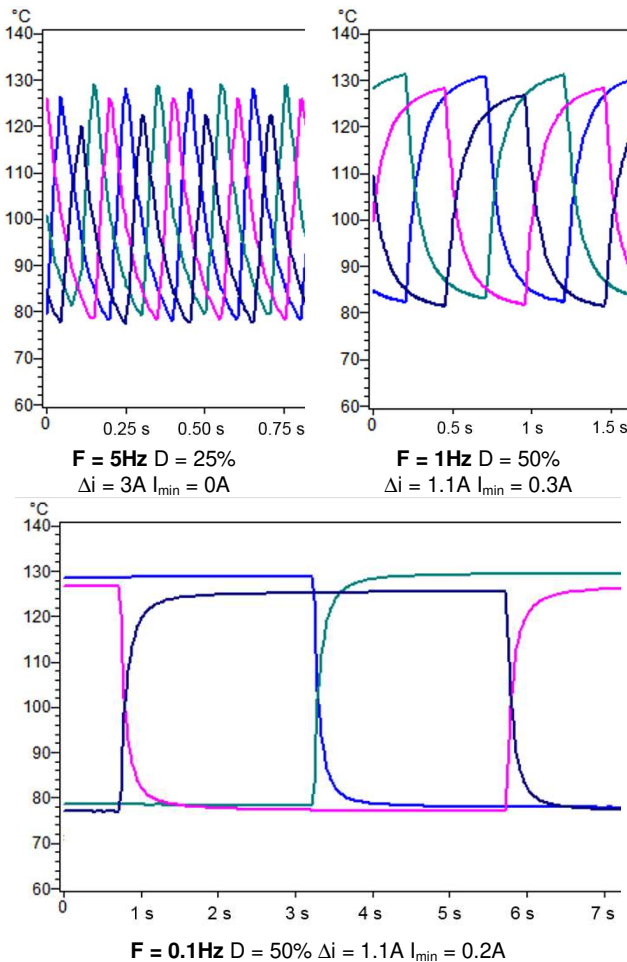


Fig. 5: Examples of junction temperature profiles

Rectangular current waveforms have been imposed in the dies under a constant voltage of 12V.

These waveforms are defined by :

- A minimal value I_{min}
- A current variation Δi (from I_{min})
- A duty cycle D

Some results obtained with thermal imaging are given **Fig. 5**, for different values of the cycling frequency. The temperatures are measured on the die center.

3 Test bench presentation

The test bench is constituted of several test blocks. A test block supports one sample (four dies) and includes a gate driver/analog regulation board, a microcontroller board and the cooling system. A Labview application achieves the supervision and the data acquisition during the test.

The MOSFETs operate in linear mode under constant voltage V_{DS} (12V), the drain current being controlled by the gate-source voltage. This method allows controlling precisely and independently the power injected in the four dies. As already mentioned, rectangular current waveforms have been chosen to adjust the temperature profiles. They are generated by an analog regulation acting on each gate-source voltage (driver board) from analog control signals elaborated by an STM32F4 microcontroller board. The cooling system consists of an air box, a heatsink with thick fins and a fan. A numerical speed regulation of the fan allows setting a temperature reference on the SMI. A plastic cover protects the dies and the bond wires.

All the operating parameters (current shape, reference temperature, protections) are managed by the LabVIEW application.

To follow the ageing of the bond wires, automatic sequential measurements of the contact resistance have been implemented. For this purpose, two source bond wires are mounted on each die. A main bond wire conducts the source current while an auxiliary bond wire is used as a reference electrode to periodically measure the contact resistance of the main bond wire and to monitor its evolution during the power cycling. The voltage drop information is measured by the microcontroller board and transmitted to the LabVIEW control system in order to calculate the contact resistance and to analyze its variation throughout the test. A GUI Matlab program displays in real-time the resistance evolution.

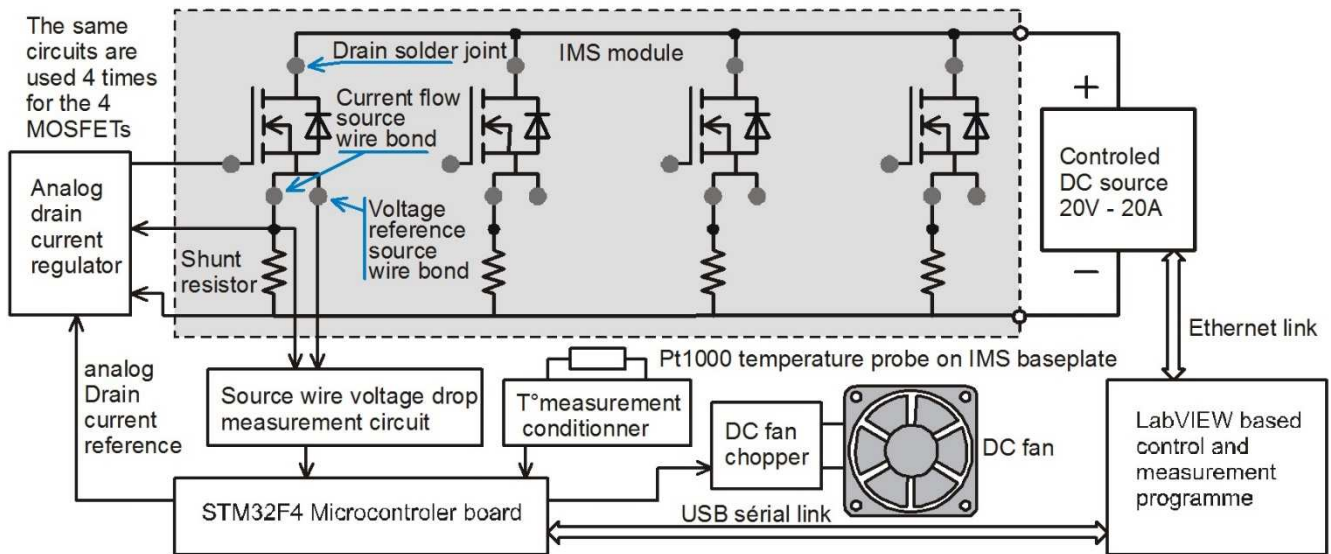
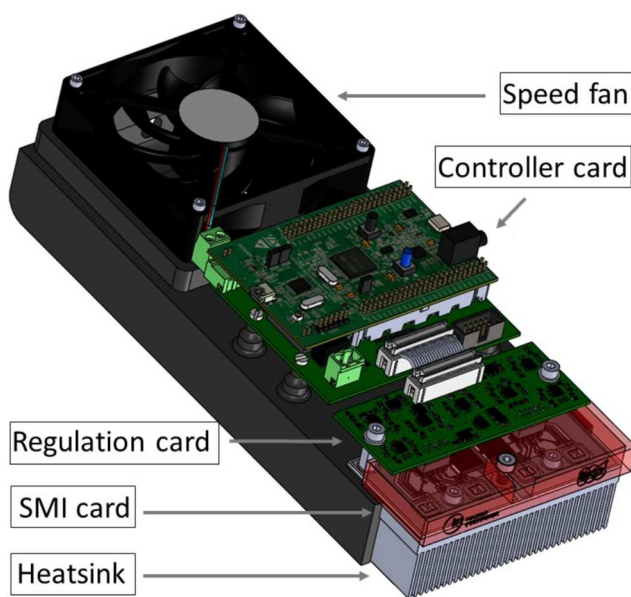


Fig. 5: Test bench simplified schematic. The analog circuits are here only drawn for one MOSFET.



3D Implementation of the test bench



Final realization

Fig. 6: Views of the test blocks

Views of 3D implementation and of the final realization are given **Fig. 6**.

4 First results

4.1 Results presentation

A first test campaign has been carried out with two samples. The test has been performed with $\Delta T_J = 50^\circ\text{C}$, a minimal temperature of 80°C and a

cycling frequency of 1Hz. These parameters have already been applied in test of IGBT modules.

Therefore, comparisons are possible. **Fig. 7** shows the junction temperature profile applied in that test.

The electrical conditions are the following :

- A square wave current varying between 0.5A and 1.8A with a duty cycle of 50%.
- A constant DC voltage of 12V.

The power consumption is limited to 13.8W per die.

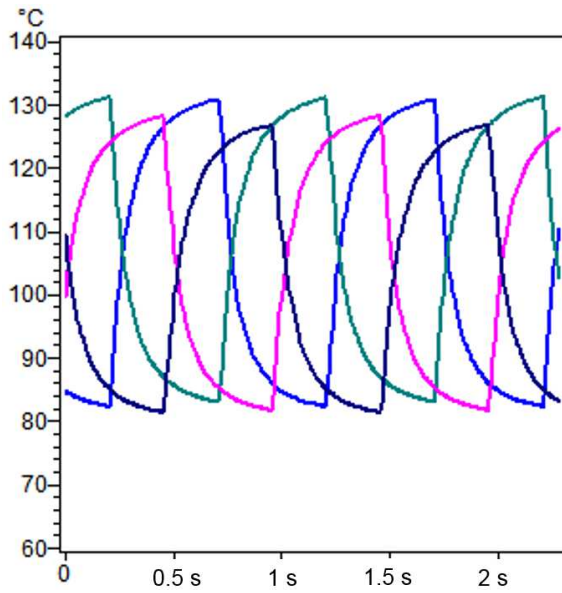


Fig. 7: Junction temperature profile for the first tests

After three weeks of tests, the first ageing results have been obtained. They are summarized in **Fig. 8**. M is related to the sample reference, N to the die location on the sample. A significant variation of connection resistances can be observed after one to two millions of cycles.

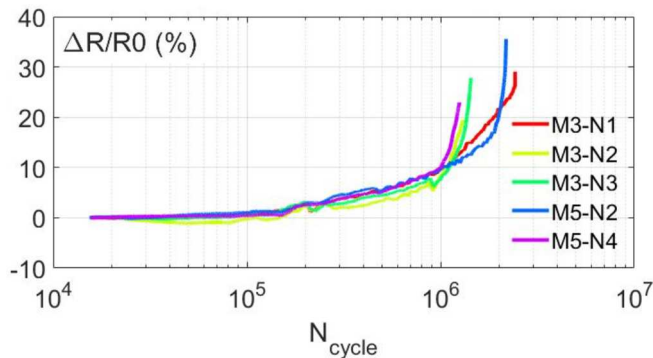


Fig. 8: Relative variations of bond wire resistance

The Table 1 presents the lifetime of the different bond wires defined for a 30% resistance variation.

Die	M3-N1	M3-N2	M3-N3	M5-N2	M5-N4
Life Time (kcycles)	2424	1311	1433	2177	1251

Table 1: Lifetime for 30% resistance variation

First, it must be recalled that bond foot degradation have been observed in previous tests after 500 kcycles to 700 kcycles, for similar power cycling parameters.

In the present case, the apparent lifetime is significantly higher.

Actually, after analysis, these results cannot be associated to a degradation of bond feet.

A MEB imaging (**Fig. 9**) reveals a degradation of metallization that could explain the increase of contact resistance. Indeed, the measurement current flows through this metallization between the main bond wire and the measurement bond wire. In addition, no degradation of the bond wires can be observed on the MEB images (**Fig. 10**).

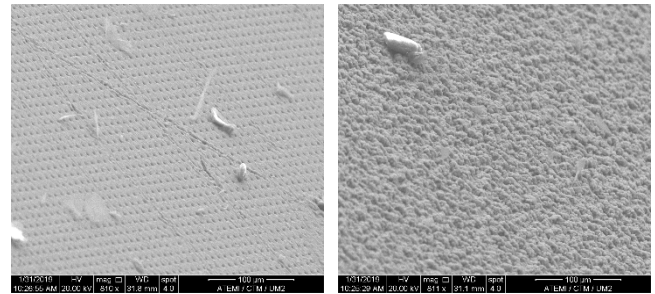


Fig. 9: The metallization before and after aging

The degradation of the emitter metallization is a well-known phenomenon but that appears classically in hardest power cycling conditions [4]. Therefore, if these first tests are not conclusive in comparison with previous results obtained on power modules, they are interesting and raise issues that need to be analyzed to eventually modify the next samples.

4.2 Ultrasonic welding quality

The first assumption that can be made concerns the ultrasonic welding process. In the present case, this operation is realized by mean of a small wire bonder dedicated to prototype realizations. The machine settings are probably different from those used in an industrial production line. If the bond wire connections are stronger than in industrial modules, the first ageing mode occurring could be the metallization degradation.

The Fig. 10 shows MEB images of the bond foot in a standard power module and in the specific sample. These views indicate clearly that the welding processes are different. The parameters used in manufacturing lines (strength and power) are normalized to guarantee the process repeatability as the respect of die characteristics. In the case of specific sample, the weld area is significantly higher, the wire being itself accompanied by strong plastic deformation zones.

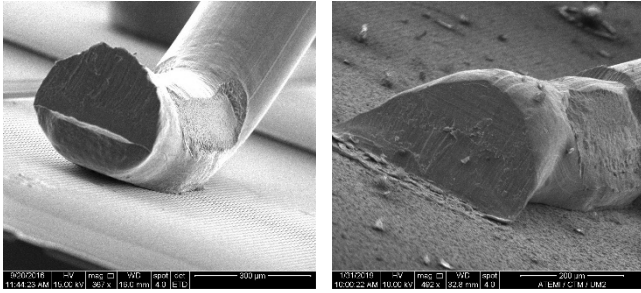


Fig. 10: bond foot – left, standard module –right, specific sample

Therefore, in the next series of samples, the bond wires will be welded with parameters as close as possible to the industrial parameters.

4.3 Bond foot location

The second assumption to explain the lack of bond wire degradations is the particular geometry and location of the bond wires on the dies in the present sample. In power modules, each die is connected by a significant number of bond wires, each of them being welded in two or three points [7]. Therefore, the bending radius between two bond feet is low and the feet can be close to the die edge, zone where the deformation due to the power cycling is maximal. In the present sample, the bond wire is welded one time on the die center and the bend radius to reach the external connection pad is high.

In order to evaluate the possible influence of the bond foot location, Finite Element simulations have been performed. Their aim is not to precisely analyze the thermo-mechanical behavior of the assembly but to collect comparative data on mechanical strains generated in the different cases. In that way, the effective plastic stresses remains a good indicator.

All the simulations are made with the same temperature profile on the die. To reduce computation times, simulations are limited to the die area. From a mechanical point of view, the behavior of the die and of the solder remains purely elastic, while a thermo-dependent elasto-plastic model has been introduced to characterize the mechanical behaviour of the bond wire.

The **Fig. 11** shows the simulated geometries. The three geometries are simulated with the same thermal and mechanical conditions. The geometry (1) represents the bond wire of a generic module with two connection points.

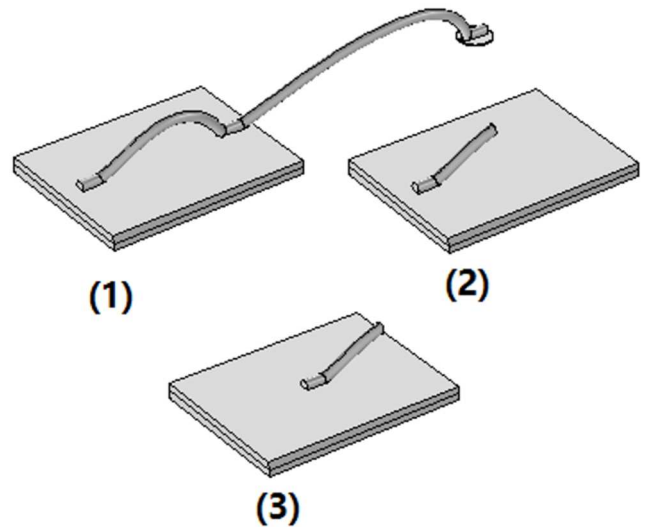


Fig. 11: Simulated geometries

The geometry (2) represents a bond foot placed near the die edge, the wire being cutted to cancel influence of the wire shape. The geometry (3) is the same as the (2) but with a bond foot placed on the die center, in accordance with the present samples.

The simulation thermal profile is identical to the experimental profile adjusted in the test. The solder is locked in such a way that expansion is possible in the three dimensions and that solid-rigid movements are not allowed.

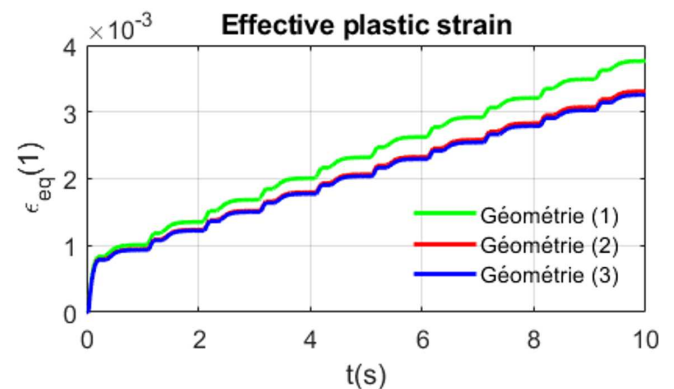


Fig. 12: Effective plastic strain for the three geometries

The **Fig. 12** shows the evolution of the average plastic strain measured on the die-foot interface, in the three cases after ten thermal cycles. No difference can be observed between geometry (2) and (3), therefore the bond foot location seems to have no effect.

Conversely, the influence of the bend radius seems to be significant. In geometry (1) it can be supposed that the low radius limits the absorption of the force variations on the bond wire, what leads to an increase of the accumulated strains on the bond foot.

Nevertheless, considering the problem complexity and the parameter variability, these simulation results cannot constitute a reliable evaluation of the ageing trends. Therefore, it is planned to test the different geometries in the next series of samples, in addition with the adjustment of wedging parameters, as mentioned in the previous section.

5 Conclusion

The use of specific samples integrated in a dedicated test bench to bring about bond wire ageing presents many advantages. The sample fabrication is straightforward and different configurations of wire bond implementation can be easily tested. Conversely to the power module, one bond wire can be stressed alone with controlled parameters and the monitoring can be more elaborated. In addition, the power consumption during the test can be drastically reduced.

In the present paper, the feasibility of the concept has been demonstrated. Nevertheless, an issue remains that concerns the test representativeness. For now, the ageing results on the first samples and on standard modules are different. Some assumptions have been formulated to explain the disparity. A new series of samples is going to be built in order to test different configurations of bond wire implementation with the hope to identify the cause of this disparity.

In addition, an automatic measurement process will be implemented in the supervision system to facilitate the tests of this new series.

6 References

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