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New metallization scheme for interdigitated back contact silicon heterojunction solar cells

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Abstract

This study reports on a new contact scheme for Silicon Heterojunction (Si-HJ) solar cells having Interdigitated Back Contacts (IBC). This new geometry with two metallization levels is used to avoid any electrical shading above the emitter and Back Surface Field (BSF) busbars. IBC Si-HJ solar cells with bi-level metallization are here compared experimentally to standard devices having a single-level contact scheme. Relative increases of 2% in Fill Factor (FF) and 8% in short circuit current density (Jsc) have been obtained with this optimized contact geometry on medium area solar cells (5x5cm²). Moreover, this technology can be used to increase the number of busbars on large area solar cells and therefore reduce series resistance effects.

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Keywords: heterojunction; Back contact; metallization

1. Introduction

To improve solar cell efficiency, photo-generation, carrier collection and transport must be maximized on the whole surface of the cell. With IBC cells, photo-generation is maximized since there is no optical shading due to contact fingers on the front of the cell. However, all regions may not collect photogenerated charge carriers in a uniform way: this phenomenon is usually called electrical shading [1]. The Figure 1 shows this variation in IQE depending on the cell region, with a lower response on BSF vs Emitter area, but also on BSF finger compared to BSF busbar. This is due to the different paths for minority carriers to reach the junction and leads to a significant loss in Jsc. Moreover, above emitter busbar series resistance losses may also have an impact on the FF due to the large lateral path that majority carriers have to travel into the bulk to reach BSF fingers [2]. Finally, it appears that busbars areas induce significant losses in Jsc and FF. Therefore, reducing those areas is mandatory to obtain high solar cell efficiency.



Fig. 1. IQE (λ =976 nm) mapping of a standard IBC Si-HJ solar cell (27cm²)

To that purpose, a "bi-level" structure was developed. This structure proposed by Sinton et al in 1990 [3] allows the removal of the active busbars placing them on a second level over the cell fingers (Figure 2). With this geometry, no "useful" area is allocated to the busbars. In addition, this geometry allows choosing the number of busbars and their location which is mostly interesting for large area solar cells where finger resistance is higher if thickness of metallization is kept constant [4, 5].

2. Study of the bi-Level metallization for IBC Si-HJ cells

2.1. Process development

In this study, bi-level structures were fabricated by screen-printing using a low temperature silver paste for metallization and polymer paste for electrical insulation. The first step consists in the metallization of the rear side with BSF and Emitter fingers (Figure 2). Then, one finger out of two is covered by an insulating paste, in order to avoid electrical contact between Emitter and BSF fingers through the deposited busbars. Finally, busbars are placed on a second level over the fingers and the localized insulating paste.



Fig. 2. 3D schemes of the metallization steps of the « bilevel » structure and cross-section of bi-level BSF Busbar

The electrical insulation properties of the polymer paste have been investigated by simple resistance measurement with an ohmmeter between the two busbars of bi-level geometry printed on dummy wafers and by leakage current density (Jleak) measurement on MIS structures (figure 3). Different thicknesses of insulating paste have been tested varying the number of prints (1 to 3). According to previous studies it is necessary to reach a Jleak value below 1×10^{-6} A/cm2 to avoid shunting effects [6, 7]. This is already obtained in our case with a single print even though the Jleak value decreases with the number of prints. Although the measurements on MIS structures show very low values, the measured resistance between the busbars of bi-level geometry is very low if only one print is deposited. Indeed, on bi-level geometry the polymer layer is printed directly on the metal fingers which can locally decrease the thickness of the layer and create a short circuit. For the MIS structure the paste is deposited onto a silicon substrate and is therefore more homogeneous and insulating.



Fig. 3. Jleak measurement (left) and resistance between 2 busbars (right) according to number of insulating paste prints

To conclude, it appears that resistance measurement on bi-level geometry gives a better description of the insulation characteristic of the polymer paste than MIS structures.

2.2. Influence of the bi-level structure

In order to compare standard devices and IBC Si-HJ with improved metallization, bi-level geometry was applied on standard devices of 27cm². Then, a cutting step has been done to remove the single-level busbars and keep bi-level busbar (Figure 4). J-V measurement at 1 sun as well as SunsVoc measurement have been done before and after each step to evaluate the performance enhancement of the cell.



Fig. 4. Schematic of a bi-level cell before (27 cm²) and after (23.7 cm²) removal of the single-level busbars

Cutting at first the single-level BSF busbar on several cells, a gain on Jsc is observed (Figure 5). Indeed, removing the low current collection area (figure 1), average current density is globally increased in the cell. Finally, cutting the single-level emitter busbar, Jsc is reduced by 0.5mA/cm² since emitter fraction is lower, the average current density decreases in the cell [1].



Fig. 5. Jsc for standard IBC cells, bi-level cells without single-level BSF busbar and bi-level cells without single-level busbars.

Finally, average results on ten cells (Figure 6) show a global relative increase of 7% on Jsc and 2% on FF with the bi-level metallization geometry compared to standard IBC Si-HJ cells which leads to a relative gain of 8% in efficiency even though open-circuit voltage (V_{OC}) decreases (-5mV). The decrease of the difference between series-resistance-free FF (PFF, obtained with SunsVoc measurement) and series-resistance-affected FF when cells have bi-level geometry shows that series resistance has been reduced with the new geometry while shunt resistance is stable, since PFF is stable. A part of series resistance decrease could be also attributed to the reduction of the cell size when bi-level metallization is used. It is important to specify that each busbar area was representing 6% of the cell surface in the fabricated standard IBC cells. Besides, the different relative gains obtained in this experiment depend strongly from the busbar area fraction. Indeed, with reduced single-level busbar area and large area solar cells, relative gains would have been smaller placing only two bi-level busbars on the edge of the cell.



Fig. 6. IV measurement parameters of standard IBC cells and cells with bi-level geometry.

3. 150 cm² IBC cells

The bi-level metallization has been adapted to 125PS substrates for the fabrication of large area IBC Si-HJ cells (Figure 7). Our measurement chuck for those devices was designed to measure IBC cells with "standard" (single level) metallization, with the busbars at the edge of the substrate. For these first cells the bilevel process was used, however with only 2 busbars located at the edges because of the measurement chuck design. With this geometry the finger metallization has to be highly conductive to avoid RSeries. Even though thick Ag fingers were printed on these first cells, a low FF value of 68% is obtained (PFF=80.5%) indicating RSeries losses in the metallizations. For this batch a poor passivation level above the BSF fingers limits both VOC and JSC values (657 mV and 27 mA/cm2). An efficiency of 12.2 % is obtained for these first large area cells, mainly limited by the resistive losses in the metal fingers and the recombinations over BSF regions.



Fig. 7. Image of a 150 cm² IBC cell having bi-level metallizations.

4. Conclusion

To conclude, average of 18.1% efficiency has been reached on 23.7cm² IBC Si-HJ solar cells with this new metallization process and 8% efficiency increase has been reached compared to standard metallization cells. Moreover, this new scheme may help to get a low resistivity on large area solar cells since charge carrier collection and metallization geometry are completely decoupled. In order to do this, a bi-level metallization with more than 2 busbars is necessary. The development of specific chucks for the measurement of such cells is mandatory, as well as interconnection processes for the modules fabrication.

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