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Ruben van Staden, Kyle Jackman, Coenrad Fourie, Pascal Febvre. Influence of the Superconducting Ground Plane on the Performance of RSFQ Cells. *IEEE Transactions on Applied Superconductivity*, 2017, 27 (4), pp.1300704. 10.1109/TASC.2017.2654345 . hal-02017249

**HAL Id: hal-02017249**

**<https://hal.science/hal-02017249v1>**

Submitted on 17 Jan 2025

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# Influence of the superconducting ground plane on the performance of RSFQ cells

Ruben van Staden, Kyle Jackman, *Member, IEEE*, Coenrad J. Fourie, *Member, IEEE*, and Pascal Febvre, *Member, IEEE*

**Abstract**—Single-Flux-Quantum (SFQ) digital circuits are mostly based on cells which rely on reliable boundary processes that make use of a superconducting ground plane as a reference for the active elements and the microstrip line interconnects. The quantum of magnetic flux  $h/2e$ , associated to the binary information, corresponds to a magnetic field energy density that needs to be localized in space to limit interactions between adjacent cells. In other words, mutual inductances can harm the proper behaviour of circuits unless they are taken carefully into account during the design phase. We studied extensively the Josephson Transmission Line (JTL) cell with different geometrical configurations of the ground plane and bias pads. We found with the use of InductEx that the return current sometimes follows paths that are far from what intuition tells, which can lead to non-optimized designs. In this paper we emphasize the limitations due to the presence of external or internal magnetic fields. Then we compare obtained performances with the ones with optimized geometries for which the presence of the magnetic field is taken into account from the design phase.

**Index Terms**—magnetic fields, digital circuits, flux trapping, moats, ground plane, return current

## I. INTRODUCTION

Developing a reliable tool chain to solve ground return current problems in SFQ circuits plays an important role for further large scale circuit integration. Unwanted magnetic fields originate from either the return current in the ground plane or an external field, such as the Earth magnetic field. In [1] the effect of the return current at different ground contact points was analysed. We analyse the effect that the magnetic field induced by the return current in the ground plane has on the circuit elements. This is done by representing the magnetic field as an inductance that couples to the circuit inductances.

Modeling the effect of return current has little significance in the design of individual cells, but does however become significant as the bias current increases to around the milliamper range [2], [3]. This normally happens when a couple of hundred thousand cells are connected to form a complete integrated circuit. We therefore investigate the effect a change in return current has on the circuit parameters when the ground contacts are placed at different locations around the chip. Since the JTL is a very stable circuit, we increased

the return current exponentially to observe the effect the return current has on the circuit margins.

The return current in the ground plane can be modelled using linear equations to calculate the mutual coupling the ground plane has with the circuit elements. A new implementation on analysing external magnetic fields was implemented into Fast Fast Henry (FFH) [4], which will be used in this paper. However, in [5] a method was used to analyse the effect the external magnetic field has on the circuit parameters. In this paper the D-Flip Flop (DFF) was analysed and results are given for cases where no shield, a grid shield and a completed shield was used. This method requires a coil to be implemented around the circuit through simulation. In this paper we show that the circuit margins change significantly with a change in the ground contact location, and we derive a few general rules to improve the design with respect to the ground plane topology.

## II. GROUND PLANE DRAWBACKS

The presence of the ground plane is a natural solution to limit the spread of magnetic flux lines through the shielding induced by the Meissner-Ochsenfeld effect. However, the presence of the ground plane brings the following drawbacks: magnetic vortices can be trapped in presence of a too high magnetic field energy density; the operation of the circuits can lead to a movement of vortices, causing magnetic noise and possible malfunctions of circuits in some cases. For dc bias lines the return current paths are not properly defined and the associated magnetic field can unexpectedly shift the point of operation of some cells and lead to a reduction of bias margins or even malfunctions as well. Consequently the specific position of the dc bias pads on the superconducting chips can lead to different operation margins of the digital circuits [1]. The use of moats in the ground plane and some on-chip shielding techniques have been studied already and are effective to improve the operations of the most complex circuits [1], [6]. This is done at the price of a higher complexity and of design rules based on experience rather than on quantitative established facts.

## III. GROUND CONTACT POSITIONING EFFECT

Rapid-Single-Flux-Quantum (RSFQ) cells typically have a superconducting ground plane that is general to all cells in the circuit. In traditional RSFQ circuits, all injected bias currents must leave through the ground plane [7]. The return current

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through the ground plane is not limited to a specific path in the ground plane and can spread out depending on the location of the ground contact. The JTL is used as a reference cell: see Fig. 1.

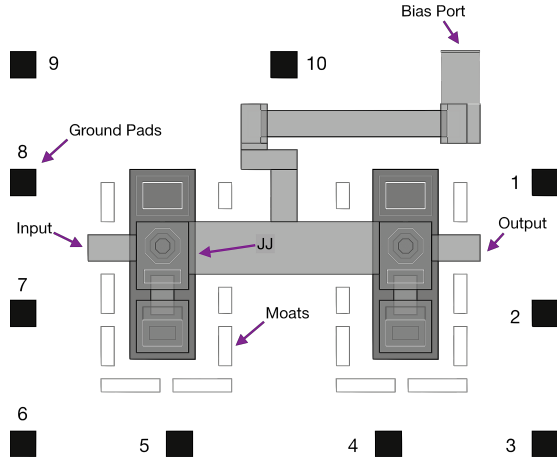


Fig. 1: Institute of Photonic Technology (IPHT)

JTL layout [8] with the ground contact positions shown and numbered.

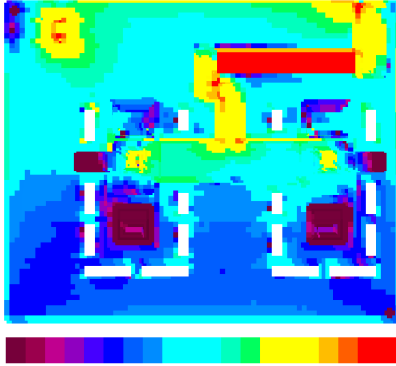


Fig. 2: Current distribution in JTL for the bias port excited and ground contact at position 9, as shown in Fig. 1. The color scale is relative to the maximum current value, with a 6dB drop per color tick.

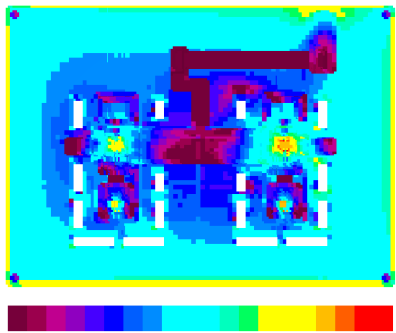


Fig. 3: Current distribution in JTL for an uniform external magnetic field applied perpendicular to the ground plane in the  $z$ -direction. The bias port is excited with the ground contact placed directly below the bias port.

The return current in the ground plane follows the path directly under the circuit back to the bias port and then spreads

to the ground contact [9]. The current in the ground plane tends to spread out to the sides of the plane, as shown in Fig. 2 and Fig. 3. The coupling factor is largest when the current direction from the bias port to the ground contact is parallel with the current flow in the inductor and their magnetic field couple (see contact 9 in Table I). The coupling is insignificant when the ground contact pad is almost directly below the bias port or close by. This validates our previous assumption of zero mutual coupling when the ground contact is directly below the bias port.

#### IV. ALGORITHM

We define the *magnetic inductance* as an extra inductance loop added to the system, see Fig. 4, to schematically analyse the effect that the coupling of the magnetic field, due to the return current, has on the circuit elements. This is possible since we can represent a magnetic field using an inductance with a current source. We can then change the current,  $I_G$ , to analyze the effects that the return current has on the circuit margins, while still keeping the bias current of the JTL at its optimal value. The modeling of the circuit is done by taking multiple superconducting loops and then solving the set of linear equations simultaneously. Using Kirchhoff's voltage law, linear expressions can be derived for these superconducting loops. Each bias port in the circuit is excited using a 1V source. To ensure that our newly derived equation gives the correct answers, the self inductance values using our new method was compared to that calculated with InductEx [10]. The linear system of equations for solving the self-inductance in Fig. 4, including the mutual coupling between the ground return current and the inductances,  $L_2$  and  $L_3$ , leads to a rank deficient matrix. We solve self-inductance of  $L_2$  and  $L_3$  by placing the ground contact point directly below the structure and assume the mutual coupling is negligible. Using these fixed values for  $L_2$  and  $L_3$ , the matrix is no longer rank deficient and the mutual coupling with the ground plane can be calculated for the various ground contact pads shown in Fig. 1. The linear system of equations that are derived from the JTL circuit are:

$$\begin{aligned} (L_2 I_2 + M_{g2} I_1) - (L_3 I_3 + M_{g3} I_1) &= 0 \\ (L_{gvb} I_1 + M_{g2} I_2) - (L_2 I_2 + M_{g2} I_1) + \frac{V_b}{j\omega} &= 0 \\ (L_{gvb} I_1 + M_{g3} I_3) - (L_3 I_3 + M_{g3} I_1) + \frac{V_b}{j\omega} &= 0 \end{aligned} \quad (1)$$

Where  $V_b$  is the bias voltage and  $M_{g2}$ ,  $M_{g3}$  are defined as the mutual inductances between the ground inductance  $L_{gvb}$  and  $L_2$ ,  $L_3$ , respectively. The values for  $I_1$ ,  $I_2$  and  $I_3$  are defined as the current through  $L_{gvb}$ ,  $L_2$  and  $L_3$  for each ground contact as calculated using InductEx. Since InductEx cannot handle inductances in series, we have to combine the ground inductance with the bias line inductance, therefore  $L_{gvb} = L_g + L_{vb}$ . To represent this as a  $Ax = b$  matrix, we simplify equation (1) to

$$\begin{aligned} M_{g2} I_1 - M_{g3} I_1 &= L_3 I_3 - L_2 I_2 \\ M_{g2} I_2 - M_{g2} I_1 &= L_2 I_2 - L_{gvb} I_1 - \frac{V_b}{j\omega} \\ M_{g3} I_3 - M_{g3} I_1 &= L_3 I_3 - L_{gvb} I_1 - \frac{V_b}{j\omega} \end{aligned} \quad (2)$$

which can be written in matrix form as

$$\begin{bmatrix} I_1 & -I_1 & 0 \\ I_2 - I_1 & 0 & I_1 \\ 0 & I_1 - I_3 & -I_1 \end{bmatrix} \begin{bmatrix} M_{g2} \\ M_{g3} \\ L_{gvb} \end{bmatrix} = \begin{bmatrix} L_3 I_3 - L_2 I_2 \\ L_2 I_2 - \frac{V_b}{j\omega} \\ -L_3 I_3 + \frac{V_b}{j\omega} \end{bmatrix} \quad (3)$$

These current values change as the ground contact position changes.

## V. EXTERNAL MAGNETIC FIELD EFFECT

To analyse the effect of the external magnetic field coupling has on  $L_2$  and  $L_3$ , we excite the circuit with a constant magnetic field in the  $x$ -,  $y$ - and  $z$ -direction. From our analysis the field in the  $y$ -direction has the strongest coupling with inductors  $L_2$  and  $L_3$ . Using the excited current in each branch we model the coupling of  $L_2$  and  $L_3$  with the field as an inductor  $L_z$ , shown in Fig. 4, connected directly to a fictitious current source. The magnitude of the current represents the magnitude of the magnetic field in Tesla.

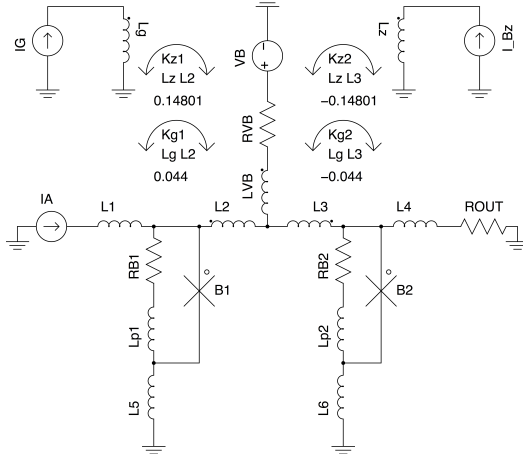


Fig. 4: JTL schematic with the added loop that represents the effect of the change in ground contact in Josephson Simulator (JSIM). Inductance  $L_g$  represents the magnetic field generated by the ground plane return current and  $L_z$  represents the inductance of the external magnetic field in the  $z$ -direction.

## VI. RESULTS

By keeping the ground contact stable at a specific position on the ground plane periphery while changing the return current, we can analyse at which ground contact positions the circuit margins are most sensitive to the change in the return current.

TABLE I: Coupling factors between ground plane and  $L_2, L_3$

Ground Contact (GC)	$L_g$ (pH)	$K_{g1}$	$K_{g2}$
1	24	0.008	-0.008
2	45	0.003	-0.003
3	59	0.001	-0.001
4	53	0.008	-0.008
5	68	0.029	-0.028
6	84	0.033	-0.033
7	71	0.040	-0.040
8	66	0.040	-0.040
9	70	0.044	-0.044
10	30	0.021	-0.021

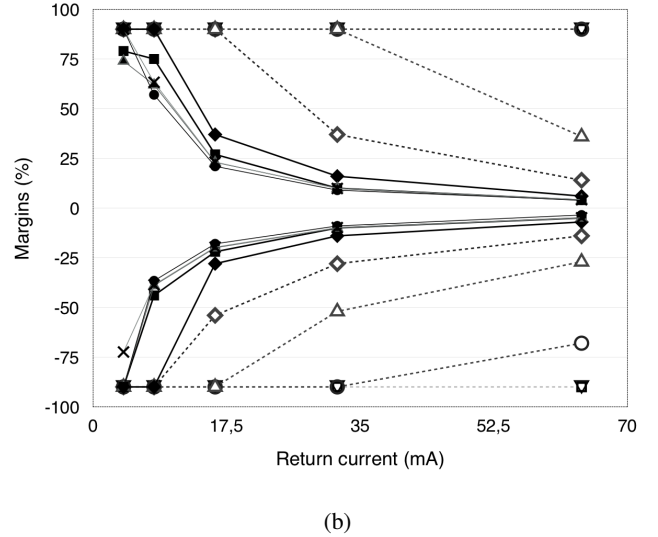
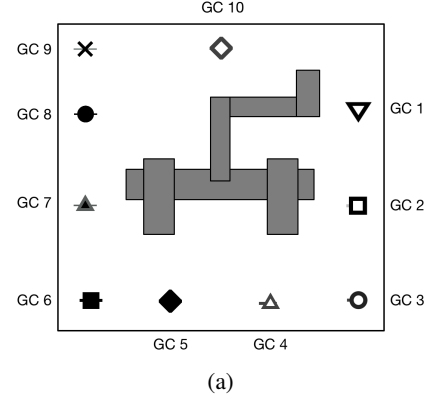


Fig. 5: Effect the ground plane has on circuit margins depending on the position of the ground contact, (a) shows the legend of (b), and (b) shows the critical margins for each ground contact.

TABLE II: Coupling factors between external magnetic field and  $L_2, L_3$

$B_{ext}$	$K_{g1}$	$K_{g2}$
$x$	0.00001	-0.00004
$y$	0.843	-0.842
$z$	0.148	-0.148

It was also observed that the closer the current path between the two points becomes to being parallel to the inductance structure, the larger the coupling factor becomes. The critical Superconducting-Quantum-Interference-Device (SQUID) loops in the circuit is that containing the bias inductance; since changing the current distribution in the ground plane drastically affects the bias inductance, which in turn changes the mutual coupling between bias inductance and the circuit inductance. In Table I the coupling factor between the ground plane inductance and  $L_2, L_3$  is given at each position of the ground contact and in Table II the coupling factor of the external magnetic field in each direction is given, where the magnetic field magnitude is represented as an inductance,  $L_z$ . We note that the difference in coupling between  $GC_1$  and  $GC_9$  is one order of magnitude. In Fig. 5b we see that for ground contacts  $GC_4 - GC_1$  the magnetic inductance does

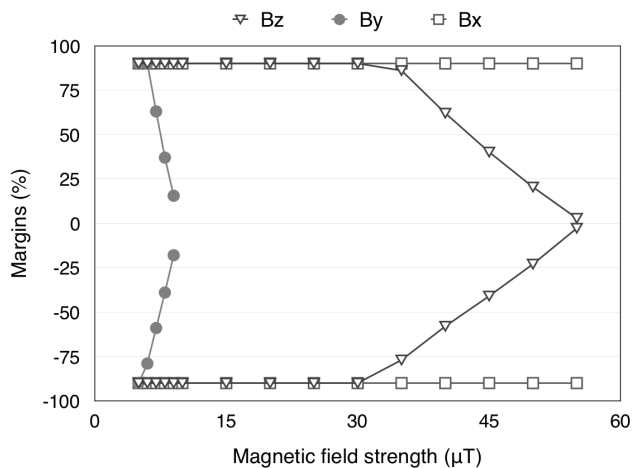


Fig. 6: Critical margins of circuit for different external magnetic field values in each directions.

not have a significant change as the return current changes, even with a return current of  $64mA$ . This is due to the fact that when a line is drawn from the bias port to the ground contact this line is almost perpendicular to the orientation of the circuit inductance. Placing a ground pad in the top-right corner of the ground plane periphery has almost no effect on the circuit margins. The reason for this is because the length of the inductance (between the bias port and the ground pad) is very small. Even though this inductance lies parallel with  $L_2, L_3$ , its magnetic field does not couple with any of the circuit inductances.

Fig. 6 shows that the  $y$ -directed magnetic field has the strongest influence on the  $x$ -directed inductances due to a higher number of flux lines that penetrate the superconducting loop of  $L_2$  and  $L_3$ . The  $x$ -directed external magnetic field has almost no influence on circuit operations, while the  $y$ -directed field causes the circuit to fail at around  $9\mu T$ , and the  $z$ -directed field causes circuit failure around  $58\mu T$ . In [11] measured results show that the magnetic fields are stronger when the ground pads are placed on the circuit corners, away from the bias port, than when a ground pad is placed close to the bias port.

## VII. CONCLUSION

Layout designers can imagine the return current in the ground plane as a straight line connected from the current bias port to the ground contact. This *magnetic inductance* will then couple with the circuit elements depending on its orientation and distance relative to the specific circuit inductance. A good rule of thumb is to try and keep this *magnetic inductance* as perpendicular and far away as possible from the dominating (largest or most sensitive) inductances in the circuit. For instance in the JTL one wants the *magnetic inductance* to be as far away and perpendicular to the critical inductance ( $L_2$  and  $L_3$ ) as possible.

We have demonstrated that the ground contact placement around the circuit periphery does indeed affect the operating margins of the circuit elements. Numerical solutions were derived to calculate the mutual coupling between the ground plane inductance and the circuit elements. We also found that we are able to represent the effect the external magnetic field has on the circuit parameters by using mutual coupling with a inductance connected to a current source. Using our methods it is possible to test the maximum magnetic field that can be applied in any direction to the circuit before failure. Future work will involve expanding our current linear equations to include multiple ground contacts and multiple ground planes.

## ACKNOWLEDGMENT

This work was supported in part by the South African National Research Foundation under Grant 93586 and by the French-South African Partenariat Hubert Curien (PHC) PROTEA No. 33944VG. The author would also like to thank J. Delpoit for his input in margins analysis.

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