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ABSTRACT

For the first time, we propose a 3D-monolithic SRAM architecture with a local back-plane for top-tier transistors enabling local back-bias assist techniques without area penalty as well as the capability to route two additional row-wise signals on individual back-planes. Experimental data are extracted from a 14nm planar Fully-Depleted-Silicon-on-Insulator (FDSOI) 0.078µm² SRAM in order to properly model 3D top-tier cells. Simulations show this technique yields a 7% bitline capacitance reduction, a 12%/16% read/write access time improvement at V_{DD}=0.8V and a reduction of minimum operating voltage V_{min} by 60mV at 6σ w.r.t. planar SRAMs.

INTRODUCTION

Static-Random-Access-Memory (SRAM) optimization under area and performance constraints suffers from conflicting best-case conditions for read/write/retention, especially for low voltage operation. While assist techniques have been commonly adopted to address this issue [1], FDSOI offers a new degree of freedom owing to the use of *static* back-biasing as demonstrated in 28-22nm node SRAMs [2,3,4]. In planar FDSOI, *dynamic* back-bias assist suffers from a large well capacitance penalty. The bias range is also limited due to partially shared wells in the SRAM matrix between neighboring rows or columns. 3D-monolithic CoolCube™ technology [5], which consists in stacking transistors on different tiers, does not suffer from these limitations (provided local back planes are dielectrically isolated from one another). This integration was recently demonstrated to efficiently enable dynamic back-bias in standard cells [6]. This work is focused on SRAM back-bias assist techniques using the unique features of 3D-monolithic top-tier 14nm FDSOI technology.

MEASUREMENT OF PLANAR 14NM FDSOI SRAMS

14nm planar CMOS devices were fabricated featuring 6nm-thin channels, 20nm minimum gate length, SiGeB/SiP in-situ doped source/drain, 90nm Contacted Poly Pitch, 64nm Metal Pitch and 0.078µm² SRAM minimum area [7]. High density (HD, $0.078\mu m^2$) and high current (HC, $0.098\mu m^2$) bitcell device dimensions are summarized in Fig.1. All the HC/HD transistors, *i.e.* the Pull-Up (PU) pMOS as well as the Pass-Gate (PG) and Pull-Down (PD) nMOS are built on silicon channel, with a single metal gate and single p-doped well (Figs 1-2). Excellent experimental static performance is obtained (nominal conditions are V_{DD}=0.8V, V_{well}=0) (Figs 3-5).

PLANAR SRAM CELL SENSITIVITY TO BACK BIAS

The sensitivity of SRAM *vs.* back bias (V_{well}) was also characterized experimentally. Since the well is shared between all devices in the analyzed bitcell, V_{well}<0 strengthens the Pull-Up PMOS (PU) and weakens the Pass-Gate (PG) and Pull-Down (PD) NMOS transistors, helping the PU to maintain BLTI=1 and thus BLFI=0 during the read operation (see SNM in Fig.6). Conversely, using V_{well}>0 improves the PG/PU strength ratio (and in turn the WNM) and increases the write current (governed by PG drive). As a consequence, back biasing can be used to assist both write (V_{well}>0) and read operation (V_{well}<0). In regular FDSOI, this cannot be practically achieved because a single well is common to the whole array (no column selection). Performing dynamic back-bias would, therefore, require switching a huge capacitance between read and write operation, leading to unacceptable increase of access energy and delay. 3D-monolithic integration with local back planes offers thus much greater opportunities for assist techniques than planar FDSOI.

PERFORMANCE ASSESSMENT OF 3D TOP-TIER SRAMS

A FDSOI SPICE model and a design kit were built using electrical parameters characteristics of the CoolCube™ low-temperature process [5]. The 14nm 3D-monolithic design environment includes four intermediate metal lines iML and a back plane, which follow the same design rules as a back-end metal layer (Figs 7-8).

A detailed study of the influence of independent back-bias for PU/PG/PD shows that the threshold voltage of the PU must be lowered (V_{Bpu}<0) for all figures of merit (FoM), which cannot easily be achieved using a gate-first FDSOI process with Si channel (Fig.9). This can be performed in 3D by using a PU-dedicated back plane with a constant bias (V_{Bpu}=-0.8V) applied in all operation modes. Additionally, PD (or PG) threshold voltage can be dynamically modulated according to SRAM operation to improve margins and currents. Three promising assist modes (with different V_{Bpg},V_{Bpu},V_{Bpd}) are selected for the write (A1) and read stability (A2) as well as for the read time (A3) assist. Using this versatile assist yields +23% WNM, +28% I_{write} with A1, +4% SNM with A2 and +28% I_{read} with A3 at V_{DD}=0.8V and V_{well}= ± V_{DD}/GND *vs.* the reference configuration with a single back-plane biased at 0V (Fig.9). Furthermore the gains are more pronounced at low supply voltage V_{DD} (Fig.10), leading to a 60mV V_{min} reduction with A2 (Fig.11). The corresponding layout (common for A1-A2-A3) has been designed, connecting two groups of local (to-the-bitcell) back planes for PD and PG through internal vias (Fig.8) without area penalty. Actually back plane lines parallel to BLs distribute a static PU bias. Moreover the two dynamic signals are routed by iML3 in the WL direction within the SRAM height (whereas wells are typically in the BL direction in planar technologies). Thus, back biasing allows boosting a selected row in top-tier without disturbing other rows.

In order to evaluate the capacitance gain provided by a local back-plane compared with a continuous one (or a single well in planar), back-end parasitics have been extracted using TCAD and included in the SPICE netlist. A 7% BL capacitance reduction and a 12/16% read/write time improvement is achieved (w.r.t. reference cell at V_{DD}=0.8V) (Figs 12-13). The demonstrated assist technique can be combined with WL underdrive, negative BL or other standard assist techniques [8] for further performance and stability improvement (Fig.14).

CONCLUSION

The presence of local back planes in 3D-monolithic technology provides an extra knob to optimize the static and dynamic bitcell performance/area of top-tier FDSOI SRAMs. This specific feature is related to the integration of row-based, local back-planes addressed by internal vias and intermediate metal lines. The optimization of back bias assist techniques in such 3D architecture allows us to reduce the read /write access time by 12/16% and V_{min} by 60mV in a 14nm HD SRAM.

Cell	Surface (µm²)	L_{ALL} (nm)	W_{PU} Pull-Up (nm)	W_{PD} Pull-Down (nm)	W_{PG} Pass Gate (nm)
High Density (HD)	0.078	30	45	68	66
High Current (HC)	0.098	30	52	114	112

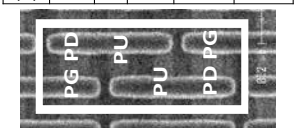


Fig.1: 14nm FDSOI 6T-SRAM. **Top:** key dimensions. **Bottom**: 14nm planar HD SRAM SEM observed at the gate level.

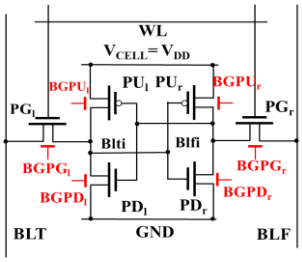


Fig.2: SRAM schematic. The additionnal terminals provided by CoolCube™ technology are highlited in red.

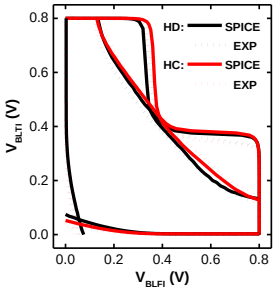


Fig.3: Exp. SNM butterfly curve and WNM at V_{DD}=0.8 V *vs.* SPICE.

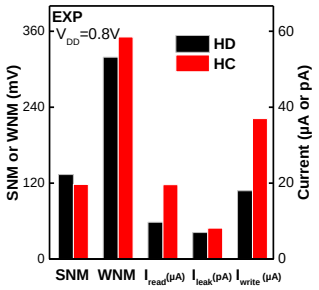


Fig.4: Exp. comparison between HD, HC cell for typical Figures-of-Merit (FoM).

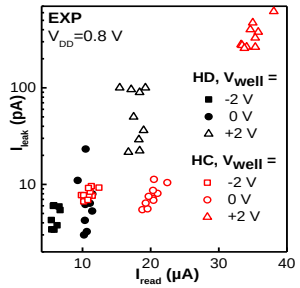


Fig.5: Exp. cell current *vs.* cell leakage for different p-well biasing (V_{well}).

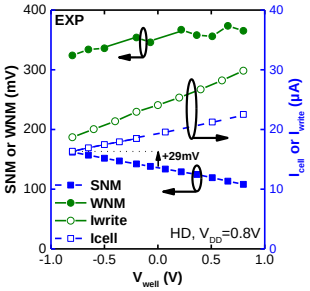


Fig.6: Exp. read and write FoM as a function of V_{well}.

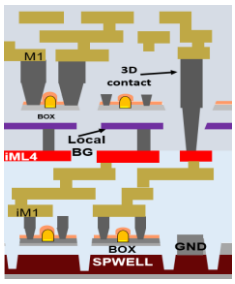


Fig.7: Schematic stack of CoolCube™ 14nm Design Kit with intermediate vias between the back plane and the upper intermediate metal line.

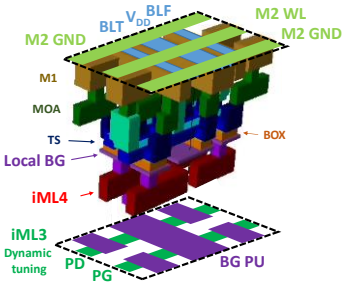
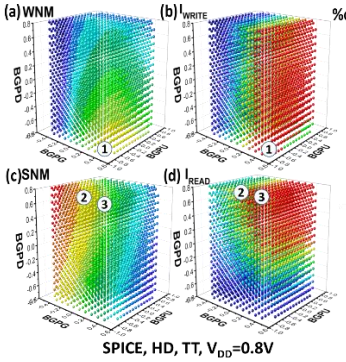
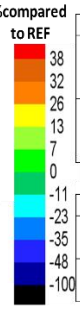


Fig.8: SRAM 3D layout view with underneath backbias connections routed in the word line direction.





	BG bias (V)	REF	A1	A2	A3
WRITE	PG	0	**0.8**	0	0.8
	PU	0	-0.8		
	PD	0	**-0.8**	-0.8	0.8
READ	PG	0	0	**0**	**0.8**
	PU	0	-0.8		
	PD	0	-0.8	**0.8**	**0.8**

	FOM	REF	A1	A2	A3
WRITE	WNM (mV)	336	**431**	338	320
	I_{WRITE} (µA)	30.6	**33**	32.7	38
READ	SNM (mV)	146	171	**164**	124
	I_{READ} (µA)	17.4	15	18.6	**22**

Fig.9: Sensibility (%) of (a) WNM, (b) I_{WRITE}, (c) SNM and (d) I_{READ} on independent back-biasing (on PD,PG,PU) (nominal configuration is at V_{BG}=GND) (SPICE). Three assist modes are highlighted: A1, A2 and A3.

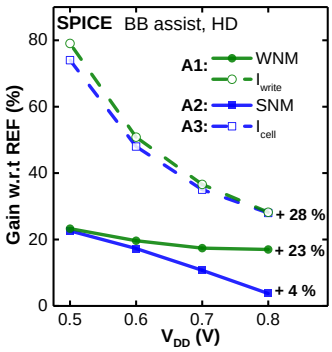


Fig.10: WNM/SNM/I_{write}/I_{read} improvement w.r.t. REF *vs.* V_{DD} (SPICE).

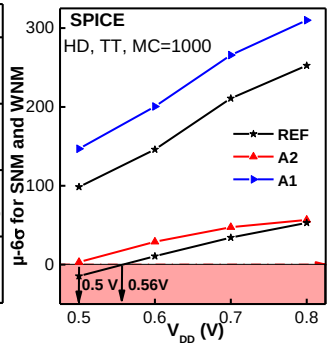


Fig.11: SNM/WNM (at µ-6σ) as a function of V_{DD}. V_{min} is lowered by 60mV with back-biasing (SPICE).

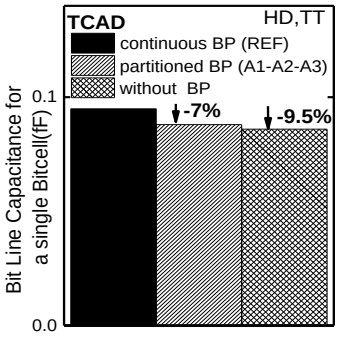


Fig.12: Bitline capacitance computation for a single bitcell with different back plane configurations (TCAD).

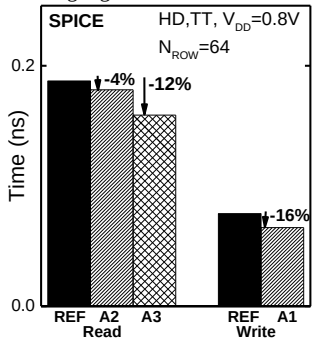


Fig.13: Read/write time (SPICE). A3 is particularly interesting to boost cell reading time.

µ-6σ (HD, WC, V_{DD}=0.8 V)	SNM (mV)	I_{READ} (µA)	WNM (mV)	I_{WRITE} (µA)
REF	45	11	235	15
A2 (V_{BPG}=0V, V_{BPU}=-0.8V, V_{BPD}=0.8 V)	61	13	-	-
WL underdrive (V_{WL}=80%*V_{DD}=0.64 V)	116	11	-	-
WL underdrive + A2	128	13	-	-
A1 (V_{BPG}=0.8V, V_{BPU}=-0.8V, V_{BPD}=-0.8 V)			298	23
Negative Bitline (V_{BL}=-0.15V)	-	-	258	36
Negative Bitline + A1	-	-	315	45

Fig.14: Gain summary of different read/write assists.

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