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# Emergence of SiC Thyristors Featuring Amplifying Gate Design

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**Abstract.** This paper will highlight ISL's research activities aimed at high-power SiC-based thyristor switching devices. With the emergence and implementation of novel gate architectures large-area devices will come within reach in the near future. In this context, we report on SiC thyristors fabricated on wafer substrates, featuring an integrated amplifying gate structure: as a result, primary device functioning was established on wafer; on-state and blocking characteristics have been verified so far up to 0.1 A and -20 V, respectively. Herewith, an innovative technology platform is emerging which allows for the development of SiC devices for operational scenarios such as high temperature, harsh environment, and ultra-high (> 10 kV) voltages.

## Introduction

Advances in silicon carbide (SiC) materials, processing, and device design have recently resulted in the implementation of SiC-based electronics for high voltage, high temperature, and high frequency applications [1]. To date, SiC is even the only viable wide-bandgap material which is considered for devices and components to be used in high power and pulsed power electronic systems. In this context, the thyristor device is the premier choice due to its bipolar conduction, low conduction losses, and high-current handling capabilities. However, in order to take full advantage of these characteristics in applications the power handling capabilities of SiC thyristors need to be further increased and optimized. This can be achieved by both implementing larger device area and parallel connection of devices. In either case, optical triggering as recently demonstrated in a joint effort of ISL and Ampère Laboratory by using SiC thyristors is an advantageous technology to eliminate a source of electromagnetic interference and to facilitate the control of high-voltage device stacks [2].

In view of the tremendous progress made in SiC crystal quality and wafer size, large-area SiC thyristors become more and more feasible. One major challenge along this route, however, is the development of advanced gate structures. For electrical as well as optical triggering, amplifying gate architecture has been state of the art in Si technology for decades [3] and thus needs to be thoroughly revamped for SiC thyristors: in this context, a new device conception was set up aimed at 1.2 kV amplifying gate thyristor (AGT) structures with mesa termination and optimized based on two-dimensional numerical simulations both using mixed-mode and finite-element methods [4].

## Device Conception and Fabrication

**Structure and Layout.** The fundamental idea behind the concept of amplifying gate turn-on or follow-up triggering is to take the power being necessary for triggering a large emitter periphery from the load circuit of a small integrated auxiliary thyristor rather than from the gate circuit [5]. All technical variants of this concept have in common that – given the auxiliary (or pilot) thyristor is

properly dimensioned – triggering proceeds in two phases: first, within the integrated auxiliary thyristor which then is followed by the main (or principal) thyristor. Once the latter is turned on it will take over the load current from the pilot thyristor and preserve it against damage by overload.

The implementation of such a concept into a SiC device configuration is quite obvious, see Fig. 1. The device configuration reported here is based on an epi-structure having the same layer sequence, namely  $n^+(\text{substrate})/p/p^-/n/p^+$ , that is commonly used for asymmetric SiC thyristors. The AGT structure comprises a central gate electrode (G) and – concentrically arranged – pilot thyristor ( $A'$ ), anode (A), and junction termination extension (JTE). Note that the anode of the pilot thyristor ( $A'$ ) and the gate contact of the main thyristor ( $G'$ ) are connected with each other and consequently overlap the  $p^+/n$ -base junction. As a result of the mesa-like p-emitter structure this overlapping contact passes a step. Due to the epitaxial structure, two characteristic features were identified as regards the AGT device: first, the contact bridging auxiliary anode and main gate require a mesa step, and second, the design criterion for realizing an amplifying gate structure must rely on geometrical constraints only, see Ref. 6. While the former was part of the technological hurdles to be cleared the latter is more of fundamental importance for the entire device layout.

In order for the AGT device conceptualized to work properly, *i.e.*, trigger the auxiliary thyristor rather than the main thyristor, the voltage drop produced by the gate current when passing through the lateral n-base resistance beneath the auxiliary anode, here, denoted as  $R_P$ , see Fig. 1, must exceed the threshold voltage and, moreover, the voltage drop across the resistance  $R_M$  underneath the main anode; in terms of  $R_P$  and  $R_M$  this is equivalent to

$$R_P > R_M, \quad (1)$$

which obeys when transferred to a circular device geometry to

$$\frac{r_{SA}}{r_{EA}} > \frac{r_{SM}}{r_{EM}}, \quad (2)$$

where  $r_{EA}$ ,  $r_{SA}$  and  $r_{EM}$ ,  $r_{SM}$  refer to the radial distances from the gate center to the edges of the auxiliary and the main anode (*cf.* Fig. 1), respectively.

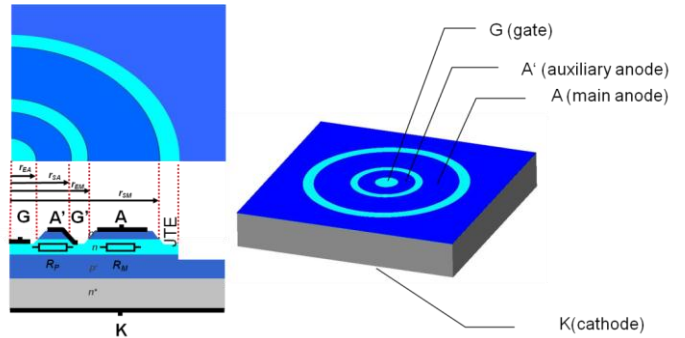


Fig. 1. Scheme of an amplifying gate thyristor (AGT) based on SiC.

The device under investigation is a SiC thyristor with a blocking capability of nominal 1.2 kV and a die size of 10 mm<sup>2</sup>. The first constraint reflects the fact that the device is aiming at fundamental investigations and thus does not require any advanced performance; the latter is a trade-off between the need for sufficiently large gate periphery and a rather small die size necessary to assure an adequate yield of equally functioning devices.

The source material of our devices comprises a 4° off-axis n-type 4H-SiC production-grade 100-mm wafer substrate from SiCrystal AG. The epi-layer structure was grown at Ascatron AB in compliance with our target specifications; prior to epi-layer growth, the wafer top side (Si face) was chemical-mechanical planarization (CMP) polished.

**Processing.** The thyristor fabrication process is based on a mask set comprising six levels; in general, prior to each of these mask steps a cleaning procedure was applied in order to remove residuals from the previous step. First, the gate/anode structure was formed using reactive ion etching (RIE); the subsequent mesa etching process ensured that the n/p junction of the two bases is cut and the etching depth is sufficiently deep to achieve a single-step JTE. For both RIE steps, a resist mask was used for reasons of simplification; moreover, it allows for inclined side walls being important for the overlapping amplifying gate contact as well as the efficiency of the etched JTE.

In the next step, the electrical contacts to the intermediately doped ( $1 \times 10^{17} \text{ cm}^{-3}$ ) n-base (gate) layer and the highly doped cathode ( $1 \times 10^{19} \text{ cm}^{-3}$ ) on the backside of the wafer were realized, each comprising a bilayer of Ti and Ni. The electrical contacts to the highly doped ( $\geq 1 \times 10^{19} \text{ cm}^{-3}$ ) p<sup>+</sup>-emitter (anode) layer were made of a Ti/Ni/Al trilayer and realized only afterwards taking into account that the relevant annealing temperature is distinctly lower than the annealing temperature for the alloyed contacts to the n-type SiC; for contact alloying, a rapid-thermal processing (RTP) reactor was used. Once the primary metallization has been finished the final mask step is used to cover gate and anode contacts with a thick trilayer made of Ti, Ni, and Au allowing for wire bonding to the outer periphery. Likewise, the backside contact was prepared for a soldered die attach. Note that for reasons of simplicity, in particular, as the focus was less on preventing surface breakdown or high leakage currents rather than giving proof of the conceptual design, deposition of a passivation layer, *e.g.*, as formed by SiO<sub>2</sub> has intentionally been omitted.

## Electrical Characterization

**Test structures.** Extensive preliminary tests were performed to adjust the annealing conditions and ensure that the final contact resistance of gate and anode metallization be sufficiently low. Hereto, SiC chips,  $10 \times 10 \text{ mm}^2$  in size, both of n and p-type as well as full wafers have been used as substrate; transfer length method (TLM) test structures served as a means of quantifying the individual contact resistance by using a manual four-head needle probe system.

For n-type, it has been demonstrated that resistivity sinks to a minimum at around 1050°C; reproducible annealing conditions thus result in a contact resistance well below  $10^{-4} \Omega \cdot \text{cm}^2$ , the best value in this context is  $3 \times 10^{-5} \Omega \cdot \text{cm}^2$ . For p-type, resistivity values scatter far less compared to the n-type samples; scattering and resistivity, however, increase with ascending temperature – quantitatively, the contact resistance remains just slightly below  $10^{-4} \Omega \cdot \text{cm}^2$ . Best values close to  $8 \times 10^{-5} \Omega \cdot \text{cm}^2$  were achieved upon annealing at 750°C.

Fig. 2 shows the mapping of the gate contact resistances as regards the final wafer processing: as a result, a high lateral uniformity has been reached over the full wafer area, quantitatively with more than 75% of the resistance distribution below the target rating envisaged, here,  $5 \times 10^{-4} \Omega \cdot \text{cm}^2$ . Solely, in a few mask fields adjacent to the wafer edge exclusion data acquisition failed either due to the lack of test structures in accordance with the underlying mask layout or due to the presence of structural or lithographical defects which impeded performing probe testing of single TLM contacts.

**Static Characteristics.** Primary thyristor characteristics have been demonstrated so far as regards forward conducting and reverse blocking behavior between gate and anode regions, see Fig. 3. The data curves were acquired via on-wafer probing from single gate thyristors which, solely for the purpose of comparison, are configured with a large single gate contact instead of an amplifying gate structure.

Proper blocking behavior has been verified, here, up to -20 V, by connecting the gate to ground potential ( $V_{\text{GA}} = 0 \text{ V}$ ,  $I_{\text{G}} = 0 \text{ A}$ ), on-state behavior by delivering a gate current of  $I_{\text{G}} = -50 \text{ mA}$ . In order to avoid thermal problems with the needle probes the on-state current was limited, here, to a maximum of 100 mA when applying a voltage sweep between anode and cathode from 0 to -6 V and vice versa. When sweeping in positive direction the gate current was switched off immediately after starting the sweep. In this way, it could be demonstrated that the thyristor keeps switched-on until the cathode current falls below the so-called holding current.

**Dynamic Characteristics.** In preparation of the acquisition of dynamic characteristics different test-beds have been developed at ISL and Ampère: At ISL the basic concept is based on a circuit comprising two Si thyristors used for emulating pilot and main thyristor in an AGT configuration. Thus, it has been demonstrated that follow-up triggering can be modeled appropriately using PSpice simulations and likewise be verified through I-V transients as taken from TIC 106 N test devices.

At Ampère a test-bed has been developed which allows for pulse characterization of individual thyristors or AGTs regardless of their forward and blocking voltages or their respective peak

current. Its main part is a load inductance which in combination with a proper charging capacitance enables the thyristor to reach the maximum peak current desired and to turn off thanks to the negative oscillations induced by the LC resonance circuit.

As a result, both test-beds will enable us to further analyze our SiC AGTs as regards their fundamental properties as well as their specific power handling capabilities.

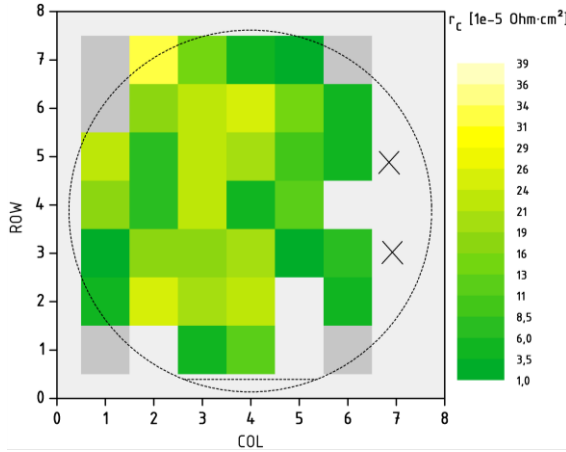


Fig. 2. Mapping of the final wafer *vis.* the distribution of gate contact resistances.

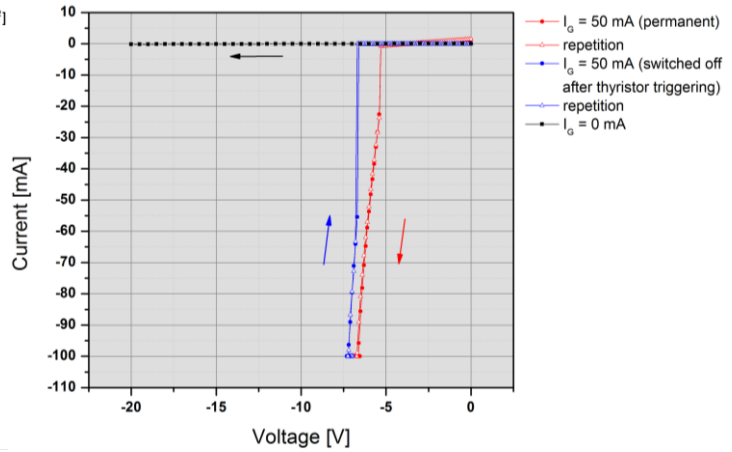


Fig. 3. Thyristor on-state characteristics (arrows indicate sweep direction).

## Summary

Here, for the first time, we report the fabrication of SiC thyristor devices featuring an integrated amplifying gate structure: Thyristor functioning has been demonstrated for the present by means of their static characteristics such as forward conducting and reverse blocking behavior between gate and anode regions. TLM measurement data reveal a gate contact resistance of a few Ohms only ( $< 5 \times 10^{-4} \Omega \cdot \text{cm}^2$ ) being negligible compared to the n-base sheet resistance underneath pilot and main thyristor. Finally, the realization of a bonding scheme in combination with establishing appropriate test-beds will allow for retrieving the AGTs' high voltage and pulsed power characteristics. Thus, an innovative technology platform becomes available which in the near future is planned with the aim to go deeper into SiC devices for operational scenarios such as high temperature, harsh environment, and ultra-high ( $> 10 \text{ kV}$ ) voltages.

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