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A Novel Passive Cost-Effective Technique to Improve Radiated Immunity on PCBs

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Jean-Luc Levant, and Mohamed Ramdani ^{id}, *Senior Member, IEEE*

Abstract—This paper proposes a novel simple cost-effective technique to improve the potential immunity of integrated circuits (ICs) to radiated electromagnetic (EM) disturbances. It is based on dielectric loading which lessens the susceptibility of ICs independently of frequency by confining the reactive fields inside the dielectric load. This has no side effects on the IC performance. To highlight the importance of the proposed technique, immunity testing was performed numerically both in near and far fields. A loaded IC (a microcontroller) was compared to an unloaded one through far-field measurements inside a transverse EM cell to indirectly assess the suitability of the proposed approach. Results show that loading the IC with non-ferromagnetic dielectric material not only effectively decreases its susceptibility to electric field, but also to magnetic field. Moreover, a significant difference of $\sim 48\%$ less failure rate was achieved for the loaded compared to the unloaded IC demonstrating the usefulness of this technique as a potential solution for radiated immunity improvement.

Index Terms—Dielectric loading, far field, integrated circuits (ICs), near field, radiated immunity, transverse electromagnetic (TEM) cell.

I. INTRODUCTION

ELECTROMAGNETIC (EM) immunity (EMI) and EM compatibility (EMC) testing are of great importance with the fast increasing functionality and complexity of integrated circuits (ICs) [1]–[3]. A higher clock frequency or any electrical transition with sharp edges (e.g., addressing or controlling data) gives rise to EMI issues [4].

In an embedded system, a microcontroller (μC) plays a major role in governing specific operations. μC s are subjected to a partial or a complete malfunction in presence of an EM disturbance [5]. Moreover, printed circuit boards (PCBs) having relatively long tracks connected to IC pins suffer more in terms of radiation, as they act as antennas driven by IC activity. These have led the EMC/EMI regulatory commissions (e.g., international electrotechnical commission IEC [6]) to define limits on EM radiation produced by ICs.

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Besides, the industrial trends in the EMC of μC s show an increasing demand for IC miniaturization technology, which leads to speed up their functionality at the cost of a higher power consumption and stronger switching currents [7]. To counteract the latter effect, voltage supply is reduced, which in return lowers the noise margin of digital circuitry and consequently IC immunity [8]. This fact fostered some interest in the wireless communications community for ways to improve immunity of ICs to radiated disturbances.

A most commonly used approach to improve the EMI field generated by today's high-speed ICs is shielding [9]. Another prevalent solution is to take benefit from flexible polymer absorbers [10], [11]. They are made of either soft metal flakes filler in polymer resin or high permeability magnetic flake particles. The latter is usually preferred as it is non-conductive and can be directly applied to circuit tracks.

Here, we propose a new simple passive approach to improve the radiated immunity on PCBs using dielectric loading. It is worth mentioning that dielectric loading has been mainly employed by antenna engineers as an effective technique to reduce antenna dimensions [12], to introduce notch frequency bands [13], and, in general, to improve antenna behavior with no side effects [14]. It has also been used to reduce interactions between antenna and human body by making the antenna less sensitive to human body proximity effects [15]. It consists in gluing small pieces of demetalized commercially available substrate with a proper permittivity around/over the IC. Simulations and measurements were conducted to confirm the adequacy of the proposed technique.

There exist several near and far field measurements techniques to evaluate the radiated EM immunity of ICs. The most commonly used near-field technique is the IEC 62132-9 scan method [16], which is a reciprocal use of IEC 61967-3 employed for immunity testing. A transverse EM (TEM) cell, which approximates a uniform and linearly polarized plane wave, is widely used for far-field EMI/EMC tests of radio frequency (RF) devices [17]. In general, measurements in far field indicate the PCB radiation with respect to its orientation and to frequency. However, they cannot determine the internal sources of emissions. Conversely, near-field techniques overcome this limitation providing a precise location of radiation sources. Here, for the sake of completeness, the suitability of the proposed approach was investigated both in near and far field zones.

The paper is organized as follows. Section II describes the materials used, the methodology employed, and the simulation

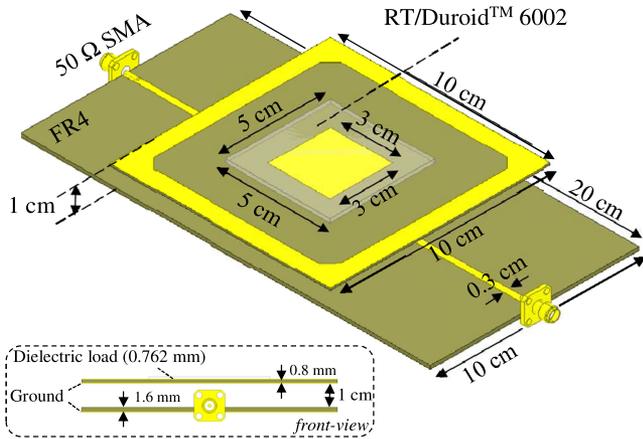


Fig. 1. Schematic geometry used in simulation.

and experimental setup configurations. Section III details the analysis of the numerical results, while Section IV addresses the experimental results of the proposed technique. Concluding contributions of this study are provided in Section V.

II. MATERIALS AND METHODS

This section deals with the research material and methodology to study the influence of dielectric loading on the radiated immunity on PCBs.

A. Simulation Setup and Method

As described in IEC 62132 [6], a simple 10 cm \times 10 cm square PCB was considered with a 3 cm \times 3 cm square metal patch in its center representing a rough approximation of an IC (see Fig. 1). The patch is printed on a low-cost FR4 epoxy substrate ($\epsilon_r = 4.4$, thickness = 0.8 mm, and $\tan \delta = 0.02$). The other side of the PCB is coated with metal serving as ground plane. The PCB is mounted 1 cm above a 50 Ω transmission line (TL) of 0.37 cm width to be in near-field conditions (see Fig. 1). The other side of the TL substrate (FR4, thickness = 1.6 mm) is a metallic ground plane. All the metallic parts in the numerical model are considered to be copper.

A 5 cm \times 5 cm solid piece of demetalized low-loss commercial substrate (RT/Duroid 6002) with a permittivity of $\epsilon_r = 2.94$, thickness of 0.762 mm, and $\tan \delta = 0.001$ was used as the dielectric load to fully cover the square patch. This small low-loss load confines the reactive (non-radiating) fields, which would result in lower electric field intensity while maintaining magnetic field, with no EM power dissipation. To evaluate the importance of the proposed dielectric loading technique, simulations were performed using Ansys HFSS full-wave solver both in near and far EM field zones. In EMC, the limits for near and far field zones are usually fixed at $\frac{\lambda}{2\pi}$ and $\frac{2D^2}{\lambda}$ from the source, respectively, where λ and D are the wavelength and the largest radiator dimension, respectively.

B. Measurement Setup and Method

In order to perform experiments, an indirect measurement was considered due to the impossibility of measuring the EM fields directly at the PCB level under the dielectric pad. As modern μ Cs are generally equipped with embedded phase lock loops (PLLs) to accurately protect the system clock from jitter and instabilities, they are very sensitive to EM disturbances [5], [19], [20]; in [5] and [20], the μ C malfunction due to injecting magnetic field on PLL power supply pins has been reported. Here, a 32-bit μ C (ATMEL SAM3S4B) [21] initially designed for a previous research project was used. It was loaded by a piece of dielectric to check whether it improves the immunity of the μ C's clock PLL to the EM interferences. A TEM cell as the far-field free space condition emulator was also employed for radiated immunity testing. We used a standard TEM cell (Model: FCC-TEM-JM2, dc up to 1.6 GHz) for the purpose of this study [22].

The thermal conductivity of RT/Duroid 6002 is $0.6 \frac{W}{m \cdot K}$ [18]. For the considered load dimension of 50 mm \times 50 mm \times 0.762 mm layer, the thermal resistance is $0.5 \frac{K}{W}$, which would lead to a low temperature difference between both sides of the load even for large size ICs (e.g., dissipating about 15 W, such as Intel CoreTM i3-7020U laptop processors). In case of small ICs, such as SAM3S4B, with 10 mm \times 10 mm package, the thermal resistance would be $12.5 \frac{K}{W}$ ($25 \times 0.5 \frac{K}{W}$), considering the worst case scenario where no heat would be dissipated in the horizontal plane. With the SAM3S4B dissipating about 132 mW (40 mA \times 3.3 V), the difference between the upper and lower sides remains very low ($0.132 \times 12.5 = 1.65^\circ \text{C}$).

III. NUMERICAL RESULTS AND DISCUSSION

This section presents the impact of dielectric loading on the PCB behavior in near and far field scenarios. A comparison is made between the loaded and unloaded ICs (an equivalent patch) considering the distribution of wave impedance, i.e., the ratio of the norms electric to magnetic field ($\|E\|/\|H\|$), as the criterion to provide an index of the relative strength between the electric and magnetic fields. The magnitude of the electric field decreases under the load due to the dielectric properties of the material. As far as the magnetic field is concerned, coupling with the pins of an IC depends on the orientation of the tangential component: The more parallel to the pins, the lesser coupling and consequently lower is the disturbance injected into low-impedance pins (such as power supply pins).

In a TEM cell, magnetic field lines are supposed to be all in the same direction. In the case presented in the paper, it must be noted that the purpose of loading is not to ensure the most homogeneous magnetic field below the load surface, but to decrease the IC susceptibility. Therefore, when the IC is replaced by an equivalent patch, it is necessary to check out the following, when the patch is loaded:

- 1) If the direction of the tangential magnetic field around the patch at a given frequency remains unchanged, the magnitude of that field decreases (or, at least, does not increase).

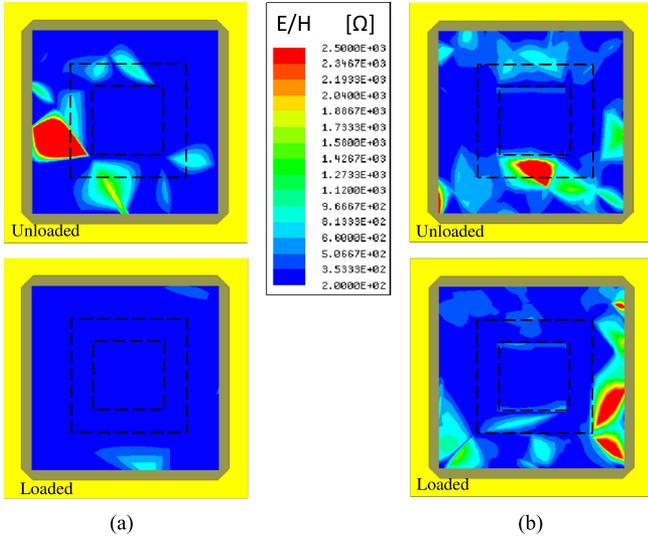


Fig. 2. $\|E\|/\|H\|$ ratio for unloaded and loaded ($\epsilon_r = 2.94$) PCBs for 1-W input power at (a) 1 GHz and (b) 1.85 GHz.

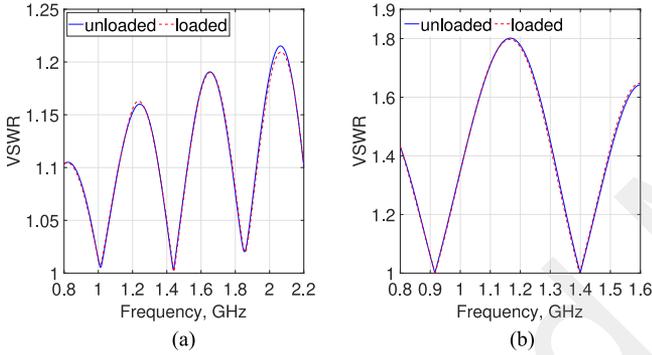


Fig. 3. Influence of dielectric loading on VSWR. (a) TL. (b) TEM cell.

- 2) If the direction of that magnetic field changes, the latter becomes more perpendicular to the patch sides (i.e., parallel to IC pins).

If those conditions are met, it is possible to claim that the immunity of the IC to magnetic field would either decrease or remain unchanged with the dielectric load.

A. Near Field

Fig. 1 shows the simulation setup; one port is excited, while the other one is terminated with a $50\ \Omega$ load. The IEC standard for the voltage standing wave ratio (VSWR) with $50\ \Omega$ termination has to be lower than 1.25, which is the case here over a wide range of frequencies [see Fig. 3(a)]. To evaluate the importance of the dielectric loading, a comparison was made with the unloaded PCB.

Fig. 2 shows the wave impedance distribution on the PCB surface with and without the dielectric loads at two gigahertz-resonance frequencies, i.e., 1 and 1.85 GHz [see Fig. 3(a)]. Note that loading neither detunes the frequency nor changes the level and, therefore, the variation in impedance distribution is not a result of a frequency change due to the load. In Fig. 2, the colors representing the $\|E\|/\|H\|$ ratio distribution in linear

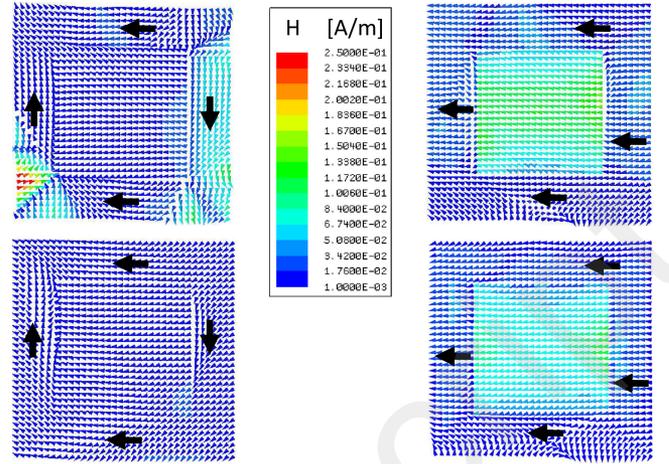


Fig. 4. Simulated vector magnetic field distribution around the unloaded (top) and loaded (bottom) patch under the load at (a) 1 GHz and (b) 1.85 GHz. Black arrows indicate the privileged orientation.

scale go from dark blue (low impedance) to green, yellow, and red (high impedance). As observed in Fig. 2(b), we can clearly see that the highest impedance at the bottom side of the IC is $\sim 800\ \Omega$ for the loaded case, whereas for the unloaded case, it ranges over relatively higher values from 1500 to 2500 Ω . This is a result of reactive field confinement in the dielectric loads. The effectiveness of the loading technique was checked through simulations and found to remain unchanged for a similar scenario, but with the PCB flipped down to have the patch facing the TL.

Fig. 4 plots the simulated distribution of the vector magnetic field around the patch for both frequencies, with and without the load. At 1 GHz, the orientation is almost the same in both cases, with a worst-case coupling (the field is often parallel to a side and, consequently, perpendicular to IC package pins) over a very significant part of the patch perimeter, while the magnitude decreases and becomes much more uniform in presence of the load. At 1.85 GHz, the orientation does not change with the load either (but is the same on the four sides of the patch), while the magnitude distribution exhibits low-color spots at different locations; however, that fact can be neglected, as field lines are perpendicular to the patch left and right sides where magnitude increases (hence, negligible coupling to IC pins); conversely, where field lines are parallel to the top and bottom sides, magnitude is reduced.

In both cases, it can thus be considered that the susceptibility of an IC to magnetic field would decrease (most of the time) or remain unchanged depending on the frequency and the location of the sensitive pins. Meanwhile, it should be remembered that, in all cases, the susceptibility to electric field would decrease.

On the one hand, as most of the μ Cs tend to have an emission spectrum and a susceptibility frequency bandwidth over the 10–100 MHz frequency range, a study was conducted at 60 MHz to check the suitability of the proposed technique at lower frequencies (see Fig. 5). Following the previous reasoning, improvements in immunity as a result of lower EM fields due to loading are evident; the $\|E\|/\|H\|$ ratio at 60 MHz reduces from

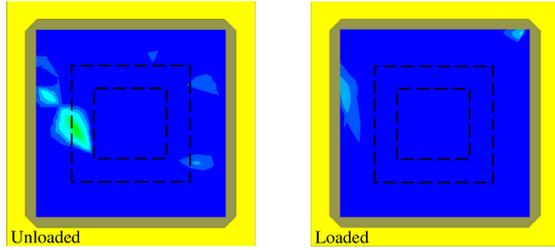


Fig. 5. $\|E\|/\|H\|$ ratio for unloaded and loaded ($\epsilon_r = 2.94$) PCBs for an input power of 1 W at 60 MHz. The scale is the same as in Fig. 2.

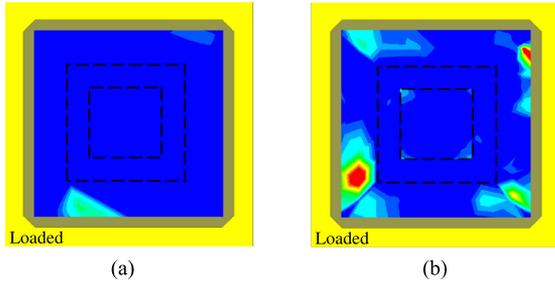


Fig. 6. $\|E\|/\|H\|$ ratio for a loaded PCB with $\epsilon_r = 10.2$ PCB for 1-W input power at (a) 1 GHz and (b) 1.85 GHz. The scale is the same as in Fig. 2.

1400 to 200 Ω (by 85%) for a loaded compared to an unloaded PCB.

On the other hand, since the amount of stored energy in a dielectric is directly proportional to its permittivity, it is expected to have even higher immunity in a loaded IC with higher ϵ_r values. Fig. 6 shows results for a case study with RT/Duroid 6010 loads ($\epsilon_r = 10.2$) demonstrating a significant improvement in wave impedance around the IC where the load is located; it reduces from 800 to 200 Ω (by 75%) for a dielectric load with a higher ϵ_r of 10.2 compared to 2.94.

B. Far Field

A standard TEM cell as the far-field free space condition emulation was used for far-field testing of radiated immunity [22]. Loaded and unloaded versions of the 10 cm \times 10 cm PCB, shown in Fig. 1, were placed on the TEM cell aperture. The IEC standard for VSWR lower than 1.25 was fully met at the TEM cell resonant frequencies. Fig. 7 shows the $\|E\|/\|H\|$ ratio distribution over the PCB at the first two resonance frequencies, i.e., 0.9 and 1.4 GHz [see Fig. 3(b)]. Note that, unlike the septum used in simulation, the one of the real TEM cell is asymmetric, which allows much lower VSWR. As observed, loading neither detunes the frequency nor changes the VSWR level and, hence, the variation in impedance distribution is independent of the load impact on the resonant frequency change.

Following the above-mentioned reasoning at the beginning of the current Section, a first glance at the results in Fig. 7 clearly shows the effectiveness of the proposed dielectric loading technique to improve IC radiated immunity independently of frequency. At both considered frequencies, much lower impedance was observed in the loaded compared to the unloaded PCB around the IC where the dielectric loads are attached; the wave

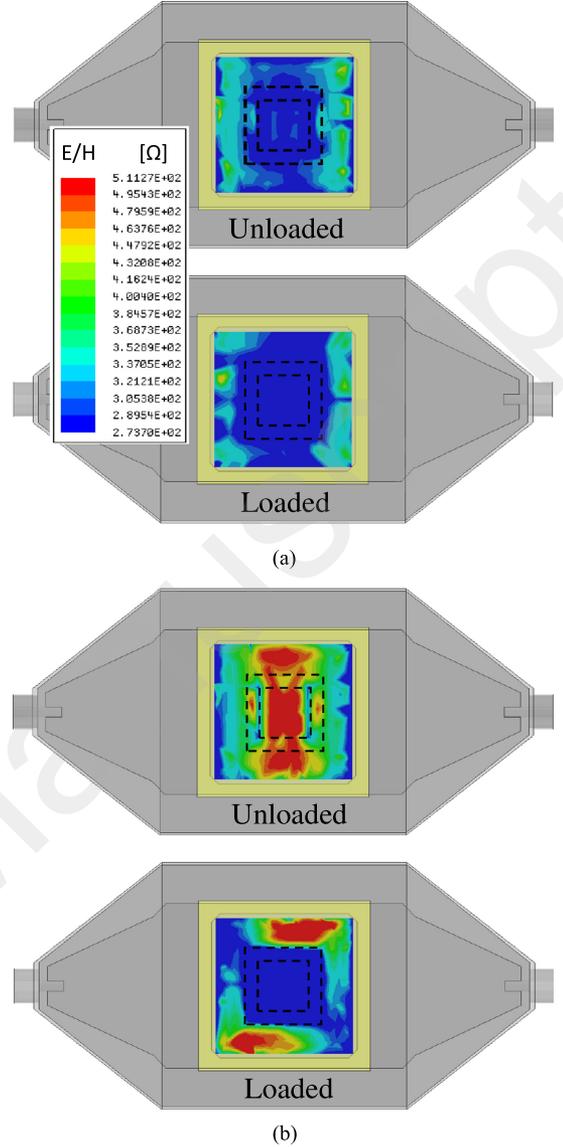


Fig. 7. $\|E\|/\|H\|$ ratio for unloaded and loaded ($\epsilon_r = 2.94$) PCBs inside a standard TEM cell for an input power of 1 W at (a) 0.9 GHz and (b) 1.4 GHz.

impedance at higher frequency is reduced by 46.5% (from 511 to 273 Ω).

A plot similar to Fig. 4 for near field is provided in Fig. 8 for far field. As observed, at both frequencies, the magnetic field on left and right sides of the patch has the same magnitude and orientation with or without any load. On top and bottom sides, higher magnitudes can be observed with the load, but can be neglected due to the magnetic field lines being perpendicular to the patch sides. Note that those simulations were performed at the resonant frequencies of the TEM cell, which is indeed the worst case in terms of field homogeneity. Consequently, the same conclusions can be drawn in a TEM cell: Loading would decrease the susceptibility of an IC both to electric and magnetic fields (or, in the worst case, leave the latter unchanged).

At 60 MHz, thanks to dielectric loading, a similar behavior of the $\|E\|/\|H\|$ ratio to that of higher frequencies (around 1 GHz)

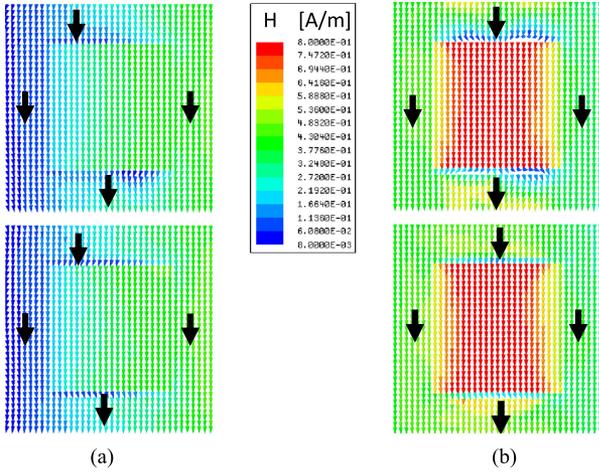


Fig. 8. Simulated vector magnetic field distribution inside the TEM cell around the unloaded (top) and loaded (bottom) patch under the load at (a) 0.9 GHz and (b) 1.4 GHz. Black arrows indicate the privileged orientation.

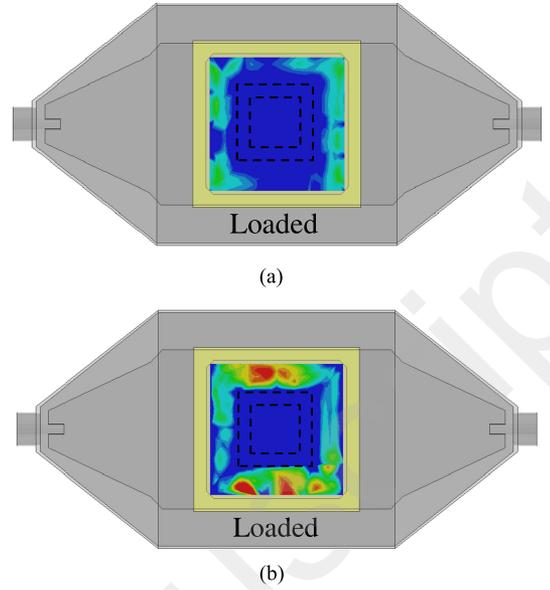


Fig. 10. $\|E\|/\|H\|$ ratio for a loaded PCB with $\epsilon_r = 10.2$ for an input power of 1 W at (a) 0.9 GHz and (b) 1.4 GHz. The scale is the same as in Fig. 7.

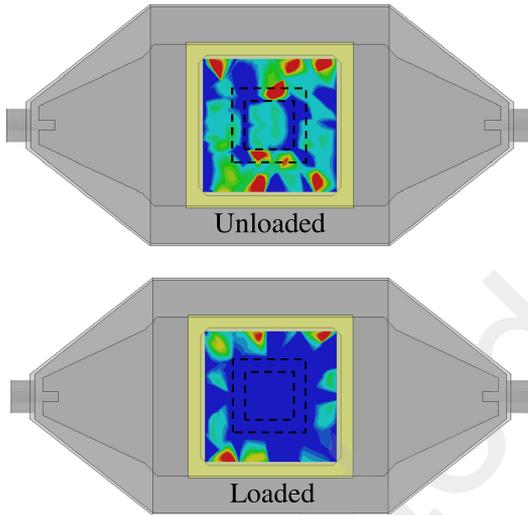


Fig. 9. $\|E\|/\|H\|$ ratio for unloaded and loaded ($\epsilon_r = 2.94$) PCBs for an input power of 1 W at 60 MHz. The scale is the same as in Fig. 7.

was achieved observing lower impedance and consequently less field strength around the IC (see Fig. 9). Therefore, the dielectric loading technique is also effective at lower MHz frequencies where most μC tend to radiate.

A plot similar to Fig. 6 for near field is provided in Fig. 10 for far field in a TEM cell. It can be seen that the higher permittivity ($\epsilon_r = 10.2$) does not provide any $\|E\|/\|H\|$ improvement compared to the lower value ($\epsilon_r = 2.94$).

IV. EXPERIMENTAL RESULTS AND DISCUSSION

Due to the impossibility to measure the EM field directly under the dielectric layer, an indirect measurement technique was set up. It consisted in using an IC (a μC) with an observable criterion for radiated immunity. A loaded IC was compared to an unloaded one through measurements using a standard TEM cell (see Fig. 11).

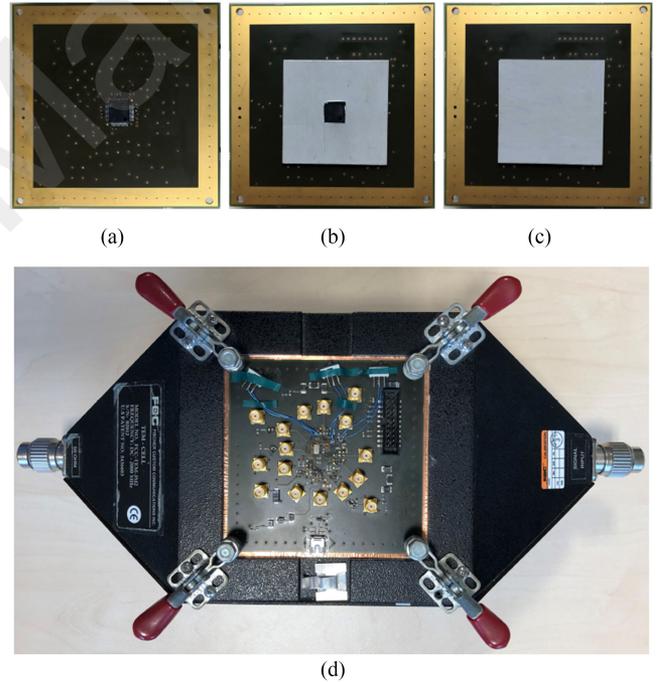


Fig. 11. Measurement setup with a loaded and unloaded 32-bit μC . (a) Unloaded. (b) Partially loaded. (c) Fully loaded. (d) TEM cell used for the purpose of this study [22].

A 10 cm \times 10 cm PCB with a 32-bit μC (ATMEL SAM3S4B) [21] was employed for the experiments (see Fig. 11). The μC was configured to generate a 48-MHz core clock from its internal PLL referenced by an external 18.432 MHz crystal. It was then programmed with simple software toggling one output pin at a fixed frequency (about 1.5 kHz).

A previous measurement campaign highlighted that the clock generation circuitry of that μC was sensitive to continuous-wave

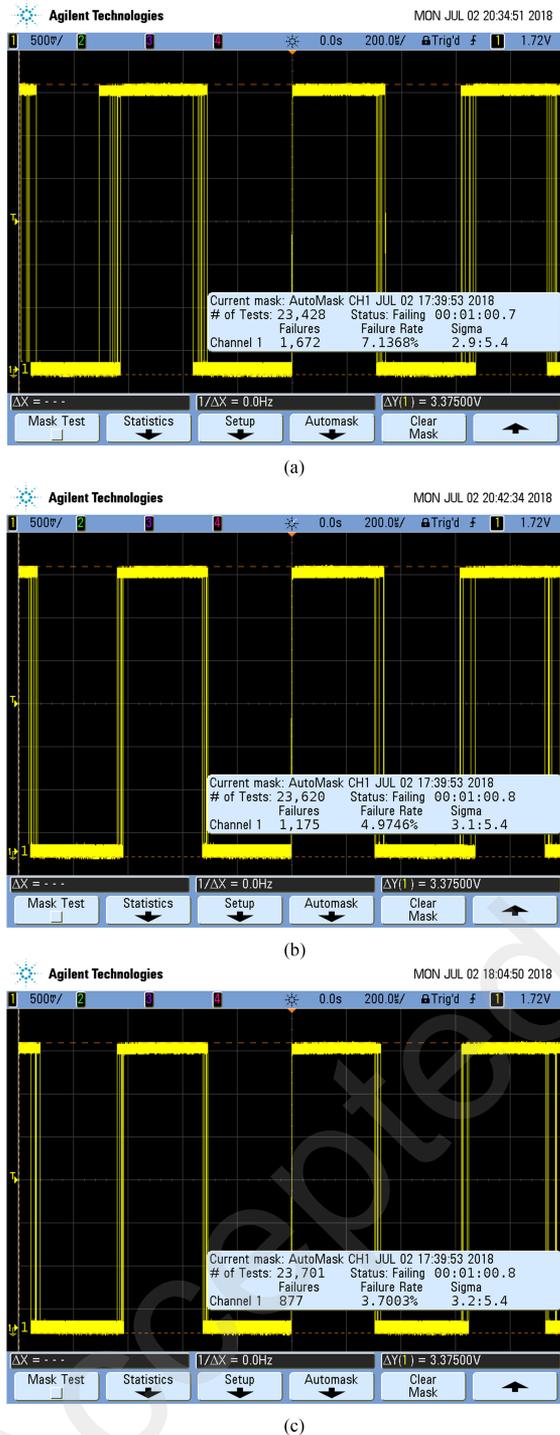


Fig. 12. Measured μC failure rate averaged over a one-minute time slot for an input power of 20 W at 223 MHz. (a) Unloaded. (b) Partially loaded. (c) Fully loaded.

interference at 223 MHz. Therefore, immunity could be assessed by measuring the jitter of the output signal through automatic mask testing, thanks to a Keysight DSO6014L oscilloscope fitted with the appropriate option. The time-domain limit of the mask was fixed at a 5% deviation in signal period in both directions (lower and higher). The immunity criterion was the statistical failure rate (i.e., the output signal leaving the area of the oscilloscope mask) averaged over a one-minute time slot.

The PCB was secured on the aperture of the TEM cell and exposed to radiated interference through continuous-wave power injection into the septum [see Fig. 11(d)], thanks to a Keysight N5183A generator feeding a Prana AP32DT120 20 W power amplifier. The other port of the TEM cell was terminated with a 50- Ω load. Incident and reflected powers were monitored with a Keysight E4419B dual-channel power meter through the built-in directional coupler of the amplifier. As mentioned in Section II, the PLL of a μC is highly sensitive to a tangential magnetic field coupled to its power supply pins (namely V_{DDPLL}), provided that the field component is in the same direction as the loops formed by the pins on the PCB: The PLL is perturbed when the interference is propagated into its power supply rail.

The incident power was measured at 43 dBm (20 W upper limit of the amplifier) while the reflected power was monitored at 15 dBm (31 mW). Of course, the injection frequency was chosen at 223 MHz, in order to make use of the weakness in immunity mentioned previously.

Three different injections were considered: (1) without any dielectric loading [see Fig. 11(a)]; (2) with dielectric loading covering only the PCB traces and μC pins [see Fig. 11(b)]; and (3) with dielectric loading over the whole μC (package and pins) and the PCB traces [see Fig. 11(c)]. They were carried out exactly in the same conditions (same RF power, same PCB location, and orientation). The orientation of the PCB was chosen to maximize magnetic field coupling to the power supply pins. That was demonstrated by the fact that no errors could be observed by rotating the PCB by 90°. Results are shown in Fig. 12 observing a 7.14% failure rate in case (1) [see Fig. 12(a)], 4.97% in case (2) [see Fig. 12(b)], and 3.70% in case (3) [see Fig. 12(c)]. These results clearly demonstrate the improvements in radiated immunity due to dielectric loading in a significant manner. The results also show that dielectric loading not only makes the IC and PCB immune to the electric field, but also decreases the susceptibility of the μC to external magnetic field. From an economic point of view, a dielectric or a non-ferromagnetic material would be a better option compared to a ferrite-based material.

V. CONCLUSION

A dielectric loading technique was proposed to improve the radiated immunity of ICs, which has no side effects on their performances. The behavior of an electronic circuit with a loaded IC was compared to an unloaded one both in near and far fields. It was found that, independently of frequency, a loaded circuit is less susceptible compared to an unloaded one due to the reactive field confinement in the dielectric load without inducing side effects on its performance. Moreover, loading an IC with non-ferromagnetic dielectric material proved to be effective to enhance its susceptibility to both magnetic and electric field, which makes it possible to reduce the cost of the technique compared to the ubiquitous use of ferrites. An experimental show case study using a TEM cell proved a $\sim 48\%$ less failure rate for a loaded μC (ATMEL SAM3S4B) compared to the unloaded IC. The obtained results demonstrate the suitability of the proposed technique as a potential candidate to improve the radiated immunity of electronic devices.

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