



HAL
open science

Electrical model and characterization of Through Silicon Capacitors (TSC) in silicon interposer

Khadim Dieng, Philippe Artillan, Cédric Bermond, Olivier Guiller, Thierry Lacrevez, Sylvain Joblot, Gregory Houzet, Alexis Farcy, Yann Lamy, Bernard Flechet

► To cite this version:

Khadim Dieng, Philippe Artillan, Cédric Bermond, Olivier Guiller, Thierry Lacrevez, et al.. Electrical model and characterization of Through Silicon Capacitors (TSC) in silicon interposer. 2014 International 3D Systems Integration Conference (3DIC), Dec 2014, Kinsdale, Ireland. pp.1-8, 10.1109/3DIC.2014.7152152 . hal-01992256

HAL Id: hal-01992256

<https://hal.science/hal-01992256>

Submitted on 24 Jan 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Electrical Model and Characterization of Through Silicon Capacitors (TSC) in Silicon Interposer

Khadim Dieng^{1*}, Philippe Artillan^{1*}, Cédric Bermond¹, Olivier Guiller², Thierry Lacrevez¹,
Sylvain Joblot², Grégory Houzet¹, Alexis Farcy², Yann Lamy³, Bernard Fléchet¹

¹ Université de Savoie, IMEP-LAHC, UMR CNRS 5130, 73376 Le Bourget du Lac-France

² STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles, France

³ CEA-LETI Minatoc, 17 rue des Martyrs, 38054 Grenoble cedex 9, France

* Corresponding authors: khadim.dieng@univ-savoie.fr, philippe.artillan@univ-savoie.fr

ABSTRACT – Inspired from Through Silicon Vias (TSVs), Through Silicon Capacitors (TSCs) are newly developed capacitors integrated throughout the silicon interposer. This paper deals with a demonstrator which investigates the first process steps of TSCs. A predictive modeling method of the impedance of large matrices of such components is proposed. The modeling method makes use of 2D/3D parasitic extraction software for the modeling of each parts of the structure. The resulting lumped RLCG parameters are used to generate a global equivalent circuit composed of segments of coupled distributed cells. The modeling method is validated by experimental results on the whole frequency range of use (up to 10 GHz). Such components demonstrate simultaneously high capacitance density (up to 23 nF/mm²), low parasitic equivalent series resistance and inductance and high serial resonance frequency (in GHz range for a capacitance value of 10 nF).

I. INTRODUCTION

Applications such as DC-DC converters and Power Distribution Networks (PDN) decoupling require high capacitance density (up to 100 nF/mm²) placed at the vicinity of the dies to avoid noise and ensure reliable operating system [1-2]. Meeting this capacitance densities value implies the use of a large die area. Since the overall dedicated area for the capacitors is constantly reduced, the integration of high value decoupling capacitors for PDN applications in LSI still remains a technological lock. In modern 3D-ICs, decoupling capacitors are placed at each stage and are mainly the Surface Mounted Technology (SMT) capacitors, silicon interposer embedded capacitors and on-chip decoupling capacitors. Depending on their location, capacitors provide decoupling solutions for a given frequency range. The SMT decoupling solution is limited to frequency range below 300 MHz due to their high access impedance from the active dies. On chip decoupling capacitors address frequencies above about 2-3 GHz [3]. Decoupling solutions for the mid-

frequency range could be provided by interposer. Different types of decoupling capacitors are embedded in the silicon interposer. Among them, the majority are Thin Film Capacitors (TFCs), in planar or trench structure. The capacitance density of planar TFCs is limited to 30 nF/mm² for high voltage and low leakage current applications [4], whereas optimized trench capacitors reach capacitance density up to 500 nF/mm² [5]. Nevertheless, the equivalent series resistance can be high due to conductor materials low conductivity. Newly developed 3D decoupling capacitors, named Through Silicon Capacitors (TSCs), are investigated in [6]. Those TSCs present high capacitance density (up to 56 nF/mm²), associated to low parasitic resistance thanks to the technological breakthrough use of copper in the structure.

This paper proposes a predictive modeling method of the impedance for both preliminary TSC components and planar MIM capacitors. Section II describes the technological stack of the components. Section III presents the method that makes use of 2D/3D parasitic extraction software for the modeling of each part of the structure. The resulting lumped RLCG parameters are used to generate a global equivalent circuit composed of segments of coupled distributed cells. The validation of the modeling method is based on impedance measurements on a wide range of frequency in section IV. Section V provides a further study on copper integration in the TSC structure and highlights the improvement of performances in terms of capacitance density and frequency limit of such components for power delivery applications. Finally, section VI provides a brief overview of perspectives of design optimization.

II. TECHNOLOGICAL DESCRIPTION

TSCs are copper vertical cylindrical capacitors inspired from the Through Silicon Vias (TSVs). The TSC technology is based on a MIM stack deposited in deep holes etched in silicon interposer. The goal of the final integration is to integrate the TSC throughout the silicon interposer and to connect the upper and the lower electrodes respectively to the front-side and the backside

of the interposer. This final integration has the advantage of sharing common steps with the TSV realization: DRIE etching, passivation, copper and polymer filling, backside contact. This co-integration with TSVs leads to an overall cost reduction of the process [6].

The presented demonstrator investigates the first process steps of TSCs (Fig. 1). Matrices of deep holes have been filled with a standard capacitive stack TiN (200 nm) / Al_2O_3 (20 nm) / TiN (200 nm) as shown on Fig. 2. The upper and lower electrodes, mentioned as lids in this paper, are on the same side of the silicon interposer. The goals of this demonstrator are to prove the TSC technology feasibility and to evaluate the TSCs performances improvement such as capacitance density increase, parasitic resistance and inductance decrease compared to a planar MIM. The fabrication method is detailed in [7].

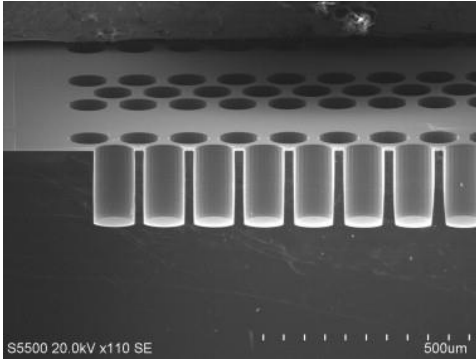


Fig. 1. Tilted SEM cross section of TSC matrix (diameter $100\mu\text{m}$, depth $188\mu\text{m}$). (CEA LETI)

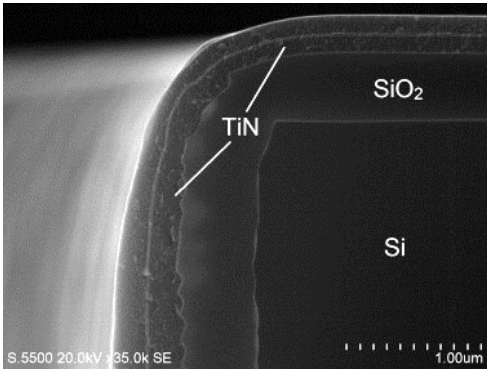


Fig. 2. SEM cross section of a $\text{SiO}_2/\text{TiN}/\text{Al}_2\text{O}_3/\text{TiN}$ stack deposited in a deep hole. (CEA LETI)

Numerous TSCs connected in parallel by lids constitute a matrix. High capacitance density can be achieved by large matrices of TSCs (more than 100). Full simulation of those matrices still remains a challenge due to the number of TSCs and their aspect

ratio. Next section performs a modeling method used to solve large matrices of TSCs.

III. MODELING METHOD

The modeling method developed in this paper allows the estimation of the performances of large matrices of TSCs described in previous section (Fig. 1). As all electromagnetic effects, i.e. inductive effects and resistive losses in conductors and capacitive and conductive losses in dielectrics, are taken into account, the frequency response is valid up to a decade above the serial resonance frequency. Furthermore, the decoupling of electrical and magnetic simulations considerably reduces the computing time, thus allowing the simulation of very large matrices that are unreachable with standard full-wave Finite Element Analysis (FEA) software.

The modeling method is based on a segmented approach of the problem, described in part A. Part B presents the magnetic and electrical models of each cascaded subpart and part C details the combination of all previous models.

A. Presentation of the segmented approach

In order to fit measurements the best as possible, the whole TSC component is simulated in a realistic manner, i.e. the input port is considered at the contact points of a GSG (Ground Signal Ground) RF probe. This can obviously be adapted to other component connection types.

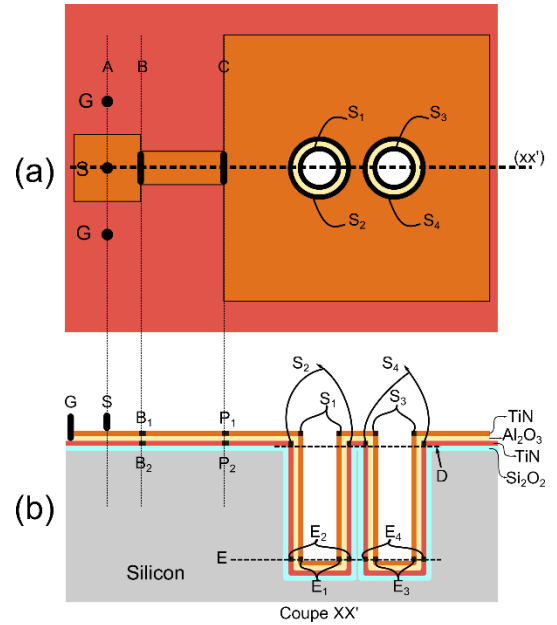


Fig. 3. Schematic representation of a 2 TSCs matrix component. Top view (a) and cross section (b)

The entire structure can be simplified into several cascaded subparts or segments under the assumption that there is no coupling between each segment. Indeed, the one-port capacitive component consists in two parallel metallic conductors separated by a very thin dielectric layer. The current density flows through the two conductors from the port connection on the contact pads to the end of each coaxial element. One can thus define several planes that are perpendicular to the current density direction and use those planes to divide the structure into cascaded segments. As shown on Fig. 3, planes (A) to (E) delimit five such segments.

An equivalent multiport is then defined for each segment (Fig. 4). The two first segments, which correspond to the contact pads are modeled by two-ports Q_{AB} and Q_{BC} . The lids which connect the one-port contact pad output to the n TSCs are modeled by the multiport Q_{CD} . The coaxial part of the TSCs is viewed as a $2n$ -port Q_{DE} with n input-ports and n output-ports. Finally, the back sides of the TSCs are modelled by n coupled admittances, constituting the n -port Q_{end} . The cascaded multiports $\{Q_{AB}, Q_{BC}, Q_{CD}, Q_{DE}, Q_{end}\}$ represent the whole component. The principle of the proposed method is to model separately each multiport and to obtain the admittance Y_{TSC} equivalent to the whole system. Next sections will present how to compute the $[ABCD]$ matrix of each segment and will provide a way to combine all these results to obtain the equivalent admittance Y_{TSC} .

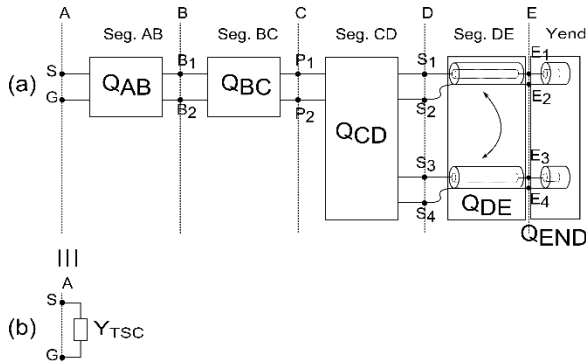


Fig. 4. Segmented equivalent circuit of a 2 TSC matrix (a) and corresponding equivalent admittance (b)

B. Modeling of each segment

Each segment of the equivalent circuit (Fig. 4) is modeled separately from the input (segment AB) to the TSCs end. The objective of each following subsection is to provide the matrices $[Z^M]$ and $[Y^E]$ for each segment. $[Z^M]$ will capture inductive and resistive effects, whereas $[Y^E]$ will capture capacitive and conductive effects. Various methods will be used

depending on the configuration and complexity of each segment.

- Contact pads (segments AB and BC)

Each segment of the contact pads can be viewed as microstrip lines and has thus been simulated by classical approach with Ansys electromagnetic solver suite. Knowing the length of each segment, $[Z_{AB}^M]$, $[Y_{AB}^E]$, $[Z_{BC}^M]$ and $[Y_{BC}^E]$ can easily be computed.

- Lids (segment CD)

Segment CD corresponds to the path of current in metallic lids, between the vertical output plane of the contact pads and the horizontal input plane of the TSCs. This part connects the n coaxial TSCs in parallel. The equivalent multiport is then composed of one input port and n output ports.

Since the number of TSCs in parallel can reach several thousands, a very special care has been taken to make the proposed simulation method efficient and able to address realistic cases. With such constraints, the classical full-wave approach leads to prohibitive computing time or even unsolvable problems, and, in that case, simulation can be performed with quasi-static solvers without lack of precision.

The lids have been modeled with Ansys Q3D quasi-static 3D electromagnetic solver. In this approach, magnetic and electrical fields are computed separately and the proposed method provides $[Z_{CD}^M]$ and $[Y_{CD}^E]$

Magnetic field simulation

The magnetic field computation leads to an equivalent inductive multiport (Fig. 5) and the raw simulation gives the raw inductive impedance matrix Z^{Msimu} .

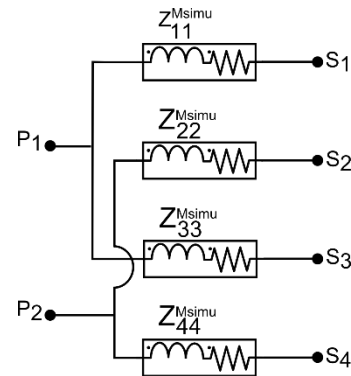


Fig. 5. Magnetic field simulation output matrix Z^{Msimu} for the lids of two TSCs.

The raw simulation matrix $[Z^{Msimu}]$ can be reduced thanks to the following relation:

$$\forall i \text{ et } j \in \{1, \dots, n\}$$

$$Z_{ij}^M = Z_{(2i-1)(2j-1)}^{Msimu} + Z_{(2i)(2j)}^{Msimu} - Z_{(2i-1)(2j)}^{Msimu} - Z_{(2i)(2j-1)}^{Msimu}$$

which defines the equivalent impedance matrix Z^M for the system (Fig. 6). This impedance matrix corresponds to $[Z_{CD}^M]$ in the whole system.

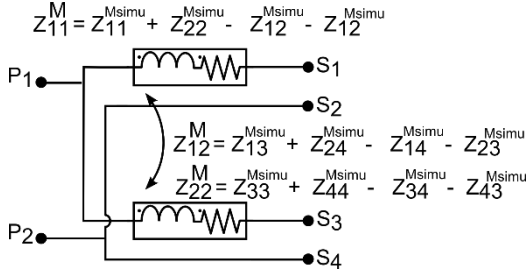


Fig. 6. Reduced impedance matrix $[Z^M]$ capturing the resistive and inductive effects in the lids of two TSCs.

Electric field simulation

On the same pattern, the electric field computation leads to an equivalent capacitive two-port (Fig. 7) and the raw simulation gives the capacitive raw admittance matrix $[Y^{Esimu}]$.

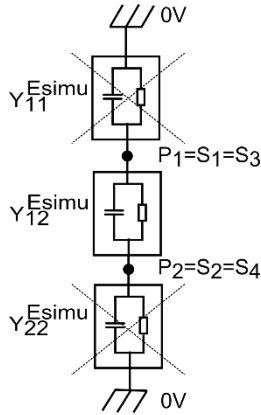


Fig. 7. Electric field simulation output matrix Y^{Esimu} for the lids of two TSCs.

The raw simulation matrix $[Y^{Esimu}]$ can be reduced, assuming that the computed coupling admittance between the two lid plates can be evenly distributed among all TSC contact points. As there are n TSCs, an $n \times n$ admittance matrix $[Y^E]$ is built. Furthermore, since the two metallic plates are very close one from another, the n subparts are supposed to be in total influence. $[Y^E]$ is thus a diagonal matrix with equal diagonal coefficients :

$$Y_{ij}^E = \begin{cases} -\frac{Y_{12}^{Esimu} + Y_{21}^{Esimu}}{2n} & \text{if } i = j \\ 0 & \text{otherwise} \end{cases}$$

The signification of the coefficients of the equivalent capacitive admittance matrix $[Y^E]$ is illustrated on

Fig. 8. This admittance matrix corresponds to $[Y_{CD}^E]$ in the whole system.

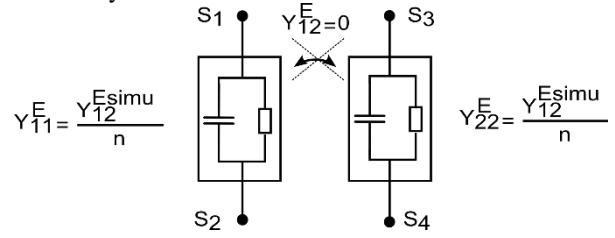


Fig. 8. Reduced admittance matrix $[Y^E]$ capturing the conductive and capacitive effects in the dielectric between the lids of two TSCs.

- Coaxial TSC body (Segment DE)

The coaxial TSC bodies can be viewed as coupled coaxial transmission lines and, as so, have been simulated with a 2D full-wave approach, using the 2D solver of Ansys Q3D Extractor. The output linear matrices $[R]$, $[L]$, $[C]$, $[G]$ are used to compute $[Z_{DE}^M]$ and $[Y_{DE}^M]$.

$$\begin{aligned} [Z_{DE}^M] &= [R]l + j\omega[L]l \\ [Y_{DE}^M] &= [G]l + j\omega[C]l \end{aligned}$$

where l is length of the coaxial body of TSCs.

- TSC end (Y_{end})

For the considered components, an analytic formulation of the admittance of the back side of the TSCs has turned out to be sufficient. Considering the real permittivity ϵ' and conductivity σ of the dielectric material, the equivalent admittance Y_{end} of the back side of a single TSC can be written as:

$$Y_{end} = j\omega \frac{(\epsilon' - j\frac{\sigma}{\omega})S}{t}$$

where S is the surface of parallel metallic plates of the back side and t the distance between them.

C. Equivalent admittance of the entire TSC matrix component

The whole multiport cascade can finally be reduced into a single admittance Y_{TSC} by bringing back the admittance Y_{end} , segment by segment, back to the input port of the device. Each segment is considered as coupled distributed cells composed of Z^M in series and Y^E in parallel (cf. Fig. 9).

By analogy with coupled transmission lines theory, and based on [8], one can use the following transformation for the bringing back of admittance matrix $[Y_{load}]$ through a segment characterized by inductive impedance matrix $[Z^M]$ and capacitive admittance matrix $[Y^E]$:

$$[Y_{eq}] = F([Z^M], [Y^E], [Y_{load}])$$

where :

$$\begin{aligned} [Y_{eq}] &= [\sinhm([\gamma l]) \cdot [Z_c]^{-1} \cdot [Y_{Load}]^{-1} \\ &+ \coshm([\gamma l]) \cdot [[Y^E]^{-1} \cdot \coshm([\gamma l]) \cdot [Y^E] \cdot [Y_{Load}]^{-1} \\ &+ Z_c \cdot \sinhm([\gamma l])]^{-1} \end{aligned}$$

$$[\gamma l] = \text{sqrtn}([Y^E] \cdot [Z^M])$$

$$[Z_c] = \text{sqrtn}([Y^E]^{-1} \cdot [Z^M])$$

and where *sqrtn*, *sinhm*, *coshm* respectively denote the matrix square root, matrix hyperbolic cosine and matrix hyperbolic sine functions. It is interesting to note that this formulation does not require the definition of coupled lines lengths (*l*), but only uses the matrix $[\gamma l]$ which is analogous to but is not the product of a propagation constant matrix and coupled lines lengths.

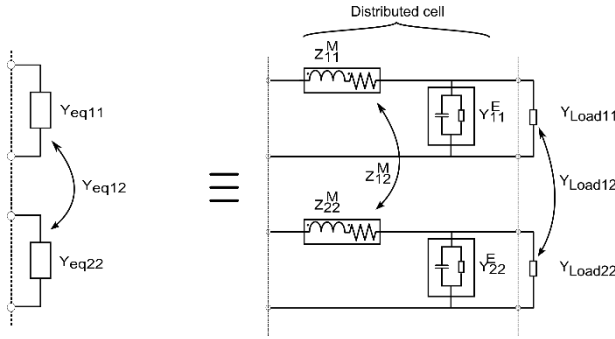


Fig. 9. Combined reduced impedance matrix Z^M and reduced admittance matrix Y^E , for a given segment, assuming even distribution of inductive and capacitive effects.

The defined transformation $F([Z^M], [Y^E], [Y_{load}])$ is successively applied to each segment of the system:

Segment DE:

$$[Y_{eqD}] = F([Z^M_{DE}], [Y^E_{DE}], [Y_{end}])$$

Segment CD:

$$[Y_{eqC}] = F([Z^M_{CD}], [Y^E_{CD}], [Y_{eqD}])$$

(at this step, all the ports of plane C are connected together in parallel)

$$Y'_{eqC} = \sum_j \sum_i Y_{eqC_{ij}}$$

Segment BC:

$$Y_{eqB} = F(Z^M_{BC}, Y^E_{BC}, Y'_{eqC})$$

Segment AB:

$$Y_{TSC} = F(Z^M_{AB}, Y^E_{AB}, Y_{eqB})$$

Finally, the presented method provides the impedance Z_{TSC} for the whole system at each frequency points:

$$Z_{TSC} = \frac{1}{Y_{TSC}}$$

IV. EXPERIMENTAL RESULTS AND MODEL VALIDATION

The preliminary TSC devices using TiN as conductor metal, presented in *section II*, have been characterized over a large frequency range:

- From 100 Hz to 110 MHz with Agilent 4294A impedance analyzer using a 42941A coaxial probe,
- From 10 MHz to 10 GHz with Agilent N5247A PNA-X network analyzer,
- and a Cascade Microtech® GSG $|Z|$ probe.

Numerous small and large matrices of TSCs have been considered for both the validation of the modeling method and the evaluation of the performances of realized components.

TABLE I. CHARACTERIZED AND MODELED COMPONENTS.

TiN component	Geometrical description				Extracted values	
	Dimensions [μm]	Number of TSCs	TSC diameter [μm]	TSC depth [μm]	C_{TSC} [nF]	f_c (cut-off frequency) [MHz]
TSCx1	220x220	1	100	188	0.37	7.90
TSCx8	340x340	8	60	168	1.45	1.60
TSCx20	640x640	20	100	188	6.03	0.25
TSCx42	640x640	42	60	168	6.70	0.19
TSCx85	640x640	85	40	152	7.67	0.12
TSCx120	640x640	120	40	152	10.26	0.10

The modeling method has been tested on six components, presented in table 1. The variety of the chosen components guarantees the validation of the model over a wide range of cases: study cases including single TSC case and realistic cases including a large matrix of 120 TSC on a surface of 0.4 mm². The impedance responses are reported on Fig. 10-11 for components TSCx1, TSCx8 and TSCx20 and on Fig. 12-13 for components TSCx42, TSCx85 and TSCx120.

Equivalent impedance magnitude and angle curves (Fig. 10 and Fig. 12) show very good agreement between model and measurements on the whole frequency range, proving that capacitive and conductive

effects in dielectrics, as well as inductive and resistive effects in conductors, are well taken into account. The parallel capacitance curve (Fig. 11 and Fig. 13) has been directly calculated from impedance values using the relation $C_p(f) = \frac{Im[1/Z(f)]}{2\pi f}$.

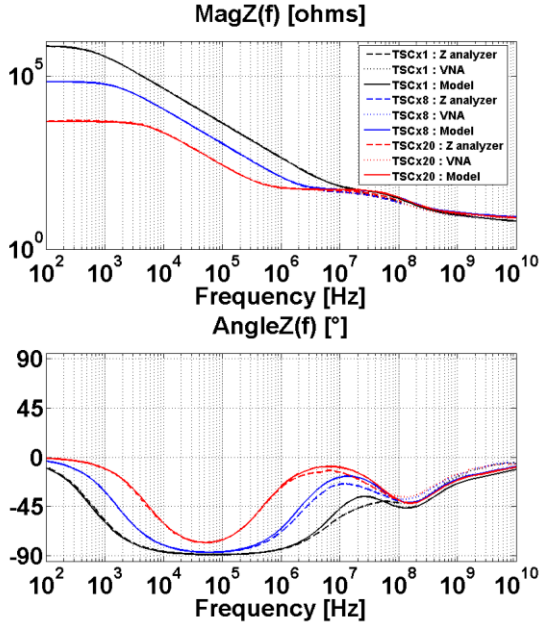


Fig. 10. Measured and simulated impedances frequency responses of components TSCx1, TSCx8 & TSCx20, presented in terms of Magnitude of $Z(f)$ and angle of $Z(f)$.

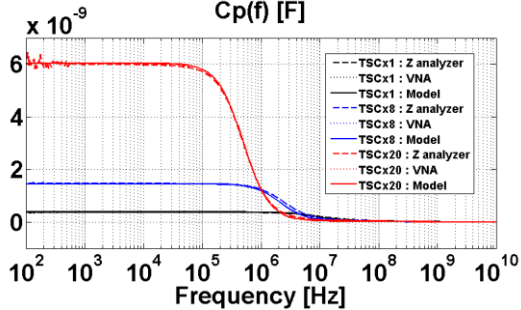


Fig. 11. Measured and simulated equivalent parallel capacitance (C_p) frequency responses of components TSCx1, TSCx8 & TSCx20.

The low frequency part of the curves gives the capacitance C_{TSC} of the components. Higher frequency part of the curves shows cut-off frequencies f_c due to high Equivalent Serial Resistances (ESR). This ESR is the consequence of low conductivity TiN ($\sigma_{TiN} = 460 \text{ kS} \cdot \text{m}^{-1}$). The frequency performances of the final components will be drastically enhanced by adding a thick copper layer to the TiN based MIM stack. Section V presents a complete study of performances improvement.

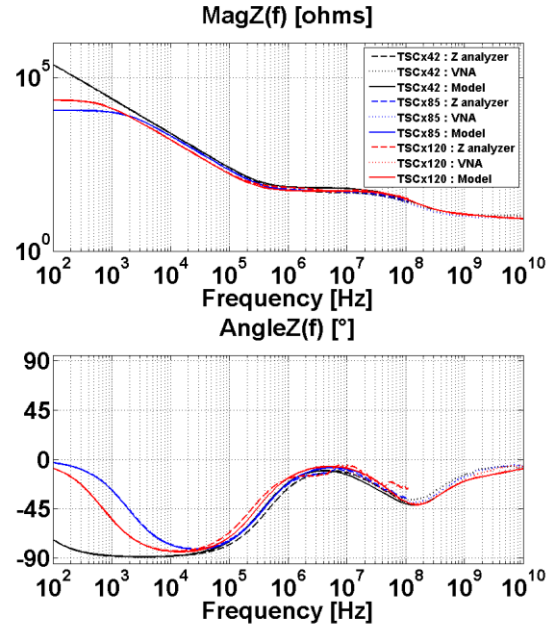


Fig. 12. Measured and simulated impedances frequency responses of components TSCx42, TSCx85 & TSCx120, presented in terms of Magnitude of $Z(f)$ and angle of $Z(f)$.

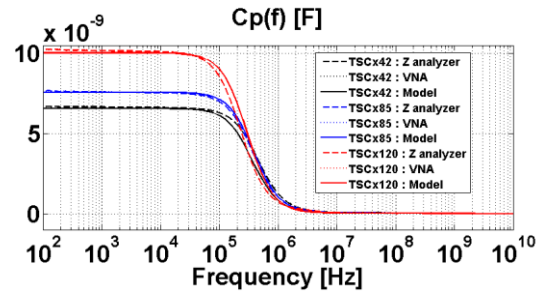


Fig. 13. Measured and simulated equivalent parallel capacitance (C_p) frequency responses of components TSCx42, TSCx85 & TSCx120.

V. PERFORMANCE ANALYSIS

Integrated capacitors for decoupling solutions in power management systems need to satisfy two performance criteria: high capacitance density and large frequency domain of use.

A. Frequency performances

Prototypes of TSC matrices using a copper layer of a higher thickness and lower resistivity are now being investigated. The technological feasibility of electroplated copper deposit both for lids electrodes and inside the coaxial structures has already been proven [3]. Simulations based on the proposed modeling method have been performed to infer copper TSC performances. The thickness of the lids has been set to $3\mu\text{m}$ and the

conformal deposit inside coaxial structures have been set to $1.5\mu\text{m}$ each. The copper conductivity is $\sigma_{Cu} = 45 \text{ MS/m}$. Relative permittivity of alumina has been extracted from planar MIM capacitors ($\epsilon_{rAl_2O_3} = 8.56$) and loss tangent has been set to a standard pessimistic value ($\tan \delta_{Al_2O_3} = 6 \times 10^{-4}$). Other geometrical dimensions of copper components are rigorously identical to TiN components. Modeled copper components are listed in table 2 and their associated impedance responses are reported in terms of impedance magnitude and angle in Fig. 14 and equivalent parallel capacitance in Fig. 15.

TABLE 2. SIMULATED COMPONENTS WITH COPPER.

Copper component	Extracted values			
	C_{TSC} [nF]	SRF (Serial Resonance Frequency) [GHz]	ESR [mΩ]	ESL [fH]
TSCx42	6.27	5.61	7.3	128
TSCx85	7.57	> 10	< 3.2	< 33
TSCx120	9.97	3.73	2.53	182

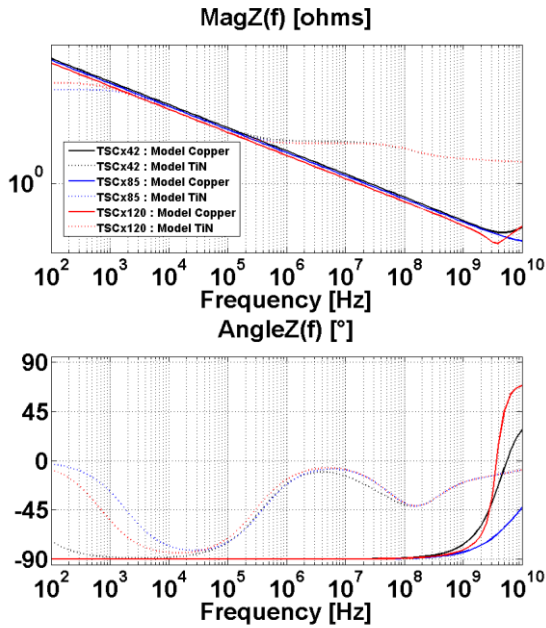


Fig. 14. Simulated impedances frequency responses of components TSCx42, TSCx85 & TSCx120, presented in terms of Magnitude of $Z(f)$ and angle of $Z(f)$ depending on used conductor (TiN or TiN+Copper)

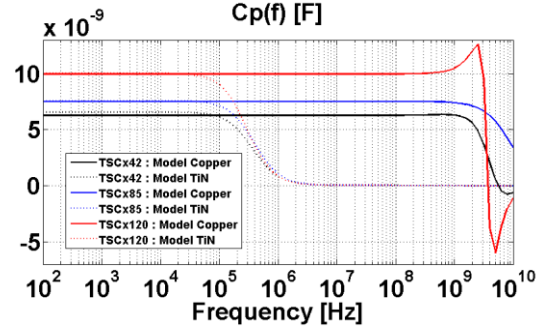


Fig. 15. Simulated equivalent parallel capacitance (C_p) frequency responses of components TSCx42, TSCx85 & TSCx120 depending on used conductor (TiN or TiN+Copper)

As can be seen on Fig. 15, the nominal capacitance values of copper components are almost the same as TiN components. Furthermore, the cut-off phenomena (due to resistive conductor losses) disappears in copper components and their frequency range of use is only limited by serial resonance (due to inductive effects). The Serial Resonance Frequency (SRF) is above several gigahertz for all studied components (cf. table 2). Finally, the Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL) have been extracted from impedance curves (Fig. 14) and reported in table 2. Low ESR values and very low ESL values confirm that the copper components present great interest for high frequency decoupling capacitor integration in silicon interposers. By the way, it is interesting to mention that the well spread rule of inverse dependency of ESR and ESL with the number of parallel vertical capacitors is not verified when realistic components are considered, due to the important effect of lids and other access connections. Nevertheless, table 2 shows that ESR tends to decrease when the number of coaxial TSCs increases.

A. Realized capacitance density

Planar MIM capacitors have been realized on the same wafer, using the same stack (TiN/ Al_2O_3 /TiN) as the TSCs in order to evaluate the capacitance improvement due to TSC technology.

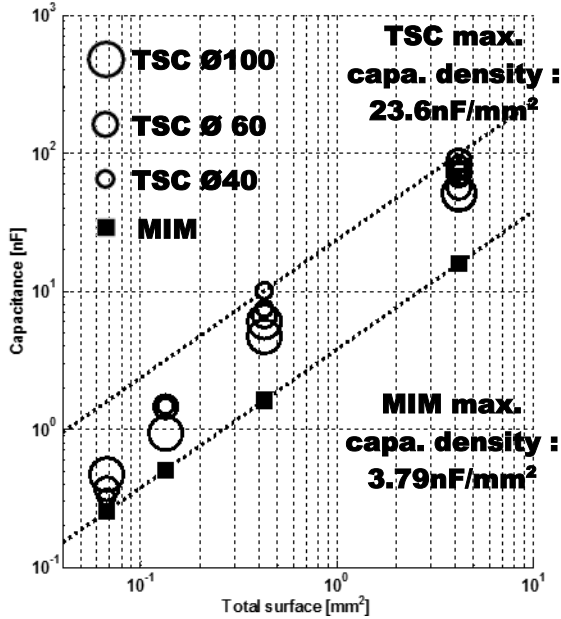


Fig. 16. Realized capacitance vs. total surface of MIM capacitors and TSC-matrix capacitors. TSC-matrix capacitors are matrices of cylindrical TSCs of diameter 40 μm , 60 μm or 100 μm . The dotted lines indicate constant capacitance surface densities.

Fig. 16 compares the maximum capacitance density of standard planar MIM technology (3.79 nF/mm²) and TSC technology (23.6 nF/mm²). TSCs demonstrate a significant increase of capacitance density up to a factor 6.

VI. PERSPECTIVE

As demonstrated by results of previous section, copper TSCs are very promising thanks to good performances in terms of capacitance density and serial resonance frequency. The modeling method used to predict this behavior has been applied to trench structures described in Fig. 1. Simulations of fully through going structures as shown on Fig. 17 would also be worth being performed for performance comparison. In that case, the current density flows in the same direction for both conductors of TSC bodies, thus disabling the coaxial decoupling effect. Such structures would then necessitate another modeling method that does not implement distributed cells but, on the contrary, makes use of lumped element cells, e.g. a method based on Partial Element Equivalent Circuit (PEEC) [9].



Fig. 17. Schematic representation of fully through going TSCs component in silicon interposer.

VII. CONCLUSION

A powerful predictive modeling method for through silicon capacitors has been proposed and validated by measurement on preliminary components using TiN conductors. This approach allows the simulation of large matrices (≥ 1000) of TSCs at least up to a decade above the serial resonance frequency. Final components made of electroplated copper have then been simulated. The predicted impedance responses show very promising performances in terms of capacitance density (23 nF/mm², six times more than equivalent planar MIM technology) and frequency limit (in GHz range) for 3D-IC power distribution networks decoupling applications.

REFERENCES

- [1] P. Artillan, et al., "Integrated LC filter on silicon for dc-dc converter applications". IEEE Transactions on Power Electronics, 26(8), pp. 2319-2325, 2011.
- [2] P. Muthana et al., "Mid frequency decoupling using embedded decoupling capacitors," IEEE 14th Topical Meeting on Electrical Performance of Electronic Packaging, pp.271-274, Oct.23-26, 2005.
- [3] D.I. Amey et al., "Application of embedded capacitor technology for High performance semiconductor packaging", DesignCon 2007.
- [4] Y. Wang et al., "Solution-derived electrodes and dielectrics for low-cost and high-capacitance trench and Through-Silicon-Via (TSV) capacitors". IEEE 61st Electronic Components and Technology Conference (ECTC), pp. 1987-1991, 2011.
- [5] F. Lallemand, et al., "Silicon interposers with integrated passive devices, an excellent alternative to discrete components," European Microelectronics Packaging Conference (EMPC), pp.1.6, 9-12 Sept. 2013.
- [6] O. Guiller et al., "Through Silicon Capacitor co-integrated with TSV as an efficient 3D decoupling capacitor solution for power management on silicon interposer," IEEE 64th Electronic Components and Technology Conference (ECTC), pp.1296-1302, May, 27-30, 2014.
- [7] O. Guiller et al., "Through Silicon Capacitor co-integrated with TSVs on silicon interposer". Microelectronic Engineering, vol. 120, p. 121-126, December 2013.
- [8] A. Aziz Bhatti, "A computer based method for computing the N-dimensional generalized ABCD parameter matrices of N-dimensional systems with distributed parameters." IEEE Twenty-Second Southeastern Symposium on System Theory, 1990.
- [9] A. E. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems." IEEE Transactions on Microwave Theory and Techniques, 22(3), pp. 216-221, 1974.