



**HAL**  
open science

## Mixed-signal test automation: are we there yet?

G. Leger, Manuel J. Barragan

► **To cite this version:**

G. Leger, Manuel J. Barragan. Mixed-signal test automation: are we there yet?. IEEE International Symposium on Circuits & Systems (ISCAS'2018), May 2018, Florence, Italy. 10.1109/IS-CAS.2018.8351734 . hal-01989162

**HAL Id: hal-01989162**

**<https://hal.science/hal-01989162v1>**

Submitted on 2 Oct 2020

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

# Mixed-signal test automation: are we there yet?

Gildas Leger

Instituto de Microelectrónica de Sevilla  
CSIC-Universidad de Sevilla  
Av. Américo Vespucio s/n, 41092 Sevilla, Spain.

Manuel J. Barragan

Univ. Grenoble Alpes, CNRS, Grenoble INP\*, TIMA  
F-38000 Grenoble, France

**Abstract**—Testing analog, mixed-signal and RF (AMS-RF) circuits represents a significant cost component for testing complex SoCs. Moreover, AMS-RF test generation and validation are still largely handcrafted tasks that rely on expert design knowledge for each particular Device Under Test (DUT). Mixed-signal test automation has been sought by the test community for the last decades, trying to mimic the success of digital test approaches. Indeed, in the digital domain, test is vastly automated and standard techniques are already available (ATPGs, BIST, scan registers, etc.). In the last decade, a methodology based on leveraging the power of machine learning algorithms has been proposed for AMS-RF circuits that opens the door to a higher level of automation. In this paper we review recent results in this line and try to put together what could be such a complete methodology and what remains to be done.

## I. INTRODUCTION

Nowadays, traditional specification-based functional test continues to be the golden standard for AMS-RF production test. However, the wide variety of AMS-RF circuits and the huge number of their associated specifications make functional test automation a challenging task. Obviously, testing an RF transceiver is completely different from testing an Analog-to-Digital Converter, and they actually require different dedicated test equipment. That being said, there exist some attempts to systematic functional test for some circuit families, essentially Built-In Self Test (BIST) approaches [1]–[5]. BIST techniques move the test problem to the design stage by embedding test instruments together with the Device Under Test (DUT). The path to automation of such approaches would parallel that of “conventional” automated design synthesis [6] since co-design is mandatory.

In the last few years the preeminent position of functional specification test for AMS-RF testing has been challenged. Current market trends in rapidly growing sectors (e.g., automotive, space, healthcare, etc.) put a lot of pressure on quality and reliability. A defect that induces no performance loss at production time may be unacceptable as a potential threat for field operation. The goal is to achieve sub-ppm defect levels and, as a matter of fact, functional tests are not enough for guaranteeing this target defect coverage. Moreover, the *a priori* evaluation of defect coverage for functional test is seldom carried out due to computational power constraints.

In the last decade, a promising alternative to functional test has been proposed based on leveraging the power of advanced machine learning algorithms [7]. The core idea is

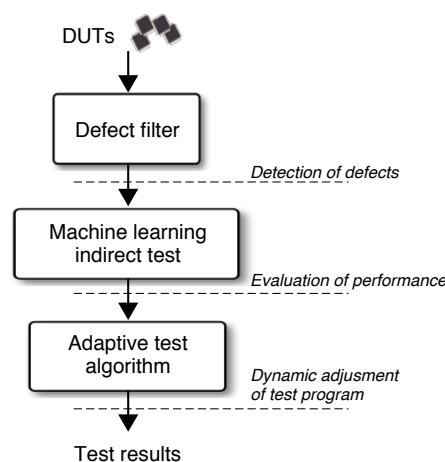


Fig. 1. Generic test flow for machine learning indirect test.

to build a mapping model from simple measurements, usually called signatures, to the set of functional specifications. The benefits of this machine learning indirect test methodology are threefold. First, the outcome of the test can be interpreted in a conventional manner: the estimated specifications are directly compared to their test acceptance windows. Second, the simple measurements are devised to be cheaper than their functional counterparts. And third, these simple measurements can also be tailored to yield a higher defect coverage.

Figure 1 depicts a generic flow for machine learning indirect test. The premise of machine learning indirect test is that the simple measurements and the specifications are correlated since their variations are controlled by the same statistical process (i.e., the parametric stochastic variations of the fabrication process). Thus, in a first stage, a defect filter is trained to screen out any outlier (which usually corresponds to a spot defect) that doesn't belong to the expected nominal distribution. Next, a machine learning regression model is trained and used to replace specification tests. Finally the test procedure can be completed by adaptive schemes that update test parameters to the possible evolutions or drifts of the fabrication process. In this paper we discuss recent advances in machine learning indirect test. The following sections develop the three steps of the test flow depicted in Fig. 1 with an accent on their automation potential.

\*Institute of Engineering Univ. Grenoble Alpes

## II. DEFECT FILTER

Machine learning indirect test is aimed at identifying extreme process variations that lead to malfunction of the DUT. In fact, defects not related to process variations may not be detected. In this scenario, a necessary first step to assure the correctness of the complete test flow is to screen out these non-parametric defects that may not obey the correlation function between signatures and specifications. This first step is usually known as a defect filter.

Defect filters were first proposed in [8]. The original implementation of the defect filter is aimed at detecting outliers in the nominal multidimensional distribution of a set of signatures. Instead of looking at the marginal distribution of the signatures individually, the authors propose to build a non-parametric multidimensional estimate of the joint probability density function of signatures from a subset of devices. The evaluation of a new device in the production line consists in performing the signature measurements and then computing its associated probability of occurrence. If this probability is below a given acceptance threshold, the device is considered as an outlier and screened out. The procedure of learning the joint probability density function can easily be automated since it relies on well known statistical tools (one-class classifiers, non-parametric kernel density estimation, etc.) [9].

However, a question remains unanswered: how can we guarantee that a given defect filter has a good defect coverage? Answering this question requires: a) proposing a set of appropriate signatures, meaning that the defects should appear as outliers with respect to their nominal parametric joint distribution; and b) either finding a mathematical proof of correctness, or being able to evaluate test coverage with sufficient accuracy. From an EDA viewpoint a) is related to Automated Test Pattern Generation (ATPG) and b) is related to formal verification and defect simulation.

In an ideal scenario, we should be able to propose appropriate signatures prior to performing any simulations, relying on some form of formal proof. Unfortunately, we are not aware of any such systematic formal approach except for the simplest circuit families, such as linear time-invariant circuits [10]. Instead of that, most approximations try to capture the designer expertise to propose *ad hoc* sensitive signatures for a given DUT. Then, an optimization loop can be employed to maximize this sensitivity to defects, that is, to maximize defect coverage. As a matter of fact, any defect-oriented test strategy may be used as a starting point for building a defect filter [11]–[14].

For the sake of brevity we cannot review all the proposals in the literature, but let us comment the recent generic proposal in [11] that takes automation into account. The main idea of this approach consists in measuring the DC voltages at primary outputs and some internal nodes, which would require some DfT modifications. In addition, since the sensitivity of these signatures may not be sufficient, authors propose to introduce some circuit topological modifications during test mode that are supposed to facilitate the detection of defects.

These topological modifications are carried out by introducing pull-up or pull-down DfT transistors on selected nodes. Both the selection of internal DC probes location and the DfT pull-up and pull-down insertion points are automatically optimized using a multi-objective genetic optimization algorithm that tries to minimize circuit modifications while maximizing defect coverage. Though it is a step in the right direction, this strategy has still some limitations: the DfT structures should be co-designed with the DUT (this is thus a problem of automated design synthesis), and some defects may not be detected by DC-only measurements (for instance an open in a unit capacitor).

In general, within the framework of defect-oriented test strategies, test coverage must be estimated, if not for optimization, at least for validation. This represents a key roadblock for the whole process. Indeed, estimating test coverage *a priori*, during the design stage, requires defect simulation and this leads to additional challenges. AMS-RF defect simulation is an old topic that has regained recent interest in the test community. A sound methodology has actually been proposed in the 80s, the so-called Inductive Fault Analysis [15]. It consists in randomly introducing disks of extra or missing material in the different layers of the DUT layout (with the radius and the layer probability coming from fab data) to induce shorts and opens with realistic likelihoods. Another simplified approach that led to a commercial tool consists in extracting shorts and opens likelihoods based on extracted parasitics. Short likelihood is deemed to be proportional to parasitic resistors in a given layer, while open likelihood is proportional to parasitic capacitance [16].

However, the main problem is not probabilistic defect generation, but the simulation of the defect itself. First of all, there are no widely accepted simulation models for defects, particularly for opens [17], [18]. Secondly, some defects lead to simulation convergence issues. And finally, the computational burden of simulating a sufficiently representative set of defects is prohibitive for practical industrial designs. Recent efforts have been carried out to address these issues, like the standardization of AMS-RF defect modeling and definition [19]. In addition, simulation frameworks have been proposed in order to minimize the number of defects to be simulated for a robust test coverage estimation (within a given confidence interval) [16], [20]. These works propose to use likelihood weighted random sampling of defects in order to avoid any selection bias while simulating a representative (but as reduced as possible) set of defects.

From an EDA point of view, it is clear that systematic approaches to defect filtering exist and could be automated, although the computational burden of test validation continues to be a challenge.

## III. MACHINE LEARNING INDIRECT TEST

As it was mentioned in the introduction, machine learning indirect test is aimed at replacing the measurement of complex functional specifications by a set of simpler signatures. A

machine learning regression algorithm is used to map the signatures to the specifications. Conceptually this is not different from the linear approach proposed in [21]. However, using modern regression tools greatly extends the validity range of the models.

The usual approach to machine learning indirect test is based on supervised machine learning algorithms. The process is developed in two stages: a learning stage, and a testing stage. During the learning stage both performance parameters and signatures are measured from a set of training devices. A machine learning algorithm is then trained over the two sets of measurements to build a mapping model. In the testing stage, signatures are measured for each DUT, and performances are inferred by using the mapping model obtained in the previous stage. Test result interpretation is the same as in conventional functional test. This is an elegant way to deal with the issue of valid ranges of acceptance, and also gives a valuable insight into reliability since we can estimate how far the circuit is from its nominal specification. In addition, machine learning algorithms are designed to handle complex multi-dimensional and non-linear relations like those between defects and specifications, and by extension, between signatures and specifications.

Machine learning indirect test is a promising test framework that is very suitable for its automation. However, it is not free of shortcomings that should be addressed. Maybe the first question for someone not familiar with this approach would be the selection of a suitable regression model and how to train it robustly. There exist plenty of regression models in the Statistics literature with different characteristics. In a first approximation, the choice of the model should rely on comparing the number of reliable signatures to the number of samples in the training set. Models with high bias and low variance (like linear models) are best suited for situations with a small number of training samples with respect to the number of signatures. On the contrary, models with high variance and low bias (like nearest neighbors) may be better suited in situations where a lot of data is available for a few signatures. In the major part of the test-related literature, relatively few signatures are considered and the most used models are possibly Multivariate Adaptive Regression Splines (MARS) [22]–[24] and Neural-Networks (typically perceptron models) [25], [26]. The possibility also exists to use classifiers instead of regression models, but this gives a much more defect-oriented flavor to the approach that we will keep out of the scope of this paper.

Anyway, if model selection is a concern, there are some techniques to automate this decision. One that we have used in the past, which also improves the robustness of the predictions, is called ensemble learning [27], [28]. Ensemble learning relies on a cross-validation process which consists in randomly splitting the training set in a number  $N$  of partitions. One of these partitions is set aside as a validation set and a model is trained on the union of the remaining  $N - 1$  partitions. Then, the prediction error is computed for the samples in the validation set and the operation is repeated by leaving a different partition

out for validation. The final model is a weighted average of the  $N$  trained models, where each individual model is weighted by the inverse of its generalization error. Notice that such an ensemble can be produced from a single model type, or from a mixture of models. The final weighted averaging implicitly performs model selection, and the variability of the generalization error in the  $N$  partitions can also be used as an indication of the robustness of the modeling process [29].

One of the key issues to enable machine learning indirect test automation is the definition of an appropriate set of signatures. It is obvious that such a set must capture the major part of the circuit parametric variability but with limited redundancy. In practice, signature sets are proposed based on expert knowledge but are usually suboptimal: they may contain redundant information, noisy signatures, signatures that are actually uncorrelated to the target performances, and even some functional test measurements. The statistic field of feature selection comes at hand to clean up such an *ad hoc* signature set. A variety of feature selection proposals can be found in the literature based on different strategies [30]–[37].

A direct approach to feature selection consists in preselecting a subset of features, based on some statistical observations, before training any regression models. This approach, widely used when the number of initial features is high, is known as filtering. Different approaches have been presented in the last few years based on non-linear correlation metrics [33], [34], PCA [36], mutual information [35], etc. However, filtering approaches tend to capture only the most significant variation components. If more accuracy are required, it is necessary to resort to wrapper techniques. Basically, a wrapper algorithm uses the machine learning prediction model as a black box within an optimization loop, with the objective of finding the subset of signatures of minimum cost that minimizes the prediction error in an independent validation set [30], [32]. The main drawback of wrapper approaches is the computational burden of the search in the input space of features, specially when the cardinality of this set is high. In such cases, hybrid filtering-wrapper approaches can be considered to guide the search in the input signature space based on the dynamic evaluation of a correlation metric [31].

While feature selection can be considered a solved problem, proposing the original set of features remains as an open problem for the automation of the test flow. Just like for the defect filter, this issue is equivalent to the definition of an appropriate ATPG: we need systematic strategies. In this line, some work has been presented for guiding the design of new features based on the missing information in the input set of signatures with respect to the Monte Carlo process parameters [30]. This diagnosis information help designing new tests that specifically target that missing information. Another approach to the problem consists in optimizing the input stimulus and the output measurements. This is the approach in [24] where the break point coordinates of a piece-wise linear stimulus are optimized together with the capture times of the output waveform in order to minimize the prediction error of the regression model. While this is a sound strategy the choice

and the parametrization of the input stimulus and output measurements are still *ad hoc*. In addition the computational cost is high since the optimization loop embeds a full Monte Carlo electrical simulation campaign for each iteration.

Another key roadblock for the automation of the machine learning indirect test is the validation of the test itself. The computational cost can be significant since it requires Monte Carlo simulation campaigns to generate both the training and the test set. Moreover, since regression models cannot be extrapolated, it is necessary that the generated data extends over the complete variation range. If we consider a mature fabrication process, a huge number of Monte Carlo samples would be needed to cover a  $6\sigma$  variation range. Some techniques have been proposed to circumvent this issue. Extreme value theory is used in [38] to estimate the performance of the test in the situation where the test boundaries lie in the tails of the distribution. Other techniques such as importance sampling [39] and statistical blockade [40]–[43] rely on altering the selection likelihood of Monte Carlo samples in such a way that sampling is pushed towards the test boundaries. This way we guarantee that the model is trained with both passing and failing devices, mimicking what should be observed in the production line.

Beside the computational cost, another issue is that this simulation-based validation implicitly accepts that the Monte Carlo models provided by the foundry are accurate, even in the tails of the distributions, something that has been questioned in [44]. Generally speaking, any model-based approach is prone to non-model errors. That is, anything not included in the model is a threat to the accuracy of the methodology and can lead to unexpected errors. This holds for the Monte Carlo model, but also for any surrogate model used to speed-up simulations, models of the package, load board and the test setup in general. An interesting concept that could be a solution to this issue is that of Bayesian model fusion [45], [46]. The idea is to train the regression model on simulation data (accepting that the available simulation models may be unreliable) and then some tuning parameters of the model are dynamically adjusted from experimental data as they become available. The underlying hypothesis is that non-model errors will only slightly perturb the regression model but not its underlying structure.

Again, from an EDA point of view, it seems that systematic methodologies exist for most problems but the computational burden associated to complex AMS-RF circuit simulation is the main obstacle for fully automated approaches.

#### IV. ADAPTIVE TEST ALGORITHM

Strictly speaking, the complete production test process could end in the previous stage with the obtention of the test results. However, in the last few years, an additional step has been proposed to extend and improve the test flow by adding adaptive algorithms. The basic idea behind adaptive test algorithms is to harness the statistic information that is accumulated during the testing procedure to adapt the test program in a device-by-device basis [47]–[50]. Adapting the test program may

call for eliminating certain test that are deemed redundant, changing the order of some tests for faster detection of likely defects, moving the test limits to account for process drifts, etc. In general, for a given test procedure comprising a list of test measurements, adaptive test approaches are aimed at optimizing the sequence of test measurements. Each time that a test is executed, the algorithm takes into account the outcome of that test to select the following best test. “Best test” must be understood as the one that brings us closer to the final test decision for this particular device.

For instance, in [47] the authors estimate the joint probability density function of the measurements in the test list and use it to guide test execution towards the tests that are more likely to fail. If no test is deemed likely to fail based on previous measurements, the device is considered as a good device and the test stops. The approach in [50] is slightly different: The test list is ordered *a priori* by building a sequence of classifiers with an incremental number of test measurements. The resulting test list and classifier list are applied to each device and the test sequence is stopped if a classifier outputs a pass decision with sufficient confidence. The benefit of this “stop-on-pass” approach is that it is compatible with multi-site testing. One of the main difficulties faced by these academic proposals is the lack of actual production data to perform valid experiments in actual production conditions. Recently, the adaptive approach presented in [48] has been successfully applied to an actual production line which shows the industrial interest on the technique.

Moreover, adaptive algorithms can be also added to the other stages of the test flow. Thus, the work in [51] presents an adaptive defect filter which updates the definition of outlier taking into account process drifts, while the work in [52] proposes a generic adaptive strategy for machine learning indirect test. The circuits are tested with a machine learning indirect test but undergo a full characterization if the confidence in the test outcome is insufficient. As more data is collected, the uncertainty region shrinks.

#### V. CONCLUSIONS

Enabling mixed-signal test automation faces two key roadblocks. The first and most obvious one is the computational burden of test evaluation. Indeed, complex mixed-signal simulation are prohibitive to be introduced in optimization loops. This problem is not exclusive of mixed-signal test, but it is shared by automated design synthesis. The second challenge is to find a way to capitalize expert knowledge to provide measurement candidates for both defect filter and test signatures. Again, this problem is similar to capturing the expertise of a designer for automated design synthesis. Hopefully, future advances will benefit both domains.

#### ACKNOWLEDGMENT

This work has been partially funded by the Spanish Government project TEC2015-68448-R (co-funded by FEDER program) and by the CNRS PICS project IndieTEST PICS07703.

## REFERENCES

- [1] M. J. Barragan *et al.*, "A Fully-Digital BIST Wrapper Based on Ternary Test Stimuli for the Dynamic Test of a 40 nm CMOS 18-bit Stereo Audio  $\Sigma\Delta$  ADC," *Trans. on Circ. and Syst. I: Regular Papers*, vol. 63, no. 11, pp. 1876–1888, Nov. 2016.
- [2] S. Sunter and A. Roy, "Purely Digital BIST for Any PLL or DLL," in *European Test Symposium*, May 2007, pp. 185–192.
- [3] B. Dufort and G. W. Roberts, "On-chip analog signal generation for mixed-signal built-in self-test," *J. of Solid-State Circuits*, vol. 34, no. 3, pp. 318–330, Mar. 1999.
- [4] A. Valdes-Garcia *et al.*, "Built-in self test of RF transceiver SoCs: From signal chain to RF synthesizers," in *Radio Frequency Integrated Circuits Symposium*, 2007, pp. 335–338.
- [5] B. Karthik Vasan *et al.*, "Low-Distortion Sine Wave Generation Using a Novel Harmonic Cancellation Technique," *Trans. on Circ. and Syst. I: Regular Papers*, vol. 60, no. 5, pp. 1122–1134, May 2013.
- [6] R. A. Rutenbar *et al.*, "Hierarchical Modeling, Optimization, and Synthesis for System-Level Analog and RF Designs," *Proceedings of the IEEE*, vol. 95, no. 3, pp. 640–669, Mar. 2007.
- [7] P. N. Variyam and A. Chatterjee, "Enhancing test effectiveness for analog circuits using synthesized measurements," in *VLSI Test Symposium*, 1998, pp. 132–137.
- [8] H.-G. Stratigopoulos *et al.*, "Defect Filter for Alternate RF Test," in *European Test Symposium*, Sevilla, Spain, May 2009, pp. 101–106.
- [9] B. W. Silverman, *Density estimation for statistics and data analysis*. CRC press, 1986, vol. 26.
- [10] G. Fontana *et al.*, "A Fast Algorithm for Testability Analysis of Large Linear Time-Invariant Networks," *Trans. on Circ. and Syst. I: Regular Papers*, vol. 64, no. 6, pp. 1564–1575, Jun. 2017.
- [11] B. Esen *et al.*, "A very low cost and highly parallel DFT method for analog and mixed-signal circuits," in *European Test Symposium*, 2017.
- [12] R. Rajsuman, "Iddq testing for CMOS VLSI," *Proceedings of the IEEE*, vol. 88, no. 4, pp. 544–568, Apr. 2000.
- [13] K. Arabi and B. Kaminska, "Testing analog and mixed-signal integrated circuits using oscillation-test method," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 16, no. 7, pp. 745–753, 1997.
- [14] B. Kruseman *et al.*, "Defect Oriented Testing for Analog/Mixed-Signal Designs," *IEEE Design & Test*, vol. 29, no. 5, pp. 72–80, Oct. 2012.
- [15] J. P. Shen, W. Maly, and F. J. Ferguson, "Inductive Fault Analysis of MOS Integrated Circuits," *IEEE Design & Test*, vol. 2, no. 6, pp. 13–26, Dec. 1985.
- [16] S. Sunter *et al.*, "Practical random sampling of potential defects for analog fault simulation," in *International Test Conference*. IEEE, 2014.
- [17] B. Esen *et al.*, "Effective DC fault models and testing approach for open defects in analog circuits," in *International Test Conference*, Nov. 2016.
- [18] A. Ivanov *et al.*, "On the detectability of CMOS floating gate transistor faults," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 20, no. 1, pp. 116–128, Jan. 2001.
- [19] W. Dobbelaere, "Testing of Mixed-Signal Automotive Circuits: Do we guarantee the specs or do we catch defects?" in *European Test Symposium*, 2017.
- [20] G. Leger and A. Gines, "Likelihood-sampling adaptive fault simulation," *Int. Mixed Signals Testing Workshop*, pp. 1–6, Jul. 2017.
- [21] A. Wrixon and M. P. Kennedy, "A rigorous exposition of the LEMMA method for analog and mixed-signal testing," *Trans. on Inst. and Meas.*, vol. 48, no. 5, pp. 978–985, 1999.
- [22] J. H. Friedman, "Multivariate adaptive regression splines," *The annals of statistics*, vol. 19, no. 1, pp. 1–141, 1991.
- [23] R. Senguttuvan *et al.*, "Efficient EVM Testing of Wireless OFDM Transceivers Using Null Carriers," *Trans. on VLSI Systems*, vol. 17, no. 6, pp. 803–814, Jun. 2009.
- [24] P. N. Variyam *et al.*, "Prediction of analog performance parameters using fast transient testing," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 21, no. 3, pp. 349–361, 2002.
- [25] H.-G. Stratigopoulos and Y. Makris, "Nonlinear decision boundaries for testing analog circuits," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 24, no. 11, pp. 1760–1773, Nov. 2005.
- [26] D. Maliuk, N. Kupp, and Y. Makris, "Towards a fully stand-alone analog/RF BIST: A cost-effective implementation of a neural classifier," in *VLSI Test Symposium*, Apr. 2012, pp. 62–67.
- [27] J. D. Wichard, M. J. Ogorzalek, and C. Merkwirth, "Entool—a toolbox for ensemble modelling," in *Europhysics Conference Abstracts*, vol. 27, 2003, pp. 105–105.
- [28] M. J. Barragan *et al.*, "Alternate Test of LNAs Through Ensemble Learning of On-Chip Digital Envelope Signatures," *J. of Electronic Testing*, vol. 27, no. 3, pp. 277–288, Jan. 2011.
- [29] H. Ayari *et al.*, "Making predictive analog/RF alternate test strategy independent of training set size," in *International Test Conference*, Nov. 2012, pp. 1–9.
- [30] M. Barragan and G. Leger, "A Procedure for Alternate Test Feature Design and Selection," *IEEE Design & Test*, vol. 32, no. 1, pp. 18–25, Feb. 2015.
- [31] G. Leger and M. J. Barragan, "Brownian distance correlation-directed search: A fast feature selection technique for alternate test," *Integration, the VLSI Journal*, vol. 55, pp. 401–414, Sep. 2016.
- [32] H.-G. Stratigopoulos *et al.*, "RF Specification Test Compaction Using Learning Machines," *Trans. on VLSI Systems*, 2009.
- [33] M. J. Barragan and G. Leger, "Efficient selection of signatures for analog/RF alternate test," in *European Test Symposium*, 2013.
- [34] A. Gomez-Pau, L. Balado, and J. Figueras, "Efficient Production Binning Using Octree Tessellation in the Alternate Measurements Space," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 35, no. 8, pp. 1386–1395, 2016.
- [35] H. Peng *et al.*, "Feature selection based on mutual information criteria of max-dependency, max-relevance, and min-redundancy," *Trans. on Pattern Analysis and Machine Intelligence*, vol. 27, no. 8, pp. 1226–1238, Aug. 2005.
- [36] H. Ayari *et al.*, "Smart selection of indirect parameters for DC-based alternate RF IC testing," in *VLSI Test Symposium*, 2012, pp. 19–24.
- [37] S. Laguech *et al.*, "Efficiency evaluation of analog/RF alternate test: Comparative study of indirect measurement selection strategies," *Microelectronics Journal*, vol. 46, no. 11, pp. 1091–1102, Nov. 2015.
- [38] H. Stratigopoulos, "Test Metrics Model for Analog Test Development," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 31, no. 7, pp. 1116–1128, 2012.
- [39] E. Yilmaz and S. Ozev, "Adaptive-Learning-Based Importance Sampling for Analog Circuit DPPM Estimation," *IEEE Design & Test*, vol. 32, no. 1, pp. 36–43, Feb. 2015.
- [40] A. Singhee and R. Rutenbar, "Statistical Blockade: Very Fast Statistical Simulation and Modeling of Rare Circuit Events and Its Application to Memory Design," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 28, no. 8, pp. 1176–1189, Aug. 2009.
- [41] H.-G. Stratigopoulos and S. Sunter, "Fast Monte Carlo-Based Estimation of Analog Parametric Test Metrics," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 33, no. 12, pp. 1977–1990, Dec. 2014.
- [42] H. G. Stratigopoulos *et al.*, "Evaluation of low-cost mixed-signal test techniques for circuits with long simulation times," in *International Test Conference*, Oct. 2015, pp. 1–7.
- [43] M. Barragan *et al.*, "Practical Simulation Flow for Evaluating Analog and Mixed-Signal Test Techniques," *IEEE Design & Test*, vol. PP, no. 99, pp. 1–1, 2016.
- [44] G. Leger and M. J. Barragan, "Questioning the reliability of Monte Carlo simulation for machine learning test validation," in *European Test Symposium*, May 2016, pp. 1–6.
- [45] F. Wang *et al.*, "Bayesian model fusion: Large-scale performance modeling of analog and mixed-signal circuits by reusing early-stage data," *Trans. on Computer-Aided Design of Int. Circ. and Syst.*, vol. 35, no. 8, pp. 1255–1268, 2016.
- [46] J. Liaperdos *et al.*, "Fast deployment of alternate analog test using bayesian model fusion," in *Design, Automation & Test in Europe*, 2015, pp. 1030–1035.
- [47] E. Yilmaz *et al.*, "Per-Device Adaptive Test for Analog/RF Circuits Using Entropy-Based Process Monitoring," *Trans. on VLSI Systems*, vol. 21, no. 6, pp. 1116–1128, Jun. 2013.
- [48] H. G. Stratigopoulos and C. Streitwieser, "Adaptive test flow for mixed-signal ICs," in *VLSI Test Symposium*, Apr. 2017, pp. 1–6.
- [49] A. Zjajo, M. J. Barragan, and J. P. d. Gyvez, "Low-Power Die-Level Process Variation and Temperature Monitors for Yield Analysis and Optimization in Deep-Submicron CMOS," *IEEE Trans. on Inst. and Meas.*, vol. 61, no. 8, pp. 2212–2221, Aug. 2012.
- [50] G. Leger, "Combining adaptive alternate test and multi-site," in *Design, Automation & Test in Europe*, 2015, pp. 1389–1394.
- [51] E. Yilmaz *et al.*, "Adaptive multidimensional outlier analysis for analog and mixed signal circuits," in *International Test Conference*, Sep. 2011.
- [52] H. Stratigopoulos and S. Mir, "Adaptive Alternate Analog Test," *IEEE Design & Test*, vol. 29, no. 4, pp. 71–79, 2012.