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# Reduced-code static linearity test of split-capacitor SAR ADCs using an embedded incremental $\Sigma\Delta$ converter

Renato S. Feitoza, *Student Member, IEEE*, Manuel J. Barragan, *Member, IEEE*, Daniel Dzahini, *Member, IEEE*, and Salvador Mir, *Member IEEE*

**Abstract**—Reduced-code techniques for ADC static linearity test have the potential to drastically reduce the number of necessary measurements for a complete static linearity characterization. These techniques take advantage of the repetitive operation of certain families of converters such as pipelines, SARs, cyclic, etc. In this paper we present a novel reduced-code technique for the static linearity test of split-capacitor SAR ADCs based on the on-chip generation and measurement of the major carrier transitions of the input DAC of the converter. The proposed test method does not require a test stimulus, and we show that the necessary measurements can be easily extracted by reconfiguring portions of the SAR into a low-resolution Incremental  $\Sigma\Delta$  converter. The proposed technique is validated with both behavioral and electrical simulations of a 10-bit SAR ADC in a 65 nm CMOS technology.

**Index Terms**—Analog-to-Digital Conversion; Design-for-Test; Static Linearity Test; Reduced-code testing.

## I. INTRODUCTION

**D**UE to CMOS technology scaling, Successive-Approximation Register Analog-to-Digital Converters (SAR ADCs) have paved their way back to the spotlight of both academic and industrial efforts. One of the main reasons for that is their ability to go on sleep mode and its overall energy efficiency, that are crucial in several emerging applications [1]. Additionally, since the architecture of a SAR ADC relies on few analog blocks in comparison to other architectures, it is known to be a digital-friendly topology, and hence the advantages of scaling are leveraged very efficiently.

In that context, the split-capacitor SAR (SC-SAR) ADC has been shown to provide an even better compromise in terms of area, power consumption and speed. The major contributor to the area of a capacitor-based SAR ADC is the Capacitive Digital-to-Analog Converter (CDAC) that is used for approximating the analog input samples of the SAR ADC. Due to the fact that a split capacitor SAR uses two (or more) CDAC arrays separated by bridge capacitors rather than just one binary-weighted CDAC, the area occupied by the capacitors is greatly reduced [2]. Yet, capacitor-based SAR ADCs are very prone to static errors, and the main source of these errors are the mismatches in the DAC capacitive

array. Moreover, it has been shown that this issue is even more critical for split-capacitor SC-SAR ADCs due to the parasitic capacitances of the bridge attenuation capacitors [3]. Static linearity tests are then necessary in order to assure the correct functionality of the converter. However, static test can be a very demanding and costly task. Indeed, the mixed-signal sections of a complex System-on-Chip (SoC) are amongst the more critical in terms of test time [4], and to complicate things even more, relative test cost is increased with further technology scaling. Focusing specifically on ADC/DAC testing, the paramount issues are the need of an accurate and linear test stimulus and the huge volume of samples that have to be collected in order to perform an accurate measurement. The standard in industry is the histogram test method, in which the whole set of codes available on the ADC/DAC is measured [5]. This leads to a number of samples that scales exponentially with the resolution of the ADC/DAC. In order to average noise each code has to be measured a few times, which further increases the total test time. The development of techniques to reduce test time is a critical task, since they enable not only speeding-up and reducing test cost, but they also open the door to enhanced reliability during the lifetime of the circuit.

In recent years, the development of the so-called reduced-code techniques have been drawing attention due to the potential to yield large reductions in test time. They rely on the repetitive operation of some ADC topologies, where errors across the ADC transfer function are caused by a reduced set of components. This allows inferring the complete transfer function of the ADC by measuring only a carefully selected subset of the total set of codes, greatly reducing the global test time. Moreover, the inherent simplification of static linearity tests provided by reduced-code techniques may open the door to a full built-in self-test (BIST) implementation. This way, tester requirements can be relaxed and test cost may be further contained by moving static linearity test resources to the device under test itself. Furthermore, BIST techniques may enable on-line test, self-healing, self-calibration and adaptive operation in safety-critical and mission-critical applications. Indeed, reliability and quality enhancement is becoming one of the main drivers for the development of analog and mixed-signal BIST. For instance, in safety-critical applications, such as automotive, mixed-signal BIST is even becoming a design requirement in many integrated systems.

In this direction, the work in [6] estimates the full non-linearity characteristic of a SAR converter by measuring a

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smaller set of codes through the application of a piecewise linear ramp on the ADC input. The main problem with that approach is that the generation of this type of excitation may be challenging. Another limitation is that missing codes may not be detected. Examples of reduced-code techniques for pipeline ADCs can be found in [7] and [8], while a model-based reduced-code strategy is proposed in [9]. In [10], a bit weight extraction based on the measurement of the Major Carrier Transitions (MCTs) of the CDAC is proposed. The MCTs are generated using a modified SAR operation and measured using an auxiliary CDAC for test, similarly to the approach of self-calibration proposed in [11]. However, that approach is only convenient for sub-radix calibration applications since the value of the unit capacitor has to be changed, unbalancing the weights of the CDAC. This technique is also very susceptible to the capacitor mismatch in the auxiliary CDAC.

For SC-SAR ADCs, the focus in the existing literature has been more on the calibration of the capacitive mismatches than in characterizing the static non-linearity of the converter. In works such as [3], [12], [13], a tunable capacitor is added in parallel with the LSB array to compensate for the mismatches, but no static linearity information is explicitly extracted. In [2], a differential SC-SAR ADC is tested in such a way that one branch is responsible for the measurement of the adjacent branch. There, only the MSB capacitors are characterized. The main advantage of this approach is that no extra analog circuitry is needed to perform the measurements. Similarly, in [14] one sub-array is responsible for the bit weight extraction of the other. The main disadvantage of this kind of approach is that since they require several iterative operations in order to converge, they are relatively slower than algorithms such as [6], [10].

This manuscript is an extension of our previous work in [15]. In this manuscript we propose a novel reduced-code technique for the measurement of the static linearity of a split-capacitor SAR ADC through the exploration of the properties of the MCTs of each of its partial CDACs.

The proposed methodology does not require the application of a test stimulus, since we use the split-capacitor DAC array for generating the set of codes of interest. The width of these codes are measured using an on-chip incremental  $\Sigma\Delta$  ADC ( $I\Sigma\Delta$ ) for test. In this paper we explore the trade-offs for a correct sizing of the  $I\Sigma\Delta$  and explore the co-design of both the SAR ADC under test and the  $I\Sigma\Delta$  converter by reusing the input capacitive array during the test phase.

The rest of this manuscript is organized as follows: section II reviews the basic concepts of SC-SAR ADCs and MCT theory, and presents the proposed static test strategy. Section III explores the design trade-offs for a practical implementation of the proposed reduced-code test. In Section IV we validate the feasibility of the proposed reduced-code static linearity test by electrical simulation of a 10-bit SAR ADC in a 65 nm CMOS technology. Finally, section V summarizes the main contributions of this work.

## II. THEORETICAL BASIS: SC-SAR ADC OPERATION AND MCT TESTING

### A. Introduction to SC-SAR ADC operation

The SC-SAR ADC architecture is shown in Fig. 1. It consists of a SC-DAC, one comparator and the control logic. Its operation relies on a binary search. The SC-DAC consists of an  $L$ -bit LSB array and an  $M$ -bit MSB array bridged by an attenuation capacitor  $C_{atten}$ . This attenuation capacitor is responsible for the savings obtained in area and power consumption with respect to a binary weighted SAR ADC. The value of  $C_{atten}$  is chosen in a way that the equivalent capacitance seen by the MSB array is the dummy capacitor  $C_u$ , where  $C_u$  is the unit capacitance. Each capacitor is weighted as  $C_i = 2^i C_u$ , where  $i$  ranges from 0 to  $M - 1$  for the MSB array and from 0 to  $L - 1$  for the LSB array. It can be shown that the value of  $C_{atten}$  is determined by  $C_{atten} = C_u \left( \frac{2^L}{2^L - 1} \right)$ .

The operation of the SC-SAR ADC can be described as follows. First, the input voltage  $V_{in}$  is sampled through the sampling switches ( $S_{samp} = 1$ ) in a way that the charge in the capacitors is given by  $Q_i = -C_{tot,i} V_{in}$ , where  $i = L$  for the LSB array,  $i = M$  for the MSB array,  $C_{tot,L} = 2^L C_u$ , and  $C_{tot,M} = (2^M - 1) C_u$ . After the sampling phase,  $S_{samp}$  is opened and the bottom plates of the capacitors are connected to ground, in a way that  $V_A = V_X = -V_{in}$ , where  $V_A$  and  $V_X$  are the top plate voltage for the LSB and MSB arrays, respectively. Then, the MSB capacitor is connected to the ADC full-scale (FS) reference voltage,  $V_{ref}$ , starting the conversion phase, and voltage  $V_X$  changes by  $V_X = -V_{in} + V_{ref} \frac{C_{M-1}}{C_{tot,M} + C_{eq,LSB}} = -V_{in} + \frac{1}{2} V_{ref}$ , where  $C_{eq,LSB}$  is the equivalent capacitor seen by the MSB array, given by the series equivalent between  $C_{atten}$  and  $C_{tot,L}$ . The resulting voltage goes into the comparator and if  $V_X > 0$ , the MSB switch is opened and the output bit is set to 0. Otherwise, the corresponding output bit is set to 1 and the MSB switch is kept closed. This is repeated for each capacitor on the MSB array. After exercising the least significant capacitor of the MSB array,  $V_X$  is given by  $V_X = -V_{in} + V_{ref} \sum_{i=0}^{M-1} D_i \frac{C_i}{C_{tot,M} + C_{eq,LSB}}$ , where the MSB segment of the output binary word is  $D_{M-1} \dots D_1 D_0$ . The same process is then performed for the capacitors on the LSB array, where the scaling caused by the capacitive voltage divider between LSB capacitors and series equivalent between  $C_{atten}$  and  $C_{tot,M}$  yields a scaling equivalent to the classical binary weights.

### B. Major Carrier Transitions in a capacitive DAC

By definition, the Major Carrier Transition of an  $N$ -bit DAC is the transition for which the MSB first goes to a logic 1, i.e. the transition from 011...111 to 100...000. This transition is particularly important because it is where the worst case DNL/INL is usually found. By extension, we can also define  $N$  MCTs in an  $N$ -bit DAC, where the  $i$ -th MCT is defined as the transition where the  $i$ -th bit first goes to 1 [16], i.e. the transition from code  $2^i - 1$  to code  $2^i$ .

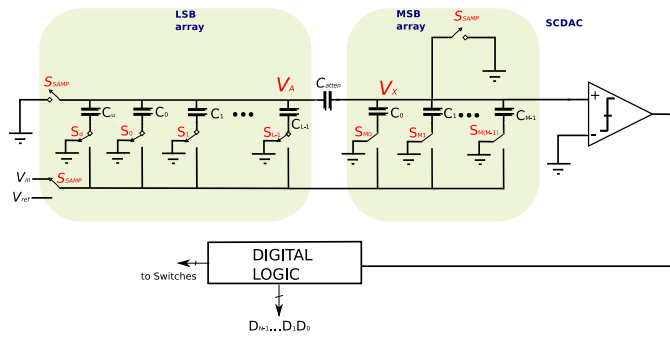


Fig. 1. SC-SAR ADC simplified block diagram.

Neglecting the offset voltage, the output voltage  $V_{DAC}$  of a binary-weighted CDAC can be written as

$$V_{DAC}[D_{N-1}...D_0] = D_{N-1}W_{N-1} + \dots + D_1W_1 + D_0W_0, \quad (1)$$

where the weights  $W_i$  are determined by the CDAC capacitor ratios and the input binary code is  $D_{N-1}D_{N-2}...D_0$ . Note that by performing only  $N$  measurements –where  $N$  is the resolution of the CDAC under measurement– it would be possible to reconstruct its full transfer function. The most direct approach to achieve that is by setting  $D_i = 1$  and all the remaining bits to 0, and calculating  $W_i$  for  $i = 0, \dots, N - 1$ . Alternatively, it is also possible to measure the code widths associated to the MCTs of the CDAC by measuring the voltage difference  $V_i$  between codes  $2^i$  and  $2^i - 1$ . Then, the values of  $W_i$  can be computed by simple manipulation of equation (1), as detailed in [16]. This alternative measurement strategy has the advantage that the code widths are expected to be relatively constant, which allows to adjust the FS of the measurement instrument for an accurate characterization. On the other hand, the direct measurement of the weights  $W_i$  would demand measurements in the range from a few LSBs to half the full scale with a precision below the LSB, which may be challenging.

To help illustrate the measurement strategy based on measuring the code widths associated to the MCTs, let us consider a simple 4-bit CDAC and let us focus on a given MCT, for example the second MCT code width ( $i = 2$ ). In that case, according to equation (1),  $V_{DAC}[2^2] = V_{DAC}[0100] = W_2$  and  $V_{DAC}[2^2 - 1] = V_{DAC}[0011] = W_1 + W_0$ , which means that  $V_2 = V_{DAC}[0100] - V_{DAC}[0011] = W_2 - W_1 - W_0$ . Now, considering  $V_{DAC}[1100] = W_3 + W_2$  and  $V_{DAC}[1011] = W_3 + W_1 + W_0$ , the difference  $V_{DAC}[1100] - V_{DAC}[1011] = W_2 - W_1 - W_0$  is also equal to  $V_2$ , since the effect of  $W_3$  is canceled. As a conclusion, after all the respective transitions are mapped, it is possible to measure only the code widths of the  $N$  MCTs and extrapolate it to the full transfer curve of the DAC.

### C. Reduced-code linearity testing of SC-SAR ADCs by measuring partial MCT widths

The static linearity of an ADC is usually characterized in terms of its DNL, INL, offset and gain errors [5]. Since a SAR ADC only uses one comparator (i.e. this assumption should not be valid for time interleaved SAR ADCs), it is reasonable

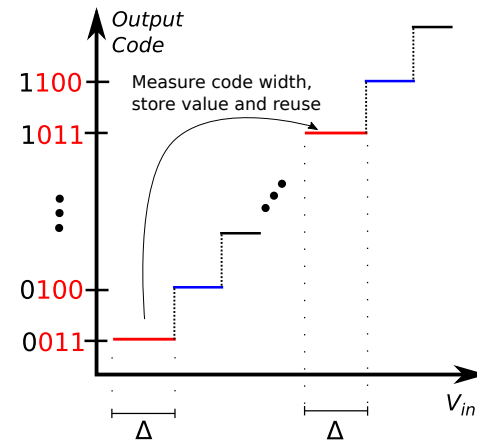


Fig. 2. Reduced-code testing of SC-SAR ADC by measuring MCT code widths.

to assume that offset and gain errors can be easily corrected. Hence, assuming that the dominant linearity error source for this ADC topology is capacitor mismatch in the CDAC array, the ADC linearity can be inferred by measuring the code widths associated to each MCT in the CDAC array, drastically reducing the total test time. It has to be noted that second-order effects such as dynamic offset and non-linear input capacitance at the comparator are usually below the mismatch error in the CDAC, so they do not play a significant role in the linearity of the SAR ADC.

For instance, if we go back to the previous 4-bit CDAC example above, in a SAR ADC built with such an array the width of code 0011 should be the same as the width of code 1011. As it is conceptually represented in Fig. 2, we only require one measurement for characterizing the widths of these two codes.

The described reduced-code strategy is the base of the work in [10], [15], where MCT-based measurements are proposed for binary-weighted SAR ADCs. In this section we extend this strategy to cope also with generic  $M \times L$  split-capacitor arrays. The proposed test strategy is conceptually depicted in Fig. 3. Firstly, the MCTs of each partial CDAC are measured independently. Two test switches, labelled  $S_A$  and  $S_X$ , have been added to the SC-SAR ADC under test in order to connect the top plate of the LSB and MSB segments of the capacitor array to an embedded test instrument (conceptually represented as a voltmeter) that captures and digitizes the partial MCTs. Then, by digital post-processing of the measurement we can infer the full static characteristic, including INL, DNL and detection of missing codes in the SC-SAR ADC under test. It is important to note that even though the partial CDACs are being measured separately, the mismatches of the adjacent CDAC and bridge capacitor are taken into account because their equivalent capacitance has influence on the linearity of each CDAC segment.

Let us detail the complete test strategy for a generic  $M \times L$  SC-SAR ADC. Firstly we characterize the  $M$ -bit MSB segment in the following way: initially, switches  $S_X$  and  $S_A$  are opened, and the bottom of the  $i$ -th capacitor in the MSB array is connected to  $V_{ref}$  while all the remaining capacitors are connected to ground. In this first phase,  $S_{samp} = 1$ ,

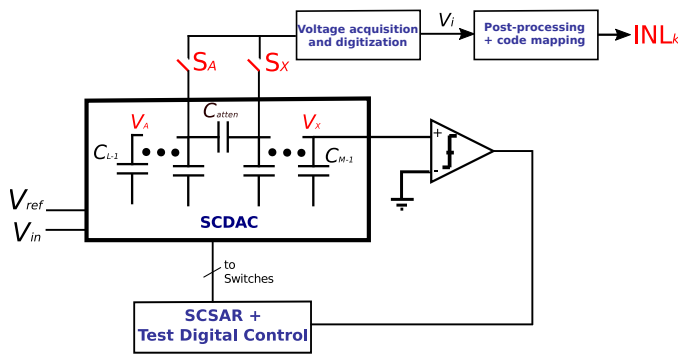


Fig. 3. Conceptual block diagram of the proposed on-chip reduced-code linearity test setup.

which means that all other capacitors are grounded and the  $i$ -th capacitor is pre-charged to  $Q_i = -V_{ref}C_i$ . Then, in the next clock cycle, the  $i$ -th capacitor is switched to ground and all capacitors of the MSB array from  $i - 1$  to  $0$  are connected to  $V_{ref}$ . By charge conservation, it can be shown that after performing this operation, in an ideal SC-SAR ADC voltage  $V_X$  evolves to  $V_X \approx \Delta_X$ , where  $\Delta_X = V_{ref}/2^M$  is the ideal step of the MSB segment of the DAC array. Voltage  $V_X$  is fed to the embedded acquisition instrument through  $S_X$  and it is subsequently digitized and stored for post-processing. The process is repeated for each of the  $M$  capacitors in the MSB array.

The methodology is similar for the  $L$ -bit LSB segment of the DAC array. The bottom of the  $j$ -th capacitor in the LSB array is first connected to  $V_{ref}$  and all remaining capacitors to ground. In the following clock cycle the  $j$ -th capacitor is switched to ground and capacitors  $j - 1$  to  $0$  are connected to  $V_{ref}$ . Again, by charge conservation it can be shown that voltage  $V_A$  in an ideal SC-SAR ADC is given by

$$V_A \approx \Delta_A = V_{ref} \frac{C_u}{2^L C_u + \frac{C_{atten} C_{tot,M}}{C_{atten} + C_{tot,M}}} \approx \frac{V_{ref}}{2^L + 1}, \quad (2)$$

Again, this voltage is fed to the embedded acquisition instrument via the  $S_A$  switch and it is digitized and stored for further post-processing. The process is repeated for each of the  $L$  capacitors in the array.

Once that both segments of the DAC array have been characterized as described above, the obtained digitized measurements represent the width of the codes associated to the MCTs of the MSB and LSB segments of the SC-DAC, that we will denote as  $\ell_i^{MSB}$  and  $\ell_j^{LSB}$ , respectively, with  $i = 0, \dots, M - 1$  and  $j = 0, \dots, L - 1$ . The partial weights of the MSB and LSB segments of the SC-DAC can be easily computed from  $\ell_i^{MSB}$  and  $\ell_j^{LSB}$  as described in [15]. However, to estimate the static linearity of the complete SC-SAR ADC they should be appropriately combined.

First, after the inductive calculations, one matrix containing the normalized weights of the LSB segment is obtained, namely  $\hat{\mathbf{W}}_{LSB} = [\hat{W}_{LSB}^0, \dots, \hat{W}_{LSB}^{L-1}]$ , and another consisting of the relative normalized weights of the MSB segment, that is  $\hat{\mathbf{W}}'_{MSB} = [\hat{W}'_{MSB}^0, \dots, \hat{W}'_{MSB}^{M-1}]$ . Considering the weight scaling between the two CDAC segments, the normalized

weights of the MSB segment are given by

$$\hat{\mathbf{W}}_{MSB} = 2^L \hat{\mathbf{W}}'_{MSB}. \quad (3)$$

After that step, the two matrices  $\hat{\mathbf{W}}_{MSB}$  and  $\hat{\mathbf{W}}_{LSB}$  are concatenated, giving as a result the normalized weights matrix of the SC-SAR ADC  $\hat{\mathbf{W}} = [\hat{W}_0, \dots, \hat{W}_{N-1}]$ . Finally, the normalized weights can be converted to the actual voltage weights

$$\mathbf{W} = \frac{V_{ref}}{2^N} \hat{\mathbf{W}}. \quad (4)$$

Considering the previous definitions of MCT and its associated code width, it is important to observe that each element in  $\mathbf{W}$  corresponds to a digital representation of  $W_i$  in equation (1). That means that the actual binary weights of an  $N$ -bit ADC have been obtained by measuring the partial CDACs. Thus, one can now define a “digital” MCT code width  $\tilde{V}_i$  by using the same relationship used for the analog domain, applying it on the elements of  $\mathbf{W}$

$$\tilde{V}_0 = W_0, \quad (5)$$

$$\tilde{V}_i = W_i - \sum_{j=1}^{i-1} W_j \quad i = 1, \dots, N - 1. \quad (6)$$

Besides, it is important to notice that the ideal values of  $\tilde{V}_i$  are positive, since they correspond to the code width of each MCT. If they happen to be negative, that means that there are missing codes, since a zero or negative step length should correspond to a code that does not exist. It can be shown that the number of missing codes corresponds to the number of times  $V_{LSB}$  can be added to  $\tilde{V}_i$  before the voltage is larger than  $0$ , where  $V_{LSB} = V_{ref}/2^N$  is the LSB step of the full SC-SAR ADC.

After the estimation of the missing codes, the obtained code widths are mapped to the full  $2^N$  codes of the SC-SAR ADC following the guidelines in [15] in order to obtain the code widths  $\tilde{L}_k$ , for  $k = 1, \dots, 2^N - 2$ . Finally, the DNL and INL can be calculated by

$$DNL_k = \tilde{L}_k - 1, \quad (7)$$

$$INL_k = \sum_{j=1}^k DNL_j, \quad (8)$$

for  $k = 1, \dots, 2^N - 2$ . It is important to remark that  $INL_k$  may be severely affected by the accumulation of quantization errors in the estimation of  $DNL_k$ . However, since the accumulation of this error is linear, it can be easily corrected using well-known best-fit techniques [15], [17] to subtract the error contribution.

### III. PRACTICAL ON-CHIP IMPLEMENTATION

The proposed reduced-code static test strategy has the advantage of not requiring a test stimulus. This greatly simplifies the on-chip implementation of the technique and opens the door to an efficient full-BIST approach. The key element for the on-chip implementation of the proposed technique is the embedded test instrument that acquires and digitizes the partial MCTs. In this manuscript we will show that a suitable candidate for performing this task is the  $\text{I}\Sigma\Delta$  ADC, which,

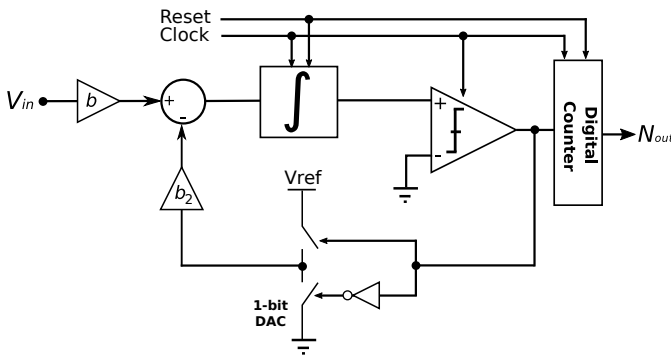


Fig. 4. Conceptual block diagram of an Incremental  $\Sigma\Delta$  ADC.

conceptually, is a mix between a dual-slope and a  $\Sigma\Delta$  ADC [18]. This topology is suited for measuring DC voltages such as in digital voltmeters and instrumentation and measurement applications. On the other hand, oversampling  $\Sigma\Delta$  ADCs are more prone to gain and offset errors, and it has been proved that the incremental  $\Sigma\Delta$  modulation is inherently more robust to complex non-linear effects such as idle tone generation and dead zones [19]. In addition, well-known digital test solutions for  $\Sigma\Delta$  modulators can be adapted for assuring the correct functionality of the added test circuitry [20], [21]. In the remainder of this section, the basic operation of an  $\Sigma\Delta$  ADC is explained and the design trade-offs for sizing the proposed circuitry are explored. Moreover, we will show that we can merge the CDAC of the SC-SAR ADC under test with the input stage of an  $\Sigma\Delta$  ADC by using the same operation principle of a multiplying DAC (MDAC) [22], which further reduces the overhead and simplifies the implementation.

#### A. Incremental $\Sigma\Delta$ ADC for reduced-code testing

Fig. 4 shows a conceptual block diagram of a first-order  $\Sigma\Delta$  ADC. The operation of the  $\Sigma\Delta$  ADC differs from a  $\Sigma\Delta$  in which both integrator and counter are reset at the beginning of each conversion. Thus, for a given resolution  $R$ , the integration of each input sample is performed for  $2^R$  cycles. The output of the comparator is triggered every time the integrator output crosses 0, incrementing the counter and sending a logic 1 via the feedback path to be subtracted from the converter input. After  $2^R$  cycles, it can be shown that [18]

$$N_{out} = 2^R \left( \frac{bV_{in}}{b_2V_{ref}} \right) + \epsilon, \quad (9)$$

where  $b$  and  $b_2$  represent the integrator input and feedback gains, respectively, and  $|\epsilon| \leq 1$ . Note that since the number of counts is acquired by a simple digital counter, this result is already a quantized representation of the input.

Let us consider the operation of the proposed reduced-code test technique, as depicted in Fig. 3, using a first-order  $\Sigma\Delta$  ADC for acquiring and digitizing each MCT measurement. It can be shown by developing equation (9) that the digital code length representations in LSBs of each partial CDAC are given by

$$\ell_i^{MSB} \approx 2^{M-R} \frac{b_2}{b_X} N_{out,i}, \quad (10)$$

$$\ell_j^{LSB} \approx \frac{(2^L + 1)}{2^R} \frac{b_2}{b_A} N_{out,j}. \quad (11)$$

where  $b_X$  and  $b_A$  represent the input gain of the  $\Sigma\Delta$  ADC when the system is configured for measuring the MSB and LSB segments of the CDAC array, respectively. Notice that these input gains do not have to be equal, which, as it will be shown later in this paper may have important implications for simplifying the implementation.

#### B. System-level design trade-offs

In order to provide some design guidelines for the implementation of the  $\Sigma\Delta$  ADC in the context of the proposed reduced-code static linearity test application, this subsection explores the trade-offs between the accuracy in the estimation of static linearity performances and the resolution and full scale of the  $\Sigma\Delta$  ADC for test. These trade-offs are explored based on behavioral simulations performed in Matlab. Realistic behavioral models of the test setup in Figs. 3 and 4 have been developed following the guidelines in [23].

The first relevant aspect to take into consideration is the measurement accuracy as a function of the full-scale range of the  $\Sigma\Delta$  ADC for test. In this line, in order to simplify the interpretation of the results, we normalized the full scale of the  $\Sigma\Delta$  for the MSB measurement configuration,  $FS_{\Sigma\Delta}^{MSB} = (b_2/b_X)V_{ref}$  to the FS of the SC-DAC (i.e.,  $V_{ref}$ ).

Fig. 5a plots the average INL estimation error as a function of  $FS_{\Sigma\Delta}^{MSB}$  using the proposed test methodology for different SAR ADC resolutions,  $N$ . The results are obtained by calculating the average test error of 250 randomly generated SC-SAR ADC samples with capacitor mismatch standard deviation  $\sigma = 0.1\%$  and  $R = 10$ . It can be observed that the curve presents a zone with high measurement errors in the lateral extremities of its horizontal axis, and a range of small errors around its center. Not surprisingly, higher SC-SAR ADC resolutions yields higher estimation errors. Again, it is important to stress that each scenario demands only  $N$  measurements for deriving the full INL characteristic.

On the other hand, Fig. 5b shows the INL estimation error as a function of  $FS_{\Sigma\Delta}^{MSB}$  for different values of the  $\Sigma\Delta$  resolution,  $R$ . The resolution of the SC-SAR ADC is fixed to  $N = 10$  bits ( $M = 6$  and  $L = 4$ ) for this experiment. It can be observed that there is an optimal range for  $FS_{\Sigma\Delta}^{MSB}$ , like the previous case. Nonetheless, for this case there is no significant dependence with  $R$  for low values of  $FS_{\Sigma\Delta}^{MSB}$ . This is due to the fact that the output of the integrator saturates, which means that taking more samples does not affect the operation of the circuit [15]. It can also be observed that in the optimal range, the error is smaller for higher values of  $R$ . However, since the test time is given by  $3N2^R/f_s$ , where  $f_s$  is the clock frequency, it is important to pay attention to the existing trade-off between error and test time, since the latter increases exponentially with  $R$ . In this line, Fig. 6 illustrates the total percentage of time saved in comparison to the standard Linear Histogram Test (LHT) with 128 hits per code for different values of  $N$ . As it can be observed, high savings in test time can be obtained. Looking at Fig. 5b, it can be seen that relatively small errors can be obtained for some

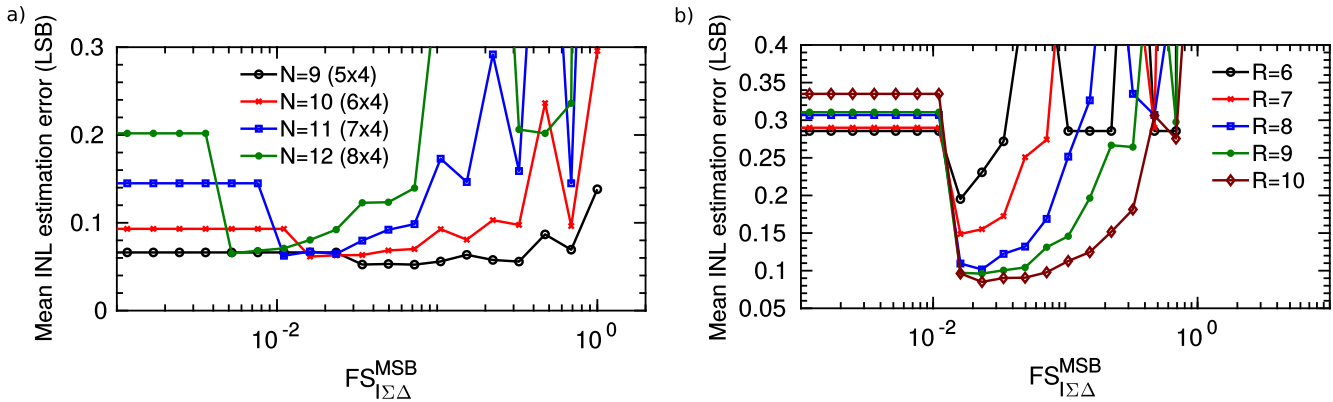


Fig. 5. INL measurement error as a function of  $FS_{I\Sigma\Delta}^{MSB}$  ( $\sigma = 0.1\%$ ) for a) different SAR resolutions ( $R = 10$ ) and b) different resolutions of the  $I\Sigma\Delta$  ADC ( $N = 10$ ,  $(6 \times 4)$ ).

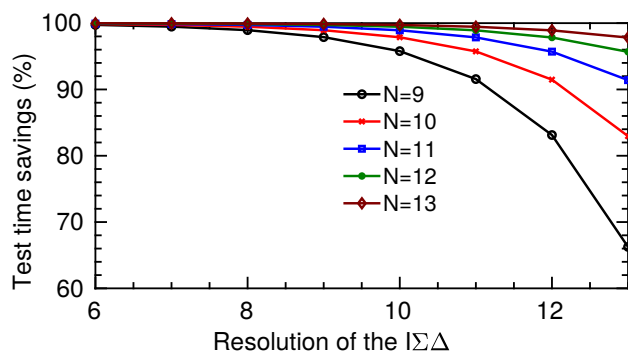


Fig. 6. Percentage of test time saved in comparison to 128 hits per code LHT for different SC-SAR ADC and  $I\Sigma\Delta$  ADC resolutions.

values of  $FS_{I\Sigma\Delta}^{MSB}$  even for modest values of  $R$ . For instance, less than 0.09 LSB error can be obtained for a 10-bit  $I\Sigma\Delta$  ADC measuring a 10-bit SC-SAR ADC with less than 3% of total standard LHT time.

In order to appropriately size the full scale of the  $I\Sigma\Delta$  for an accurate reduced code test, we can relate the obtained results to the magnitude of the intended measurements. Thus, the magnitude of the  $I\Sigma\Delta$  ADC input, that is the code width of the partial MCTs, would be in the order of magnitude of the LSB of the partial arrays in the SC-DAC. Actually, if we denote as  $\sigma$  the standard mismatch deviation of the unit capacitor in the SC-DAC, we can provide a simple guideline for designing the value of the  $I\Sigma\Delta$  full scale close to the optimum region by making

$$FS_{I\Sigma\Delta}^{MSB} = \xi A_{max} \quad (12)$$

where  $A_{max} \approx \frac{V_{ref}}{2^M} (1 + 3\sigma\sqrt{2^M - 1})$  is an estimation of the maximum variability of the MCT values and  $\xi$  is a scaling factor ( $\xi > 1$ ) for providing an extra design margin to account for additional error sources.

To further explore this design guideline, Fig. 7 shows boxplots for the INL estimation error of a 10-bit SC-SAR ADC ( $M = 6$ ,  $L = 4$ ) as a function of the expected capacitor mismatch level in the capacitors, ranging from  $\sigma = 0.1\%$

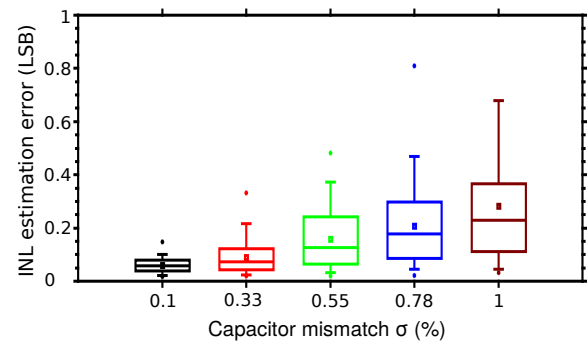


Fig. 7. INL error as a function of the capacitor mismatch standard deviation. 200 iterations for each value of  $\sigma$ ,  $R = 10$ ,  $M = 6$ ,  $L = 4$ .

to  $\sigma = 1\%$ . The resolution of the  $I\Sigma\Delta$  ADC used in this simulation is  $R = 9$  bits. For each iteration, the values of  $FS_{I\Sigma\Delta}^{MSB}$  are chosen using  $FS_{I\Sigma\Delta}^{MSB} = \xi A_{max}$ , with  $\xi = 1.25$ . The number of iterations for each  $\sigma$  value was 200. It can be observed that the proposed full scale sizing strategy yields good results, with smaller measurement errors for smaller values of  $\sigma$ , as it would be expected. It also has to be noted that large mismatch levels, e.g.,  $\sigma = 1\%$ , lead to large INL values in the SAR ADC, so even if the estimation error may seem large, the relative error may still be contained.

### C. Merging of the SC-DAC with $I\Sigma\Delta$

The input stage of a first-order  $I\Sigma\Delta$  ADC consists of an integrator, as it is shown in Fig. 4. In a classical switched-capacitor implementation, the input voltage is sampled into a sampling capacitor  $C_s$ , and then delivered through the virtual ground to a feedback capacitor  $C_f$ . While this capacitor is not reset, if we denote by  $V_s$  the voltage sampled in  $C_s$ , the integrator output voltage increments by  $-(C_s/C_f)V_s$  after each clock cycle. In this work we propose to perform the sampling differently, by building capacitor  $C_s$  using each partial CDAC. This way, the sampling stage is performed by the CDAC MCT voltage generation, and subsequently this voltage is transferred through the capacitor  $C_f$ , applying a principle similar to an MDAC in a pipelined ADC [22]. The

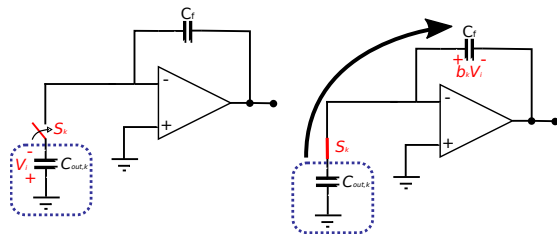


Fig. 8. Conceptual operation of merging between CDAC and IΣΔ ADC: first, MCT step length  $V_i$  is generated. Then, charge in  $C_{out,k}$  is transferred to  $C_f$  via  $S_k$ , integrating  $V_i$  with gain  $b_k$ .

main advantages of this approach are that, first, transferring charge in this manner eliminates the need of a high-impedance buffer between the CDAC and the input of the IΣΔ ADC. Second, reusing the CDAC as the sampling capacitor in the IΣΔ significantly reduces the area overhead of the proposed solution. Third, as it will be shown subsequently, we have the additional advantage of scaling the FS of the IΣΔ ADC in order to compensate for the expected change in magnitude of the MCT voltages for each partial CDAC.

The proposed configuration is conceptually shown in Fig. 8. Voltage  $V_i$  corresponds to the target MCT to be measured, generated as described in Section II.C. After  $S_k$  ( $k = A$  for the LSB segment,  $k = X$  for the MSB segment) is connected, the charge stored in the CDAC is transferred to  $C_f$  in a way that the output is incremented by  $\approx -V_i \times C_{tot,k}/C_f = b_k V_i$ , where  $b_k = -C_{tot,k}/C_f$  is the integrator gain.

Taking into consideration the guidelines for sizing of  $FS_{I\Sigma\Delta}^{MSB}$  derived in the previous subsection, we can size the capacitors in the integrator. By using the definition of  $FS_{I\Sigma\Delta}^{MSB}$  together with the definition of  $A_{max}$ , it follows that

$$FS_{I\Sigma\Delta}^{MSB} = \frac{b_2}{b_X} V_{ref} = \frac{b_2 C_f}{C_{out,MSB}} V_{ref} = \xi A_{max}, \quad (13)$$

where the output capacitance of the MSB array is  $C_{out,MSB} \approx 2^M C_u$ , with  $C_u$  being the unitary capacitor of the array. Hence, the optimal value for the integrator feedback capacitor  $C_{f,opt}$  can be derived

$$C_{f,opt} = \frac{\xi}{b_2} C_u \left( 1 + 3\sigma\sqrt{2^M - 1} \right). \quad (14)$$

The value of the reference feedback capacitor,  $C_{sR,opt}$ , is then sized as

$$C_{sR,opt} = b_2 C_{f,opt}. \quad (15)$$

The capacitive scaling of the proposed implementation has the additional advantage of naturally compensating the magnitude difference between the measurements of the MSB and LSB sections of the SC-DAC. Let us consider again the proposed test strategy described in Section II.C in the view of the proposed implementation. For the measurements of the MSB segment, switch  $S_X$  in Fig. 3 is turned on and the integrator input gain is given by  $b_X \approx 2^M C_u/C_f$ . As discussed before, for an ideal SC-DAC, the voltage generated at the node  $V_X$  when generating the partial MCTs is given by  $\Delta_X$ , as defined in the previous section. Conversely, when  $S_A$  is on for the measurement of the LSB segment of the SC-DAC the integrator input gain is given by  $b_A \approx (2^L + 1)C_u/C_f$ ,

while, for an ideal SC-DAC, the voltage generated at node  $V_A$  is given by  $\Delta_A$ , as defined in the previous section.

If we define  $r$  as the ratio between step sizes, we obtain

$$r = \frac{\Delta_X}{\Delta_A} \approx \frac{V_{ref}/2^M}{V_{ref}/(2^L + 1)} = \frac{2^L + 1}{2^M}, \quad (16)$$

but at the same time if we compute the ratio between the input gains of the integrator in the two configurations

$$\frac{b_X}{b_A} = \frac{FS_{I\Sigma\Delta}^{LSB}}{FS_{I\Sigma\Delta}^{MSB}} = \frac{C_{out,MSB}/C_f}{C_{out,LSB}/C_f} = \frac{2^M}{2^L + 1} = \frac{1}{r}, \quad (17)$$

which shows that the FS of the IΣΔ is scaled in a way that naturally compensates the change in magnitude of the expected values of the partial step sizes. The proposed implementation assures that the factor by which these magnitudes change is exactly the value that guarantees that the measurement remains on the optimal range for both the MSB and LSB segments of the SC-DAC.

#### IV. RESULTS

In order to validate the feasibility and performance of the proposed on-chip reduced-code test strategy, we have designed a SC-SAR ADC together with an embedded IΣΔ converter in STMicroelectronics 65 nm CMOS technology, following the guidelines discussed in the previous sections. The SC-SAR ADC under test is a 10-bit ( $6 \times 4$ ) SC-SAR ADC. The unit capacitor in the SC-DAC array has been designed as a 9 fF MOM capacitor, the circuit is biased at  $V_{DD} = 1.2$  V and it is clocked at  $f_s = 60$  MHz. The digital logic controlling the approximation register and the execution of the test procedure has been implemented using behavioral VerilogA models to speed up simulations. Regarding the embedded first-order IΣΔ ADC, capacitors have been sized following the design guidelines in the previous section. The integration capacitor is sized as  $C_f = 11C_u$ , and the reference feedback capacitor is set to  $C_{sR} = 4C_u$ . Relative to the CDAC array in the SAR ADC, these extra capacitors represent an area overhead of about 15%. The resolution of the IΣΔ ADC has been set to  $R = 10$  bits and the full scale has been adjusted from equation (13) to be about four times the LSB of the partial CDACs. Again, the digital counter has been modeled in VerilogA to speed up the simulations.

In order to validate the performance of the proposed reduced-code static linearity test strategy, we use the mismatch Monte Carlo models in the Process Design Kit (PDK) of the technology to generate samples of the SC-SAR ADC under test. The worst-case sample in terms of static linearity has been selected and characterized using the proposed reduced-code test strategy and the standard Linearity Histogram Test (LHT) with 128 hits per code by electrical simulation. The obtained results for DNL and INL estimations are shown in Fig. 9a and b, respectively, while the estimation error, defined as the difference of the reduced-code results with respect to the LHT results, are shown in Fig. 9c and d. As it can be observed, the test results are very close to each other, with differences smaller than 0.06 LSB. With respect to the test time savings, the proposed reduced-code static test only requires 10



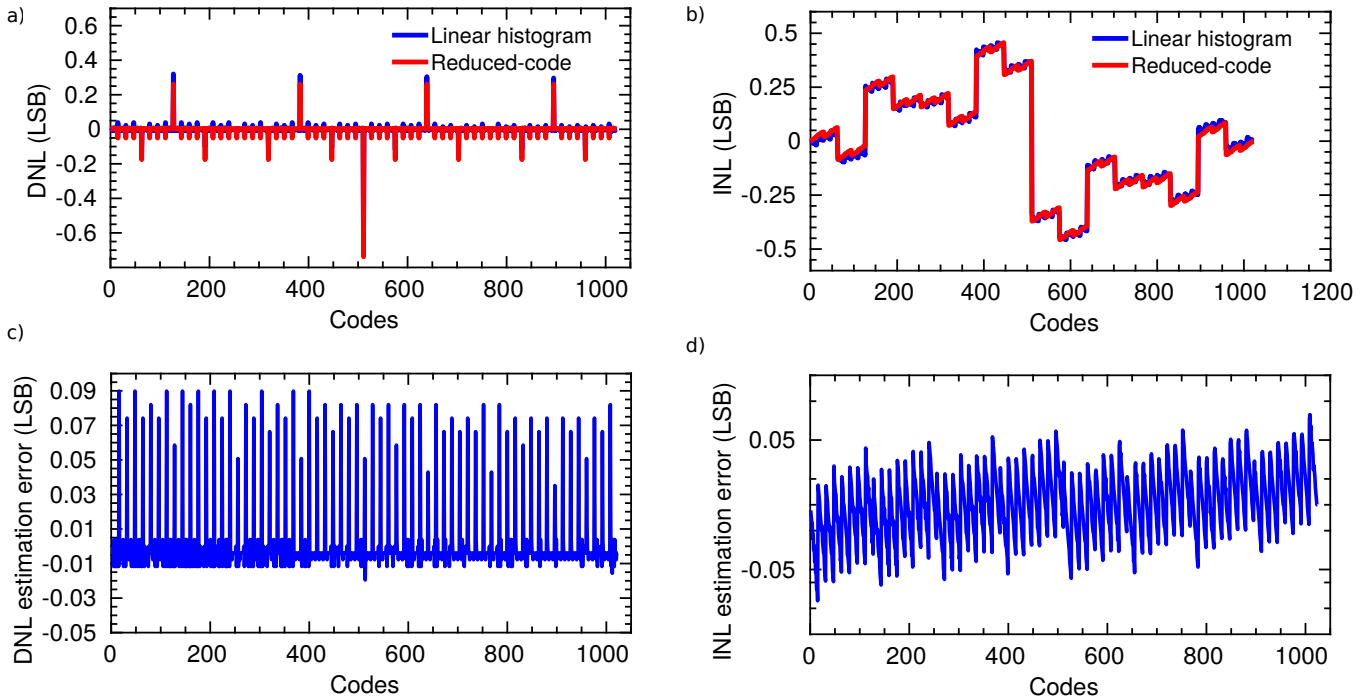


Fig. 9. Comparison between LHT and reduced-code linearity measurements for circuit implementation of SC-SAR ADC with  $R = 10$  bits ( $6 \times 4$ ): a) DNL measurements, b) INL measurements, c) DNL estimation difference, and d) INL estimation difference.

measurements, while the LHT has to traverse the complete set of codes of the ADC under test. Neglecting post-processing time, the reduced-code strategy offers about a 98% test time reduction with respect to a 128-hit-per-code histogram test.

It is important to remark that the novel reduced-code test strategy in this manuscript also offers test time savings with respect to our previous work [15]. Thus, the modified SAR operation in [10], [15] required  $i \times 2^R$  cycles for measuring the code width associated to the  $i$ -th MCT, while our novel strategy requires  $3 \times 2^R$  cycles per measurement, independently of the capacitor being exercised. For a 10-bit SAR ADC, this difference represents test time savings of about 54%.

To further validate the performance of the proposed reduced-code static test technique, another set of experiments were performed to verify the functionality of the technique in the presence of missing codes. In these experiments, we artificially increased the mismatch of the capacitors above the technological value in the PDK in order to generate missing codes in the transfer function of the 10-bit SC-SAR ADC under test. Results are shown in Fig. 10 where we present the DNL characteristic of the SC-SAR ADC under test zoomed around the area of two missing codes (DNL = -1 LSB), measured both with the proposed reduced-code static test strategy and with the standard LHT with 128 hits per code. It is clear to see that the proposed reduced-code technique accurately detects the presence of the missing codes.

## V. CONCLUSIONS

This work presented a novel reduced-code static linearity test technique appropriate for Split-Capacitor SAR ADCs. The proposed test strategy is based on the direct measurement of

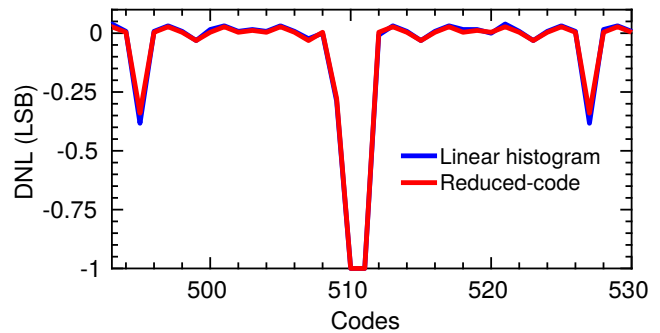


Fig. 10. Detection of missing codes.

the code width associated to the Major Carrier Transitions of each of the segments of the SC-DAC of the converter under test. The set of MCTs are directly generated with no need for a test stimulus, which simplifies the practical implementation of the technique. It has been shown that the complete static linearity characteristic of an  $N$ -bit SC-SAR ADC can be inferred with only  $N$  measurements, which may yield significant test time reductions in the static characterization of this system.

We have provided practical guidelines for the on-chip implementation of the proposed reduced-code test technique. In this line, it has been shown that the code width associated to each MCT can be measured with an embedded  $\Sigma\Delta$  ADC. Furthermore, the design of such a converter has been discussed and we have proposed an efficient implementation that reuses the input SC-DAC as sampling capacitor for the  $\Sigma\Delta$  ADC.

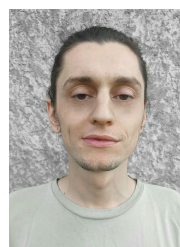
The feasibility and performance of the proposed reduced-code test technique have been validated with behavioral and electrical simulations of a 10-bit ( $6 \times 4$ ) SC-SAR ADC imple-

mented in a 65 nm CMOS technology. Obtained results show the equivalence of the proposed measurements to standard Linearity Histogram Test methods. INL and DNL estimation errors were contained to  $\pm 0.06$  LSB, while test time savings are in the order of 98% when compared to a 128-hit-per-code histogram.

Future work in this research will include the fabrication and experimental validation of the proposed BIST technique and the estimation of test quality metrics (i.e., test escapes and yield loss).

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