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Electrical properties of metal/Al_2O_3/$In_{0.53}Ga_{0.47}As$ capacitors grown on InP

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To overcome the Fermi-level pinning in III-V metal-oxide-semiconductor capacitors, attention is usually focused on the choice of dielectric and surface chemical treatments prior to oxide deposition. In this work, we examined the influence of the III-V material surface cleaning and the semiconductor growth technique on the electrical properties of metal/Al_2O_3/$In_{0.53}Ga_{0.47}As$ capacitors grown on InP(100) substrates. By means of the capacitance-voltage measurements, we demonstrated that samples do not have the same total oxide charge density depending on the cleaning solution used [$(NH_4)_2S$ or NH_4OH] prior to oxide deposition. The determination of the interface trap density revealed that a Fermi-level pinning occurs for samples grown by metalorganic chemical vapor deposition but not for similar samples grown by molecular beam epitaxy. Deep level transient spectroscopy analysis explained the Fermi-level pinning by an additional signal for samples grown by metalorganic chemical vapor deposition, attributed to the tunneling effect of carriers trapped in oxide toward interface states. This work emphasizes that the choice of appropriate oxide and cleaning treatment is not enough to prevent a Fermi-level pinning in III-V metal-oxide-semiconductor capacitors. The semiconductor growth technique needs to be taken into account because it impacts the trapping properties of the oxide. *Published by AIP Publishing.*
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I. INTRODUCTION

To surpass the limitations that the scaling of Si-based metal-oxide-semiconductor field-effect transistors (MOSFETs) is approaching, alternative III-V semiconductors have been investigated to replace Si as a channel material. Among them, InGaAs semiconductor has a higher electron mobility than Si and is of great interest for n-channel MOSFETs. $In_{0.53}Ga_{0.47}As$ is of particular interest because it is lattice matched to InP substrates and its small bandgap allows using it for lower operating voltages and less power dissipation.[1–4]

One of the most serious challenges for III-V channel MOSFETs is the reduction of the density of traps at the dielectric/III-V semiconductor interface. The choice of the gate dielectric is a key issue to avoid a Fermi-level pinning and to get a thermodynamically stable interface with the semiconductor. Atomic Layer Deposition (ALD) grown Al_2O_3 offers several advantages including a relatively large dielectric constant, a good thermal stability, and an interfacial self-cleaning on InGaAs by removing arsenic oxides which are believed to be the origin of the Fermi-level pinning.[5]

The surface chemical treatment prior to Al_2O_3 formation by ALD is also known to reduce native oxides. The capacitance-voltage (C-V) measurements of GaAs metal-oxide-semiconductor (MOS) capacitors demonstrated that sulfur-passivated GaAs leads to better frequency dispersion and a slightly smaller capacitance equivalent thickness than hydroxylated GaAs.[6]

In this work, we study the impact of the semiconductor growth technique and the surface chemical treatment prior to dielectric formation on the electrical properties of metal/Al_2O_3/$In_{0.53}Ga_{0.47}As$ capacitors grown on InP(100) substrates.

II. EXPERIMENTAL

Samples are Ni/Au/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS capacitors grown on 100 mm diameter S doped (100) InP substrates with a resistivity in the range of 0.69–1.34 mΩ·cm. The growth technique was either metalorganic chemical vapor deposition (MOCVD) with trimethylindium, trimethylgallium, and tertiarybuthylarsine as In, Ga, and As precursors, respectively, or molecular beam epitaxy (MBE). Samples fabricated by MOCVD epitaxy consist of a 200 nm unintentionally doped InP buffer layer started after an annealing under phosphorus atmosphere to remove native oxides. Then, a 200 nm unintentionally doped InGaAs layer is grown at 500–600 °C. For the epitaxy by MBE, the procedure begins with an annealing at 500–505 °C under arsenic atmosphere to clean the surface from native oxides, followed by the epitaxy of a 200 nm unintentionally doped InGaAs layer grown in the range of 480–485 °C. A surface chemical treatment with a NH_4OH solution (4%) during 1 min or a

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TABLE I. Details of the samples examined in this work.

Sample identification	Surface chemical treatment prior to Al_2O_3 deposition	Epitaxial technique for InGaAs growth
MO_{OH}	NH_4OH	MOCVD
MO_S	$(NH_4)_2S$	MOCVD
MB_S	$(NH_4)_2S$	MBE

$(NH_4)_2S$ solution (20%) during 20 min is used to clean InGaAs surface at room temperature prior to dielectric deposition. Then, an Al_2O_3 layer was formed by ALD at 300 °C using trimethylaluminum (TMA) and water as sources. TMA is the first precursor injected in ALD chamber. A Ni/Au (40/60 nm) bilayer was evaporated at room temperature on the top of the dielectric to create circular metallic electrodes of 0.126 μm^2 with a shadow mask and on the back side of the substrate to realize a planar contact. Sample description is summarized in Table I.

X-ray photoelectron spectroscopy (XPS) was performed using a Thermo Scientific Theta 300 tool in Parallel Angle Resolved mode (Pass Energy = 100 eV). The thickness measurements of Al_2O_3 layers were achieved with a J.A. Woollam M-2000 spectroscopic ellipsometer. The surface of the InGaAs layer was analyzed with a Bruker Dimension FastScan Atomic Force Microscope. The capacitance-voltage and conductance-voltage (G-V) measurements were recorded using an E4980A Agilent LCR meter. An Accent DL8000 Fourier Transform Deep Level Transient Spectroscopy (DLTS) system with a 100 mV test signal at 1 MHz was used to obtain DLTS data.

III. RESULTS AND DISCUSSION

A. Structural characterization

Atomic force microscopy allowed determining the InGaAs surface roughness just after epitaxy. The results are summarized in Fig. 1. For all samples, the root mean square (RMS) of the roughness is 0.2 ± 0.1 nm, whatever the growth technique used.

Figure 2 reports XPS spectra of the InGaAs surface after 2 nm Al_2O_3 deposition without and with $(NH_4)_2S$ (MO_S) and NH_4OH (MO_{OH}) treatments. We see that indium and arsenic oxides are removed by chemical cleaning and Al_2O_3 deposition by ALD. However, Ga-O bonds remain on spectra after cleaning in both treatments, with a slightly higher peak intensity for NH_4OH solution. Sulfur passivation of III-V materials using $(NH_4)_2S$ has been shown to be very effective in order to rule out native oxide regrowth after its removal.[6,7] Then, it is expected that $(NH_4)_2S$ is more efficient to remove Ga oxide than NH_4OH.

B. C-V measurements

Using C-V measurements at 300 K, the doping level of InGaAs layers is evaluated at 3×10^{16} cm^{-3} for all samples. According to Eq. (1), the slope of inverted capacitance versus dielectric thickness curve (Fig. 3) allows extracting the permittivity of the oxide

$$\frac{1}{C} = \frac{e_{ox}}{\varepsilon_{ox}} + \frac{1}{C_{SC}}, \tag{1}$$

where C is the total capacitance of the MOS structure per unit area, C_{SC} is the capacitance of the semiconductor per unit area, e_{ox} is the dielectric thickness, and ε_{ox} is the absolute permittivity of the oxide.

The relative permittivity ε_r of Al_2O_3 layer deposited by ALD was found to be 7.5 using data of Fig. 3. Oxide capacitance C_{ox} cannot be determined from the accumulation capacitance (C_{acc}) of experimental C-V characteristics due to the low conduction band density of states of III-V semiconductors.[8] Instead, it is derived from Eq. (2), which is independent of C-V measurement

$$C_{ox} = \frac{\varepsilon_{ox}}{e_{ox}}. \tag{2}$$

In Table II, we see that the Al_2O_3 thickness and the oxide capacitance of MOS capacitors are found to be 8.1 ± 0.1 nm and 0.82 ± 0.01 $\mu F/cm^2$, respectively.

From C_{ox} values, flat band voltages V_{FB} were extracted with the graphic method[9] based on the following equation:[10]

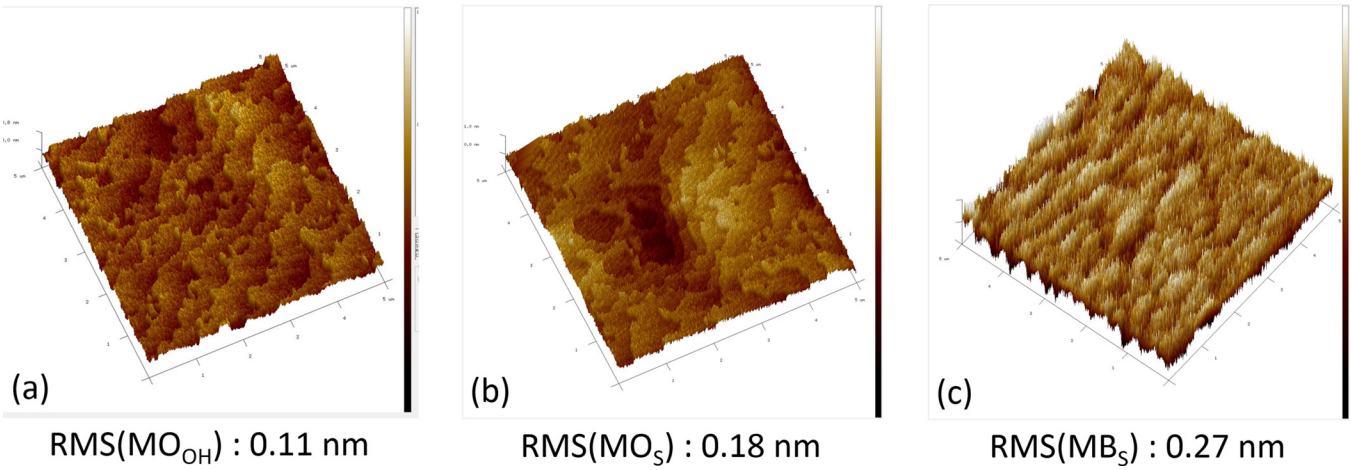

FIG. 1. Atomic force microscopy analysis of the sample's surface.

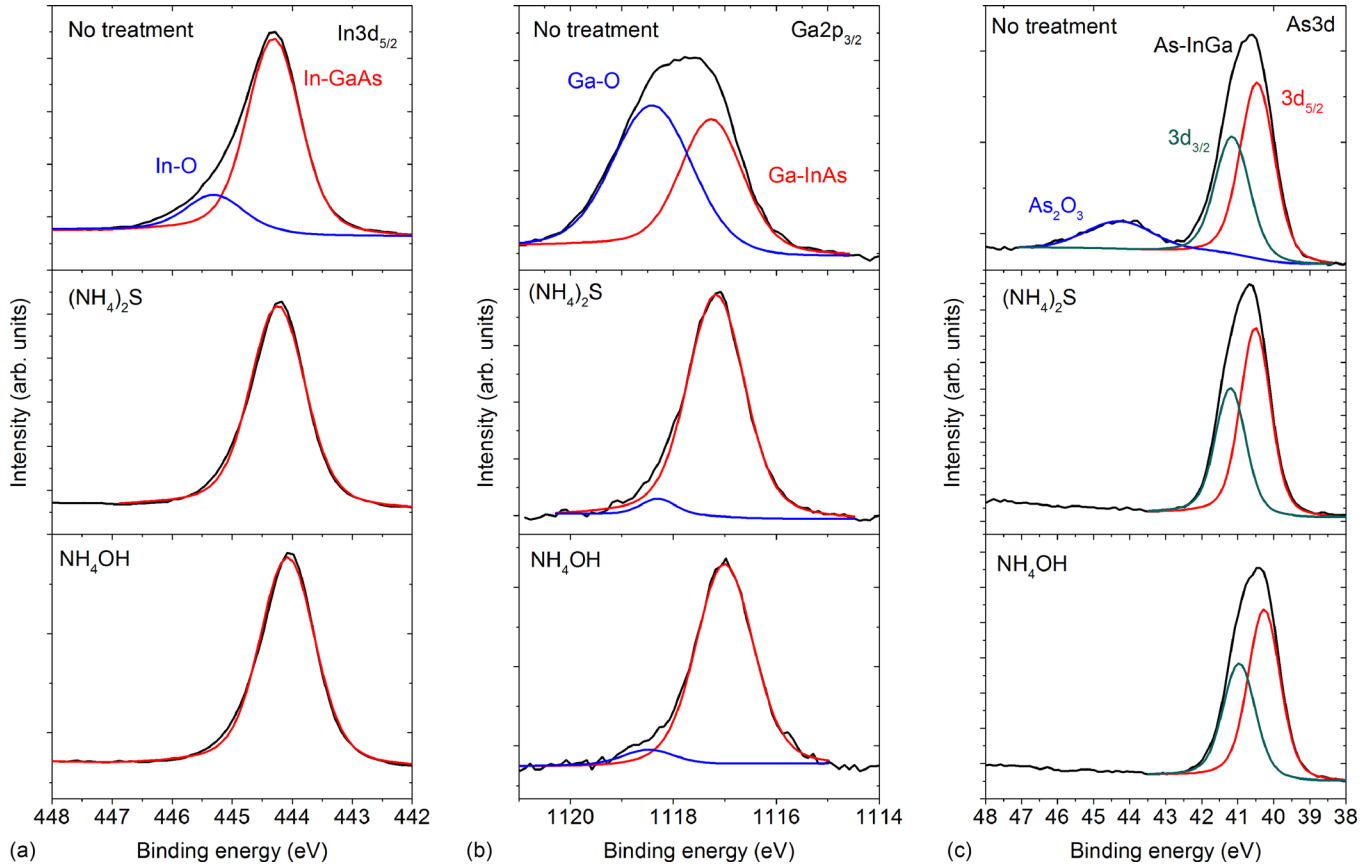

FIG. 2. XPS analysis of Al_2O_3 (2 nm)/InGaAs (MOCVD) interface without and with InGaAs surface cleaning using $(NH_4)_2S$ and NH_4OH. Less Ga-O bonds appear on the spectrum with $(NH_4)_2S$ treatment.

$$\left(\frac{C_{ox}}{C}\right)^2 - 1 = \frac{2\,C_{ox}^2}{q\,N_d\,\varepsilon_{SC}}\,(V_G - V_{FB}), \tag{3}$$

where V_{FB} corresponds to V_G when the left part of Eq. (3) reaches zero in the plot $\left(\frac{C_{ox}}{C}\right)^2 - 1$ versus V_G. The results are summarized in Table II.

The flat band voltage can be expressed using the following equation:[11]

$$V_{FB} = \varnothing_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{OX}}, \tag{4}$$

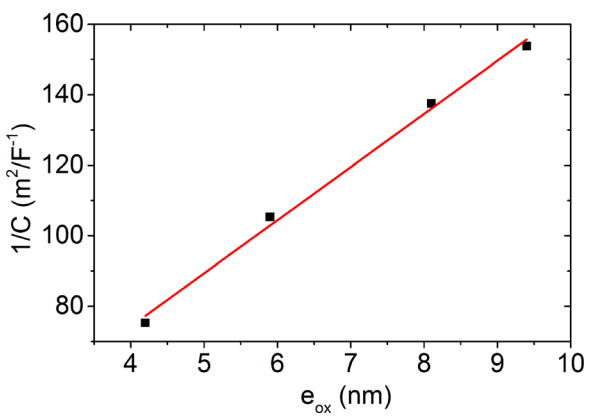

FIG. 3. Inverted total capacitance versus Al_2O_3 thickness of MOS capacitors cleaned with $(NH_4)_2S$ solution. According to Eq. (1), the permittivity of the dielectric is extracted from the slope of the curve.

where ϕ_{ms} is the work-function difference between the metal and the semiconductor, Q_f and Q_m are the fixed and mobile oxide charge, and Q_{ot} is the oxide trapped charge.

The V_{FB} difference between samples is thus directly linked to oxide charges. In Table II, a similar negative V_{FB} is found for samples MO_S and MB_S, whereas a positive and larger V_{FB} characterizes the sample MO_{OH}. Consequently, the amount of charges in Al_2O_3 oxide seems dependent on the surface chemical treatment but independent on the growth technique used for InGaAs epitaxy. Based on an assumed value of 5 eV for the Ni work function in the Au/Ni gate stack and 4.5 eV for the $In_{0.53}Ga_{0.47}As$ electron affinity, the total oxide charge density Q_{tot} has been determined at $1.3 \times 10^{12}\,cm^{-2}$, $2.1 \times 10^{12}\,cm^{-2}$, and $2.2 \times 10^{12}\,cm^{-2}$ for samples MO_{OH}, MO_S, and MB_S, respectively.[12] Q_{tot} represents the sum of a positive charge density uniformly distributed throughout the oxide and a negative sheet interface charge at the flat band voltage condition. It is the equivalent charge density located at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface.[12]

TABLE II. Oxide thickness e_{ox} determined by ellipsometry measurements, oxide capacitance C_{ox} extracted from Eq. (2), and flat band voltage of $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors found using Eq. (3).

Sample	e_{ox} (nm)	C_{ox} (μF/cm^2)	V_{FB} (V)
MO_{OH}	8.1	0.82	0.15
MO_S	8	0.83	–0.03
MB_S	8.2	0.81	–0.01

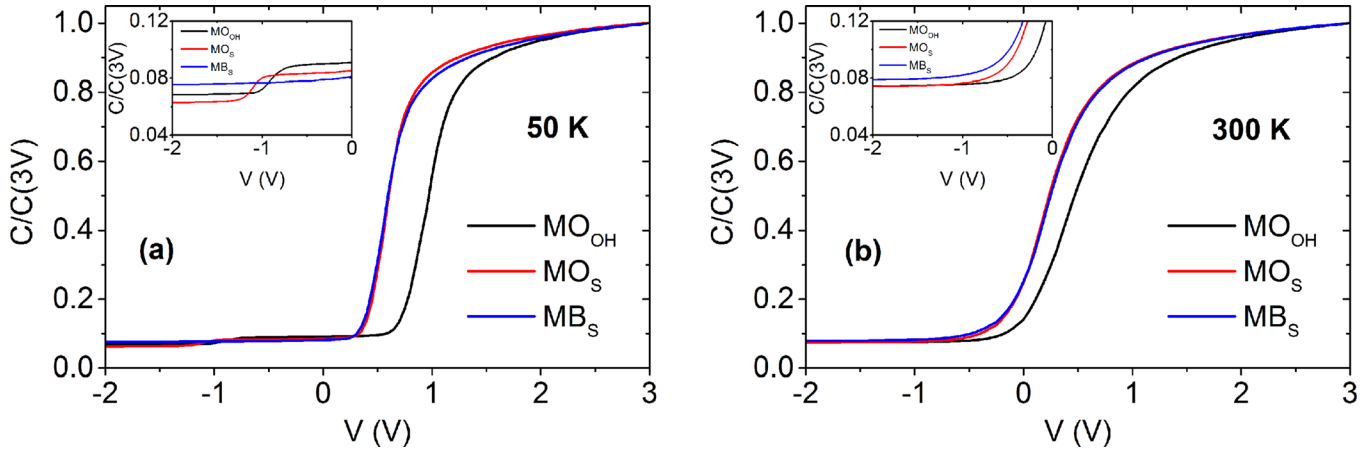

FIG. 4. Normalized 1 MHz C-V characteristics of MOS capacitors recorded at (a) 50 K and (b) 300 K. Insets are focused on minimum capacitances between –2 V and 0 V.

Although the peak intensity of Ga-O bonds reported by XPS analysis is slightly higher for NH_4OH solution, this difference between the two chemical treatments seems not enough relevant to explain the dissimilarity of Q_{tot} between the sulfur-passivated samples (MO_S and MB_S) and the hydrogenated sample (MO_{OH}).

In Fig. 4, normalized C-V characteristics highlight the difference on the flat band voltage between first samples MO_S and MB_S, which underwent a similar surface chemical treatment using $(NH_4)_2S$ and second sample MO_{OH} cleaned with NH_4OH solution.

At 50 K [Fig. 4(a)], we remark a step on C-V curves of samples MO_{OH} and MO_S around –1 V. This step does not occur with sample MB_S grown by MBE. Near –1 V, the space charge region in the InGaAs layer extends until the InGaAs/InP interface. As no buffer was grown by MBE technique, the InP substrate is in direct contact with the InGaAs layer. So, the InP doping, which is between 5.23×10^{19} and $1.12 \times 10^{20}\,cm^{-3}$, is too high to allow the appearance of a desertion region in InP. However, by MOCVD technique, a 200 nm nonintentional doped InP buffer layer was grown. At the interface with the InGaAs layer, the doping level of the InP buffer was measured by C-V at approximately $5 \times 10^{16}\,cm^{-3}$. This value is low enough to permit the formation of a desertion region in InP, which appears as an additional series capacitance on C-V plots of samples MO_{OH} and MO_S.

Previous data were completed by C-V measurements carried out on all MOS capacitors as a function of frequency and temperature. An example is shown in Figs. 5 and 6 at 300 K.

Figures 7 and 8 report the capacitance of MOS capacitors in accumulation at 3 V, recorded versus frequency (f) and temperature (T). For $f \leq 100$ kHz, the capacitance as a function of temperature follows the same trend for all samples. For highest temperatures in Fig. 7 and for all curves in Fig. 8, capacitances increase above 100 kHz. This behavior is due to a parasitic series inductance *Ls* which comes from our coaxial cables.[13] Experimental data of Figs. 7 and 8 were well fitted using the model developed by Yuan *et al.*[14] including a series inductance $Ls = 9 \times 10^{-7}$ H. For $f > 100$ kHz and $T \leq 150$ K [Fig. 7(a)] or $T \leq 125$ K [Fig. 7(b)], the capacitance versus frequency decreases for samples grown by MOCVD. A simulation of data with the model introduced by Yuan *et al.*[14] allowed attributing this behavior to a series resistance which dominates the effect of the parasitic series inductance.

To understand the series resistance (R_S) influence on the high frequency measurements, which depends on the epitaxial growth technique used, we plotted R_S versus temperature according to the following equation:[15]

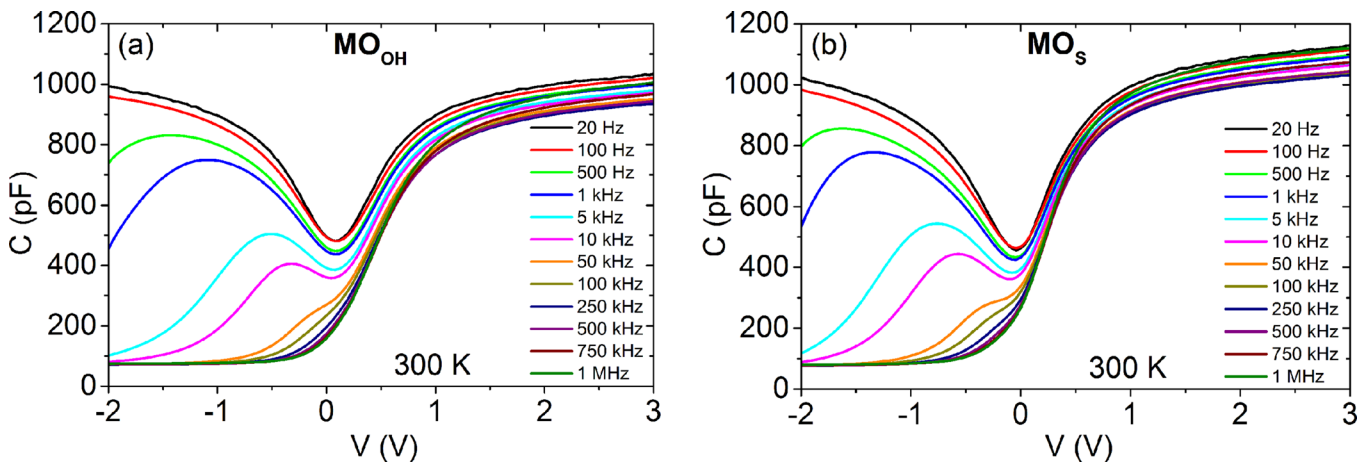

FIG. 5. C-V measurements of (a) MO_{OH} and (b) MO_S capacitors recorded as a function of frequency at 300 K.

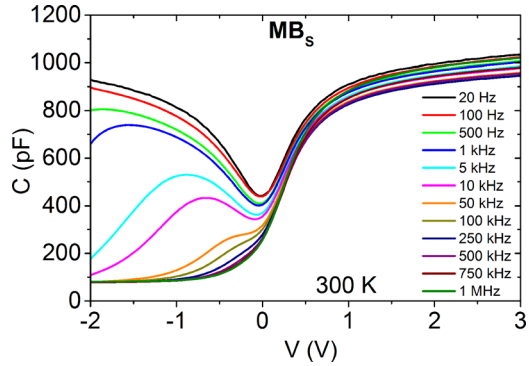

FIG. 6. C-V measurements of MB_S capacitor recorded as a function of frequency at 300 K.

$$R_S = \frac{G_{m,a}}{G_{m,a}^2 + \omega^2 C_{m,a}^2}, \tag{5}$$

where $G_{m,a}$ and $C_{m,a}$ are measured conductance and capacitance recorded in accumulation (3 V), respectively, and ω is the angular frequency.

In Fig. 9, over the whole range of temperature, the series resistance of sample MB_S remains below 30 Ω and 55 Ω for 1 MHz and 100 kHz, respectively. By decreasing the temperature, the series resistance of samples MO_{OH} and MO_S increases above 40 Ω at 1 MHz [Fig. 7(a)] and above 65 Ω at 100 kHz [Fig. 7(b)] for 150 K and 125 K, respectively. We conclude that an additional series resistance is recorded at low temperature for samples performed by MOCVD.

Using Eq. (6),[15] we also plotted the capacitance, corrected from the series resistance, as a function of temperature (Fig. 10)

$$C_C = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{\left[G_m - (G_m^2 + \omega^2 C_m^2)R_S\right]^2 + \omega^2 C_m^2}. \tag{6}$$

Capacitances are taken in the accumulation regime (3 V) at 100 kHz to avoid the series inductance effect and are normalized to 300 K values.

In Fig. 10, no difference appears between samples. Consequently, the capacitance measurements in the accumulation regime as a function of frequency and temperature reveal that samples do not behave similarly according to the semiconductor growth technique used. This different behavior is exclusively explained by an increase of the series resistance below 200 K for samples grown by MOCVD.

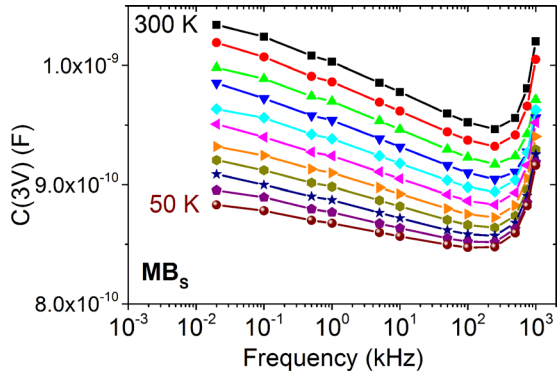

FIG. 8. Capacitance in accumulation at 3 V of MB_S capacitor recorded as a function of frequency and temperature between 50 K and 300 K with a step of 25 K.

C. Interface trap density determination

For all samples, trap energy E_T positions related to the conduction band minimum energy E_C as a function of gate voltage are reported in Fig. 11(a) based on calculations with the following equations:[15–17]

$$E_C - E_T = \frac{E_{Gap}}{2} + q V_S - q \varnothing_{Fi}, \tag{7}$$

where $\varnothing_{Fi} = \frac{kT}{q}\ln\left(\frac{N_d}{n_i}\right) = 0.278\,\text{eV}$ with $T = 300\,\text{K}$ and $\frac{E_{Gap}}{2} = 0.37\,\text{eV}$;

$$V_S = \int_{V_{FB}}^{V_g}\left(1 - \frac{C_{tot}^{LF}(V_g)}{C_{OX}}\right)dV_G, \tag{8}$$

where V_G is the gate voltage in the depletion region.

For samples MO_{OH} and MO_S, the trap level becomes nearly motionless close to the InGaAs midgap when the voltage becomes more and more negative. This behavior is

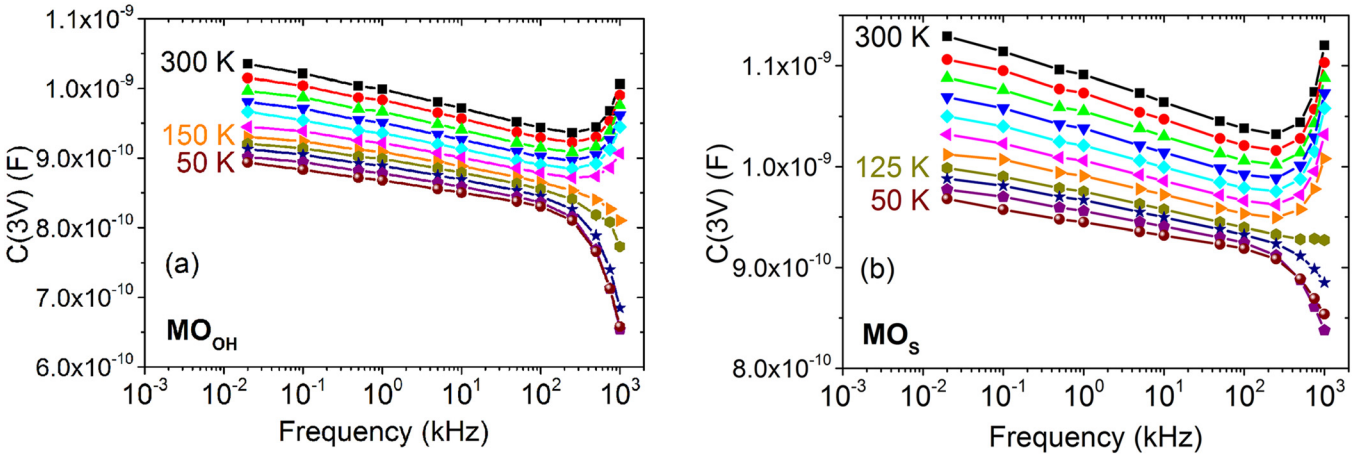

FIG. 7. Capacitance in accumulation at 3 V of (a) MO_{OH} and (b) MO_S capacitors recorded as a function of frequency and temperature between 50 K and 300 K with a step of 25 K.

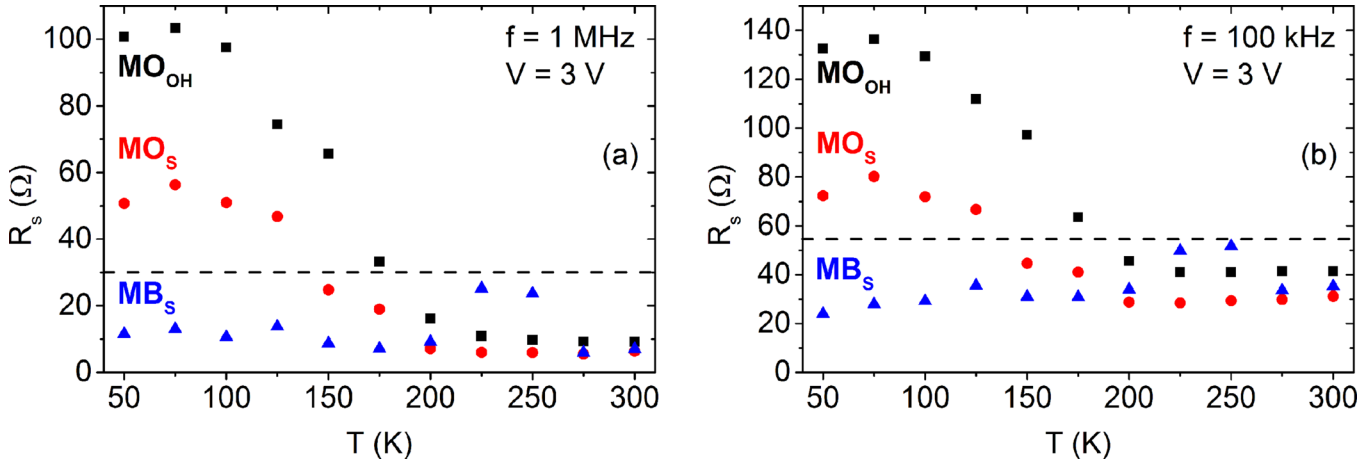

FIG. 9. Series resistances of MOS capacitors recorded in accumulation (3 V) at (a) 1 MHz and (b) 100 kHz as a function of temperature.

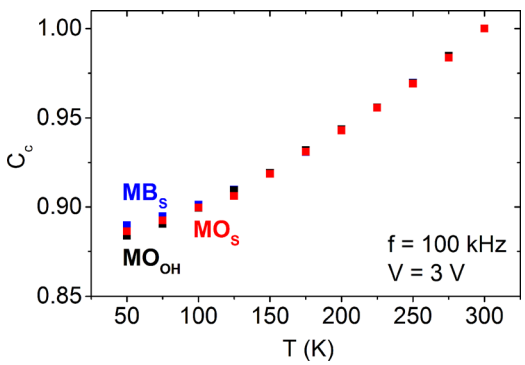

FIG. 10. Normalized corrected capacitances of MOS capacitors recorded at 100 kHz and 3 V as a function of temperature.

indicative of a Fermi-level (E_F) pinning. Such a trend does not appear with sample MB_S, meaning that E_F pinning is dependent on the growth technique used for the formation of the InGaAs layer, but is not dependent on the surface chemical cleaning prior to Al_2O_3 deposition.

In Fig. 11(a), we also remark that the curve of sample MO_{OH} is shifted toward larger $E_T - E_C$ values. To elucidate this point, we plotted Q_{SC}/C_{OX} versus $V_G - V_{FB}$ for all samples [Fig. 11(b)], where Q_{SC} is the total charge in the semiconductor. No difference appears between samples. Since Q_{SC}/C_{OX} and $V_G - V_{FB}$ are linked according to Eq. (9),[16] we conclude that the higher V_{FB} value for sample MO_{OH} is responsible for the shift observed in Fig. 11(a)

$$V_G = V_S + V_{FB} - \frac{Q_{SC}}{C_{ox}}, \tag{9}$$

where V_S is the surface potential.

Interface trap density (D_{it}) was determined at 300 K using the conductance (G) method and low and high frequency (LF-HF) measurements. For the conductance method,[15] the equivalent parallel conductance G_P is evaluated for several frequencies between 100 Hz and 1 MHz from capacitance and conductance measurements with the following equation:

$$G_P = \frac{\omega^2 C_{ox}^2 G_m}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \tag{10}$$

D_{it} is then estimated from the normalized parallel conductance peak [Eq. (11)]

$$D_{it} \approx \frac{2.5}{A\,q} \left(\frac{G_P}{\omega}\right)_{max}, \tag{11}$$

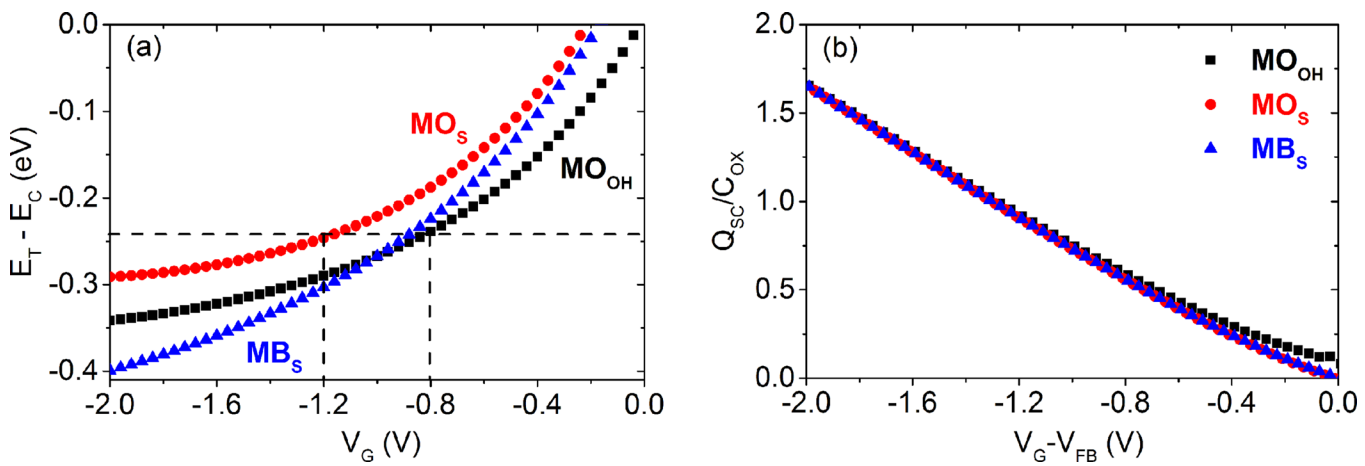

FIG. 11. (a) Trap energy positions in InGaAs bandgap related to the conduction band minimum energy as a function of gate voltage. (b) Comparison of Q_{SC}/C_{OX} versus $V_G - V_{FB}$ plots for all samples.

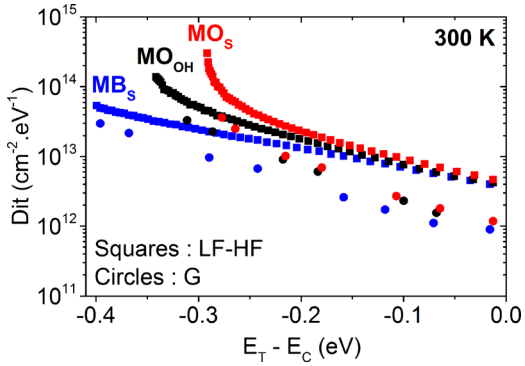

FIG. 12. Interface trap density of MOS capacitors determined at 300 K with low frequency–high frequency (squares) and conductance (circles) methods.

where A is the device area and q is the elementary charge.

D_{it}, determined with the LF-HF method[15] [Eq. (12)], was carried out using the capacitance measurements at 20 Hz and 1 MHz

$$D_{it}(V_G) = \frac{C_{ox}}{q}\left(\frac{C_m^{LF}}{C_{ox}-C_m^{LF}} - \frac{C_m^{HF}}{C_{ox}-C_m^{HF}}\right). \quad (12)$$

D_{it} determination as a function of the energy position in the bandgap for all samples was achieved using Eqs. (11) and (12) and Fig. 11(a). The results are reported in Fig. 12.

For all samples, we observe that D_{it} is lower with the conductance method. A limitation of the conductance method has been pointed out for interfaces with large D_{it}. If the interface trap capacitance is larger than the oxide capacitance ($qD_{it} > C_{OX}$), the measured impedance is dominated by the oxide capacitance and D_{it} is underestimated.[16,18] We assume that our devices fall into this consideration since $C_{OX}/q = 5 \times 10^{12}\,\text{eV}^{-1}\,\text{cm}^{-2}$.

Assuming that interface states are inactive at 1 MHz, the LF-HF method is expected to be more reliable. Nevertheless, whatever the method used, D_{it} increases toward midgap as expected from previous works.[16,19,20] For samples MO_S and MO_{OH}, a Fermi-level pinning prevents scanning a large energy range in the bandgap and explains the curvature to high D_{it} values for $E_T - E_C < -0.2$ V.[18] The Fermi-level pinning does not occur for the same energy due to the difference in the flat band voltage between these two samples. Finally, it is worth noting from Fig. 12 that it is hard to distinguish if one sample has a higher D_{it} than the other.

D. DLTS analysis

Figure 13 reports DLTS spectra recorded between 50 K and 330 K with a filling pulse height $V_P = 3$ V, a filling pulse width $t_P = 1$ ms, and a period width $T_W = 100$ ms. For a reverse bias $V_R = -0.8$ V, on all spectra, we observe some peaks in the range of 200–250 K, and only for sample MO_{OH}, an additional broad peak is visible with a maximum centered at 125 K [Fig. 13(a)]. Increasing the reverse bias to $V_R = -1.2$ V, the broad peak shifts to higher temperatures on MO_{OH} spectrum and a broad peak appears at 125 K on the MO_S spectrum [Fig. 13(b)]. The temperature of 125 K can be related to an energy difference $E_T - E_C$. In Fig. 11(a), we remark that an applied voltage of –0.8 V on the gate of sample MO_{OH} corresponds to the same $E_T - E_C$ value as an applied voltage of –1.2 V on the gate of sample MO_S. Consequently, broad peaks at 125 K on spectra of samples grown by MOCVD in Fig. 13 are expected to have the same origin. The difference of reverse bias needed for the broad peak appearance is linked to the flat band voltage difference between the two samples.

In Fig. 14, an increase of the reverse bias leads to shift the broad peak to higher temperatures. This behavior indicates that the trap related to the broad peak is only electric field dependent. As it shifts on a large energy range, it cannot be associated with a discrete level in the bandgap. Such a trend is usually attributed to interface traps.[21] The magnitude of the peak remains approximately constant below 150 K and rises close to 200 K when it meets peaks in the temperature range of 200–250 K.

For the sample grown by MBE (Fig. 15), no broad peak appears even after increasing the reverse bias up to –1.5 V. One main peak (labelled Eb1) dominates spectra and the other one appears as a low-temperature shoulder around 212 K (labelled Eb2). It means that there are at least two

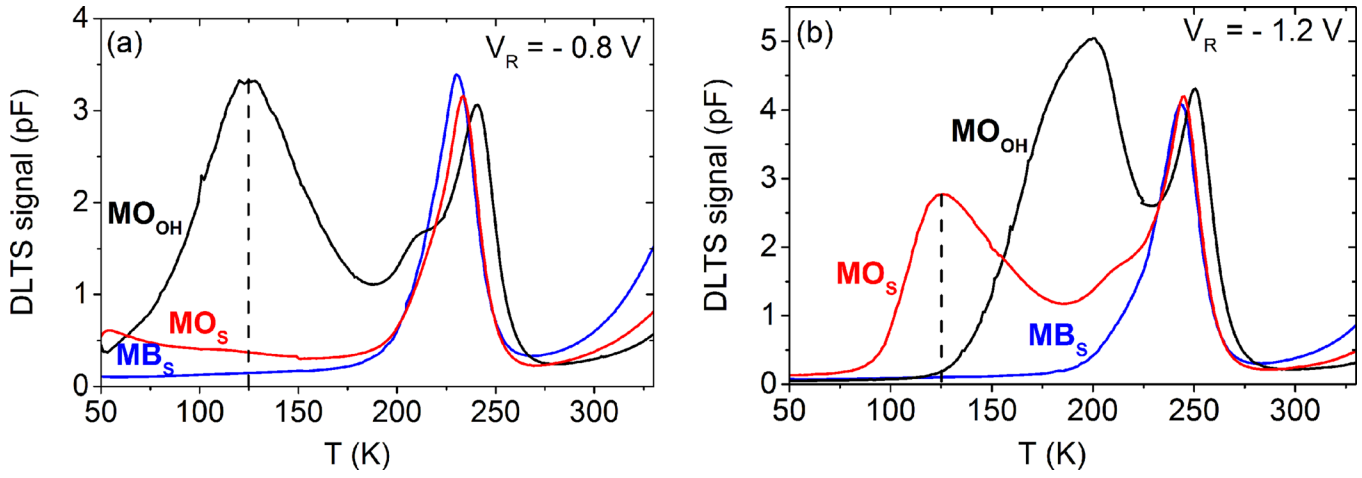

FIG. 13. DLTS spectra of MOS capacitors recorded in the warm-up mode with a filling pulse height $V_P = 3$ V, a filling pulse width $t_P = 1$ ms, a period width $T_W = 100$ ms, and a reverse bias: (a) $V_R = -0.8$ V and (b) $V_R = -1.2$ V.

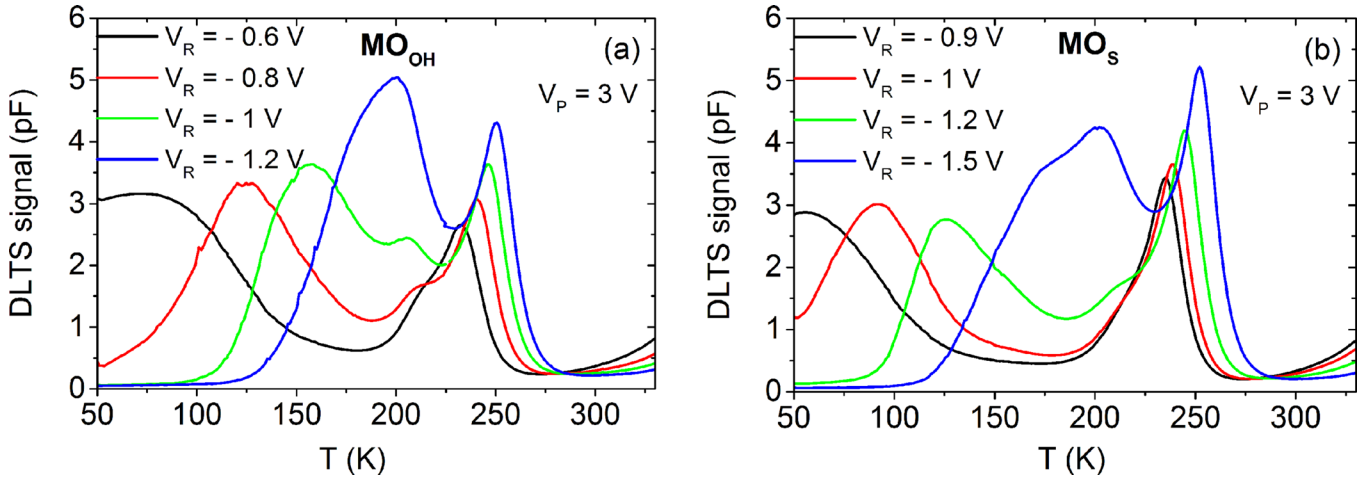

FIG. 14. DLTS spectra of samples (a) MO_{OH} and (b) MO_S recorded in the warm-up mode with a filling pulse height $V_P = 3$ V, a filling pulse width $t_P = 1$ ms, a period width $T_W = 100$ ms, and a varying reverse bias.

levels involved in the DLTS signal and they are expected to be the same as peaks in the range of 200–250 K on spectra in Fig. 14. When the reverse bias changes from –0.6 V to –1.5 V, the main peak Eb1 shifts to higher temperatures and its magnitude increases, whereas the peak Eb2 around 212 K does not move. This behavior reveals that Eb1 is electric field dependent. However, it is not likely that this peak comes from interface traps for three reasons: (i) its magnitude increases by changing the reverse bias, (ii) its temperature shift is lower than the one of the broad peak, and (iii) it does not follow the same trend as the broad peak when the filling pulse height is changed (Fig. 16).

In Fig. 16, when the filling pulse height is decreased from 3 V down to 0 V, the broad peak quenches, whereas peaks in the range of 200–250 K remain present despite a slight reduction in their amplitude. At 0 V, the MOS structure is in the flat band regime. To observe the broad peak, an injection of electrons in the oxide is necessary. This takes place when the filling pulse height is positive since the structure is in the accumulation regime. Electrons are trapped in the oxide and are subsequently emitted by the tunneling effect through interface states. Peaks above 200 K do not require the structure to reach the accumulation regime to be observed. So, it is likely that peaks Eb1 and Eb2 are related to levels in the InGaAs layer and are similar to the midgap states found in $In_{0.53}Ga_{0.47}As$ material.[22–24] The activation energy and the apparent capture cross-section of trap Eb2 were evaluated to $E_C - 0.37 \pm 0.01$ eV and $\sigma_{na} = 2.0 \pm 0.4 \times 10^{-15}$ cm^2. For trap Eb1, the activation energy moves from E_C – 0.38 eV to E_C – 0.46 eV when the reverse bias changes from –0.1 V to –1.5 V (with $V_P = 3$ V) and the apparent capture cross-section remains at $\sigma_{na} = 4.0 \pm 4 \times 10^{-15}$ cm^2. It is likely that traps Eb1 and Eb2 are associated with native defects since they are independent of the growth technique. Torchinskaya *et al.*[25] in their study of $In_{0.53}Ga_{0.47}As$/InP photodiodes suggested that a trap with E_C – 0.38 eV and $\sigma_{na} = 1.5 \times 10^{-15}$ cm^2 could be the same defect as the commonly observed EL2 center in GaAs. An electric field dependence has been proved for this defect.[26,27] Furthermore, the hybrid density functionals calculation revealed that in As-rich conditions, the As antisite (As_{Ga}), expected to be involved in EL2 center,[28] is the most stable defect in InGaAs.[29,30] This theoretical study also supports the As antisite in Ga position as the origin of the midgap defect at InGaAs/oxide interfaces. So, traps responsible for the DLTS signal above 200 K might be related to defects involving gallium vacancies whatever the growth technique used.[28,31]

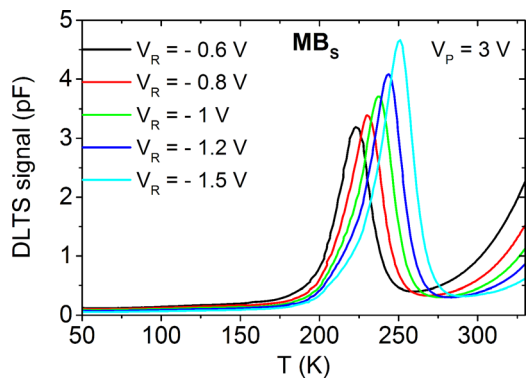

FIG. 15. DLTS spectra of sample MB_S recorded in the warm-up mode with a filling pulse height $V_P = 3$ V, a filling pulse width $t_P = 1$ ms, a period width $T_W = 100$ ms, and a varying reverse bias.

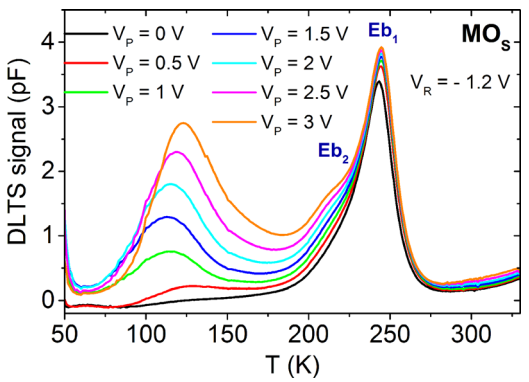

FIG. 16. DLTS spectra of sample MO_S recorded in the warm-up mode with a reverse bias $V_P = -1.2$ V, a filling pulse width $t_P = 1$ ms, a period width $T_W = 100$ ms, and a varying filling pulse height.

Bulk traps Eb1 and Eb2 are present in all samples. Thus, they cannot be responsible for the Fermi-level pinning observed in samples MO_{OH} and MO_S, even if these traps are expected to play a role on the trapping properties at the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface. However, in Fig. 14, it is obvious that the DLTS signal increases when the broad peak meets midgap bulk traps. One might suggest that the cumulative trapping effect of electrons by interface traps and bulk traps leads to a Fermi-level pinning near midgap in samples grown by MOCVD. This result is consistent with a peak of D_{it} positioned in the middle of the InGaAs bandgap at approximately 0.37 eV from the valence band edge in $Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ systems.[12,32]

The absence of a peak linked to the interface traps with sample MB_S might be explained by the distribution of traps in oxide bulk. In samples grown by MOCVD, oxide bulk traps seem close enough to the interface to allow the transfer of electrons by the tunneling effect. However, such a behavior does not occur with the sample grown by MBE, suggesting that oxide bulk traps are far from the interface and that electrons cannot reach the interface by the tunneling effect.

Finally, it is worth pointing out that the increase in the series resistance for samples grown by MOCVD appears below 200 K. It is exactly for the same temperature range that the broad peak is observed on DLTS spectra. So, we assume that trapping effects associated with the broad peak are related to the increase in the MOS structure resistance.

As a consequence, in this work, we demonstrated that the choice of an appropriate oxide[22] or an optimized surface chemical cleaning prior to oxide deposition are not the only points to address in order to prevent a Fermi-level pinning at the InGaAs surface. In addition to previous studies[12,33] which illustrated that the passivation of the interface states is a key issue to reduce D_{it}, the grown technique used to perform the InGaAs layer has to be taken into account to suppress the Fermi-level pinning.

IV. CONCLUSIONS

The electrical properties of metal/$Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS capacitors grown on InP(100) substrates have been studied by C-V, G-V, and DLTS techniques. Thanks to the flat band voltage determination, the chemical treatment of the InGaAs surface prior to Al_2O_3 deposition is suspected of influencing the total oxide charge density. It is suggested that the difference between sulfur-passivated samples (MO_S and MB_S) and hydrogenated sample (MO_{OH}) could be partly attributed to the slightly higher peak intensity of Ga-O bonds reported using XPS analysis for NH_4OH solution.

The assessment of D_{it} revealed that a Fermi-level pinning occurs for samples grown by MOCVD near the middle of the InGaAs bandgap. DLTS investigations highlighted that two distinct signals dominate spectra of samples grown by MOCVD. The first one, which does not appear on DLTS spectra of the sample grown by MBE, is a broad peak attributed to the tunneling effect of carriers trapped in oxide toward interface states. This trapping phenomenon is associated with an increase in the series resistance of MOS capacitors. The second signal is common to all samples whatever the growth technique used. It involves at least two traps expected to be related to native defects in InGaAs. The broad DLTS peak is suggested to be responsible for the Fermi-level pinning in samples grown by MOCVD when the Fermi-level reaches the middle of the InGaAs bandgap where the levels from native defects are located.

This work shows the influence of the semiconductor growth technique on the trapping properties of the oxide in $Al_2O_3/In_{0.53}Ga_{0.47}As$ MOS systems. We demonstrated that the choice of dielectric and surface chemical treatments prior to oxide deposition is not enough to consider the Fermi-level pinning issue. The semiconductor growth technique has to be taken into account, because it impacts the trapping properties of the oxide, which can lead to pin the Fermi level.

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