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► **To cite this version:**

Philippe Ferrandis, Matthew Charles, Charlotte Gillot, René Escoffier, Erwan Morvan, et al.. Effects of negative bias stress on trapping properties of AlGa_N/Ga_N Schottky barrier diodes. *Microelectronic Engineering*, 2017, 178, pp.158-163. 10.1016/j.mee.2017.05.022 . hal-01987673

HAL Id: hal-01987673

<https://hal.science/hal-01987673v1>

Submitted on 21 Jan 2019

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Effects of negative bias stress on trapping properties of AlGaN/GaN Schottky barrier diodes

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ABSTRACT

Power diodes or transistors must be able to work in high voltage/high current use, for instance in AC/DC converters. However, in such aggressive conditions trapping effects can occur. In this work, a negative voltage stress has been applied to AlGaN/GaN Schottky barrier diodes by sweeping the bias from 0 V to -600 V. This voltage corresponds to the real conditions of use of the power diodes. Using deep level transient spectroscopy measurements, we demonstrated that five traps labeled E1, E2, E3, B and A with activation energies 0.4, 0.44, 0.50, 0.58 and 0.65 eV respectively, are linked to the effects of the negative bias stress. Trap E2 has been localized in the channel region and carbon impurity is expected to be involved in trap E1. We demonstrated that no significant contribution on the reduction of the sheet carrier concentration in the channel can be attributed to these deep traps.

Keywords:

DLTS

Defects

GaN

Schottky barrier diode

Trap levels

Stress

1. Introduction

The AlGaN/GaN heterostructure field-effect transistor plays an important role in high-power and high-frequency applications [1,2]. However, charge trapping phenomena limit the dynamic performance of these devices for next generation electronics [3]. One of the clearest effects of traps is the so-called current collapse, i.e., a persistent yet recoverable reduction of the DC drain current after the application of a high gate voltage [4,5]. This effect is reported to be related either to surface states [6,7] or to charge trapping at deep levels, which can be present in the as-grown material, related to the processing conditions [8], and/or induced by electrical stress. As a result, a great deal of interest has been generated in detecting and identifying these trapping centers and in determining in which part of the device structure they are located. Several works reported deep levels in GaN at 0.18 [9–11], 0.5 [10–13], 0.76 [10–11], 1.47 [9], 1.8 [5] and 2.85 eV [5] below the conduction band minimum (E_C) which may account for electrons trapped and be responsible for current collapse. In this work, we present the negative

bias effects on trapping properties of AlGaN/GaN Schottky barrier diodes (SBDs) thanks to deep level transient spectroscopy (DLTS) measurements. The aim is to determine if deep traps located in the upper part of the GaN layer can contribute to electrons trapping during the use of a power diode at room temperature.

2. Experiment

The AlGaN/GaN bilayer was grown by metalorganic chemical vapor deposition (MOCVD) on 200 mm diameter silicon substrate, oriented (111). The epitaxy consists of an AlN nucleation layer, followed by 1.6 μm of AlGaN buffer layers, then 1.6 μm thick semi-insulating carbon doped GaN buffer layer, a 100 nm unintentionally doped GaN layer acting as the channel, a 1 nm unintentionally doped AlN layer and a 24 nm unintentionally doped $\text{Al}_{0.22}\text{Ga}_{0.78}\text{N}$ layer. Interdigitated comb-like diodes with six $15 \times 1000 \mu\text{m}$ fingers are then formed using TiN/W as Schottky electrodes and Ti/Al annealed for 30 s at 875 °C as Ohmic contacts. The Schottky/Ohmic spacing is 15 μm and is passivated with Si_3N_4 . In this work, the measurements of two identical diodes #1 and #2 taken at two positions on the same wafer are introduced. An Accent DL8000 Fourier Transform DLTS system with a 100 mV test signal at 1 MHz was used to obtain DLTS data. The negative voltage stress was performed using an Agilent B1505A power device analyzer/curve tracer.

3. Results

3.1. Measurements

The capacitance-voltage (C-V) characteristic at room temperature of fresh diode #2 used for DLTS measurements exhibits a pinch-off voltage at -1.6 V, as shown in Fig. 1.

DLTS measurements were recorded between 50 K and 400 K in the warm up mode. No signal was detected below 180 K with a filling pulse time up to 10 ms. Above 330 K, a negative DLTS signal related to a hole-like trap appears (not shown here) and disturbs the positive signal, especially for filling pulses larger than 1 ms. As a consequence, for this study, we focused our attention on positive DLTS signals related to electron traps in the range 180 K–320 K.

In Fig. 2, we see DLTS spectra of two diodes #1 and #2 recorded with a reverse bias $V_R = -10$ V, a filling pulse height $V_p = 0$ V, a filling pulse width $t_p = 10$ ms and a period width $T_w = 1$ s. Both diodes come from two different positions on the wafer. We remark that the same phenomenon occurs when the diodes are subjected to a negative voltage stress. In the following, the discussion deals with the measurements of diode #2 because the DLTS signal on spectra of this diode is higher and less noisy. However, the same results has been obtained with diode #1.

In Fig. 2b, the DLTS signal of the fresh diode (black curve) increases between 200 K and 275 K, before becoming nearly independent of the temperature. The diode was then subjected to a negative voltage stress applied at room temperature to the Schottky electrode by sweeping the bias from 0 V to -600 V (steps of 6 V). The reverse current between 0 V and -600 V, recorded during the stress, remains constant and enough low to keep a good accuracy in the DLTS measurements. On DLTS spectrum recorded immediately after stress (red curve), we observe two main changes. First, the signal rises at lower temperature, from 190 K to 255 K, then a significant reduction of the signal appears at 280 K. This spectrum modification indicates that the trapping properties of the diode have been modified by the high negative voltage applied to the Schottky contact. The stress effect demonstrated in Fig. 2 with diodes #1 and #2 has been confirmed with a third diode close to the two firsts used to carry out DLTS measurements exhibited in this work.

3.2. Data simulation

Multiple peak fits of DLTS data before and after stress were performed according to the theory introduced by Weiss and Kassing [14]. To fit DLTS data in the temperature range of 180 K–320 K, we first used traps A, A_x and B which are commonly observed in GaN, taking their signatures from the literature. Among the range of activation energies and capture cross sections summarized in Table 1, the selected trap

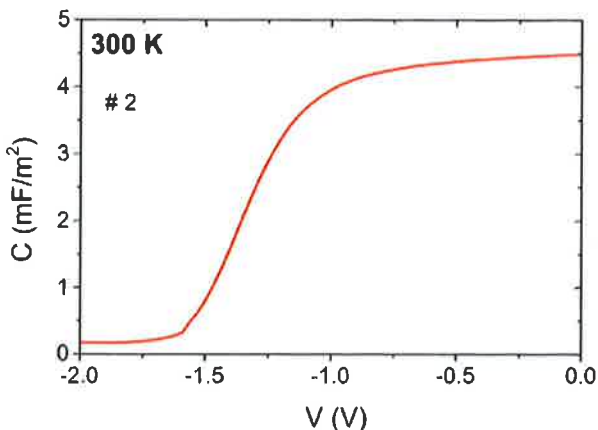


Fig. 1. Capacitance voltage measurement at room temperature of fresh AlGaIn/GaN SBD #2.

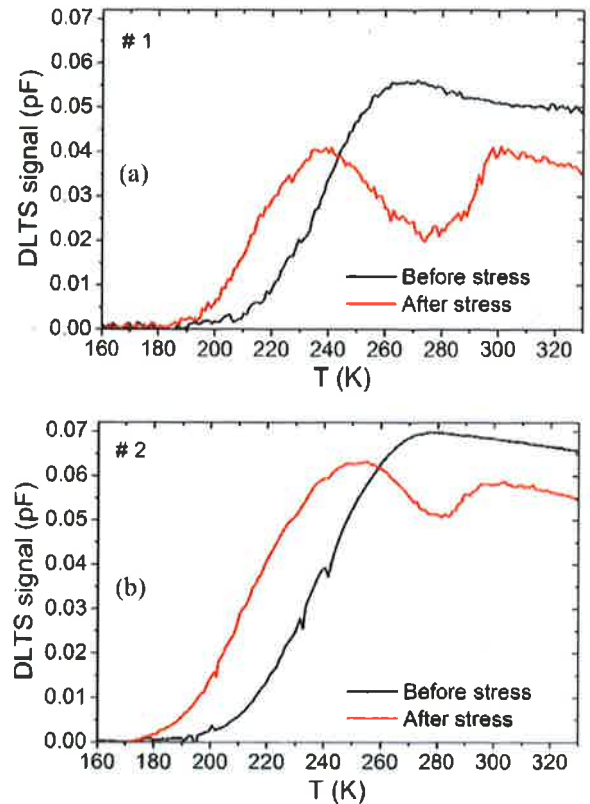


Fig. 2. DLTS measurements on AlGaIn/GaN SBDs #1 (a) and #2 (b) before and after stress, $V_R = -10$ V, $V_p = 0$ V, $t_p = 10$ ms and $T_w = 1$ s. (For interpretation of the references to color in this figure, the reader is referred to the web version of this article.)

features were those which gave the best fit of the experimental data. Before stress (Fig. 3a), two additional traps are necessary to correctly fit the experimental curve (labeled E2, E3). After stress (Fig. 3b), we had to add another trap (labeled E1) to complete the 5 previous peaks.

The reliability of this method was checked by fitting several spectra of diodes #1 and #2 with different filling pulse widths t_p (Fig. 4) and period widths T_w (Fig. 5a). The activation energies relative to E_c of GaN and the capture cross sections of peaks which allowed to fit all spectra are summarized in Table 2.

In Fig. 3, the amplitude of the peak A_x is over estimated to compensate the absence of others levels at higher temperature and therefore the change in this amplitude cannot be analyzed.

In Fig. 6, we observe a logarithmic dependence of the peak amplitudes on t_p for all peaks, without saturation. Additional measurements were carried out with filling pulse widths up to 1 s and no saturation of the DLTS signal was observed.

To achieve a perfect fit of the experimental data in Fig. 5a, when T_w became lower, only the amplitude of the peaks was increased, keeping constant the activation energy and the capture cross section (Fig. 5b). As no saturation of the DLTS signal occurs when the filling pulse width is increased (Fig. 6), a higher peak height is expected for a shorter T_w , since the traps are subjected to more filling pulses over same time period [19,42].

On the other hand, Sasikumar et al. [3] studied the correlation between trap formation and electric stress-induced degradation in Plasma Assisted MBE grown AlGaIn/GaN HEMTs. In their work, they found that the electric stress produces the increase of a constant drain-current DLTS signal associated with $E_T = 0.45$ eV and $\sigma_T = 5 \times 10^{-17}$ cm².

Previous works also reported the increase of the DLTS signal of a trap at $E_c - 0.5$ eV and $\sigma_T = 5 \times 10^{-16}$ cm² localized in GaN buffer layer and

Table 1

Level features (E_a : activation energy, σ_{na} : apparent capture cross section) of native defects and impurities in GaN with a level between $E_c - 0.37$ eV and $E_c - 0.8$ eV. (TD = threading dislocations).

Trap	E_a (eV)	σ_{na} (cm ²)	Identification
A _x	0.72–0.8		Associated with TD [15–19]
A	0.65–0.7	$6.8\text{--}17 \times 10^{-16}$	V _{Ga} -related defect [20–25]
B	0.56–0.62	$1.7\text{--}12 \times 10^{-15}$	N _{Ga} or V _{Ga} -related defect [20–22,25–33]
	0.5/0.57/0.72	$-/-/1 \times 10^{-13}$	Fe [34–36]
C	0.41–0.45	$2.8\text{--}70 \times 10^{-14}$	V _N -related defect [16,17,30,32]
	0.38/0.4	$10^{-20}/1.4 \times 10^{-15}$	C [37–39]
	0.37–0.4	$5.2\text{--}8.5 \times 10^{-17}$	Si [40,41]

associated with GaN HEMT degradation during stress experiments [11, 12]. The similarity of these trap features with those of traps E2 and E3 confirms the reliability of the multiple peak fits of DLTS data.

4. Discussion

4.1. Traps assignment

Trap A and B are commonly observed in epitaxial GaN grown by various techniques including reactive molecular beam epitaxy (RMBE)

[22], hydride vapor phase epitaxy (HVPE) [20] and MOCVD [21,23]. Trap A has been ascribed to Ga vacancy (V_{Ga}) -related complexes based on a study with electron irradiation [17]. Trap B has been assigned to N antisite (N_{Ga}) or V_{Ga} and their complexes with impurities [21,43]. Trap A_x has been reported to exhibit a logarithmic dependence with t_p , which indicates that it is associated with extended defects, such as threading dislocations [18].

Table 1 summarizes levels reported in the literature to native defects and impurities in GaN between $E_c - 0.37$ eV and $E_c - 0.8$ eV. Among them, Fe and Si impurities were not used to perform the diodes used in this work and are not expected to be present in the GaN layer. Others authors suggested that oxygen could be involved in a level around $E_c - 0.45$ eV [44,45]. However, Secondary Ion Mass Spectrometry analysis of the GaN layer revealed that the O concentration is lower than the detection limit. Consequently, carbon is the most likely impurity which could be involved in the formation of trap levels since the GaN buffer layer of the diodes is carbon doped.

A negative correlation between the concentration of traps A and B and the carbon content has been established [37,38,46,47]. Furthermore, several groups established a link between a trap at $E_c - 0.40$ eV and the carbon concentration in GaN [37,38,39]. The amplitude of the DLTS peak associated with this trap rises as the carbon concentration in GaN increases [37,38]. A link between carbon-related defects and a trap with $E_T = 0.5$ eV, associated with a positive correlation between the trap concentration and the carbon content, has also been suggested [47,27].

By comparing the peak amplitudes in Fig. 6, we find a similarity between the evolution of the concentration of traps A, B and E1 versus (i) the carbon content, reported in the literature and (ii) the negative

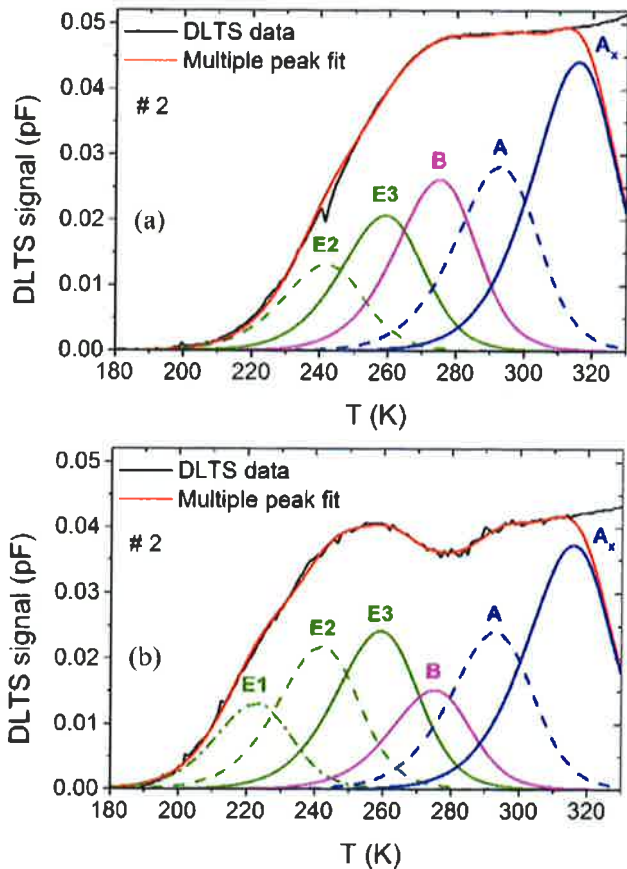


Fig. 3. Multiple peak fit of DLTS data recorded with $V_R = -10$ V, $V_p = 0$ V, $t_p = 1$ ms and $T_w = 1$ s (a) before stress and (b) after stress. The amplitude of trap A_x is over estimated.

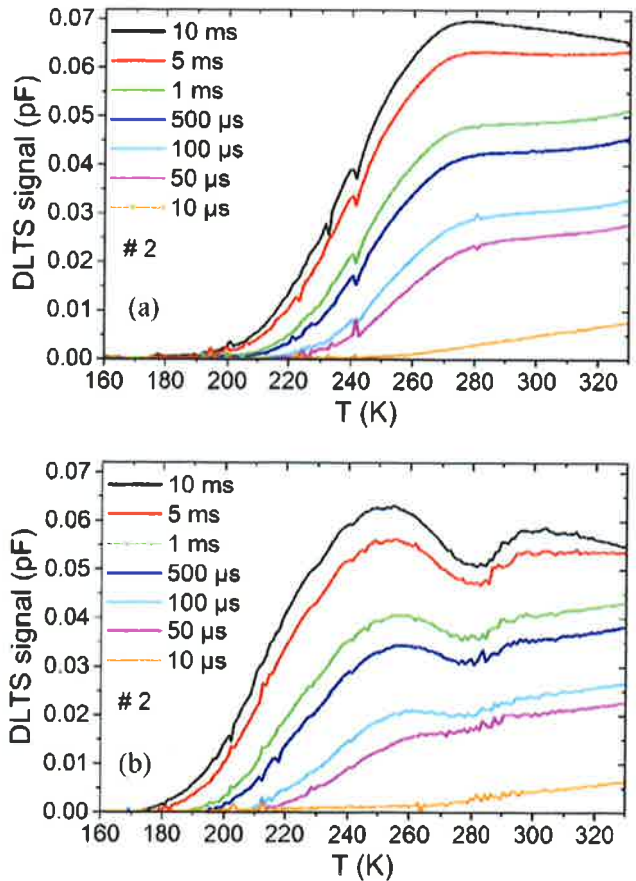


Fig. 4. DLTS spectra of diode #2 recorded with $V_R = -10$ V, $V_p = 0$ V, $T_w = 1$ s and t_p varying between 10 μ s and 10 ms (a) before stress and (b) after stress.

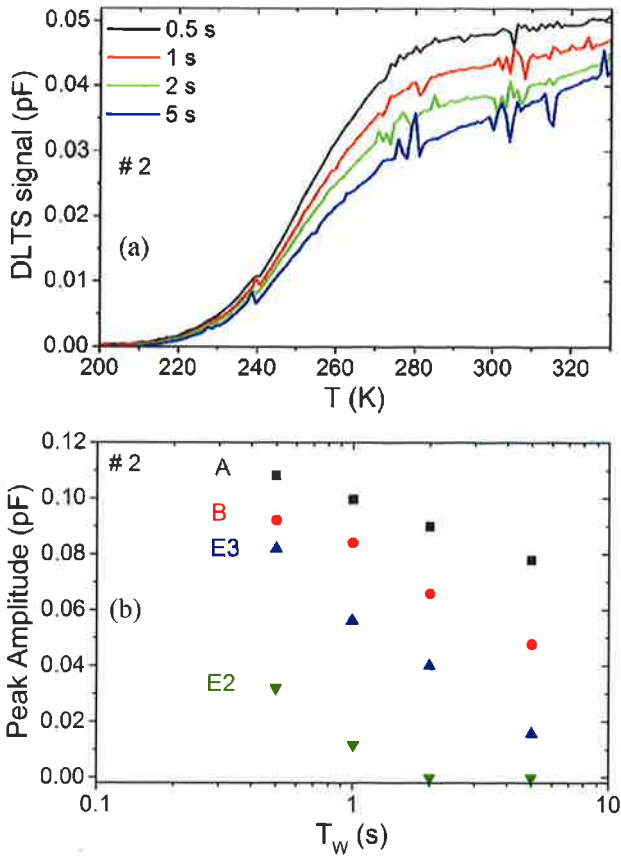


Fig. 5. (a) DLTS spectra of diode #2 recorded with $V_R = -10$ V, $V_p = 0$ V, $t_p = 1$ ms and T_w varying between 0.5 s and 5 s. (b) Peak amplitudes of traps A, B, E2 and E3 versus T_w extracted from multiple peak fits of data in (a).

voltage effect. After stress, traps A and B decrease whereas traps E1, E2 and E3 increase. Consequently, it is expected that traps E1 is associated with carbon-related defects. This result also suggests a link between V_{Ga} involved in traps A and B and carbon impurity.

Fang et al. [42] demonstrated that traps in GaN behave as point defects in thick free-standing material and turn out to behave as line defects in thin epi-layers no matter how the layers where grown and which substrates were used. The logarithmic dependence of the peak amplitudes on t_p in Fig. 6 is consistent with that.

Carbon atoms are known to occupy the nitrogen substitutional site during the growth but this defect acts as an acceptor C_N (0/-) with a level at $E_v + 0.9$ eV [48]. When carbon concentration exceeds that of Si, the formation energy of the Ga substitutional configuration becomes equal to that of the N substitutional site [49]. However, the C_{Ga} (+/0) defect has been attributed by Shah et al. [50] and Armstrong et al. [46] to a level at $E_c - 0.13$ eV and $E_c - 0.11$ eV, respectively. In interstitial position, carbon atoms have been found to form a deep acceptor C_i (0/2-) at $E_c - 1.35$ eV [46,51]. Although the nature of the carbon-related defect

Table 2
Activation energy and capture cross section of traps identified by the multiple peak fits of DLTS data of diodes #1 and #2.

Trap	E_a (eV)	σ_{no} (cm ²)
E1	0.4	8×10^{-17}
E2	0.44	9×10^{-17}
E3	0.5	2.8×10^{-16}
B	0.58	2×10^{-15}
A	0.65	6.3×10^{-15}
A _x	0.72	1.1×10^{-14}

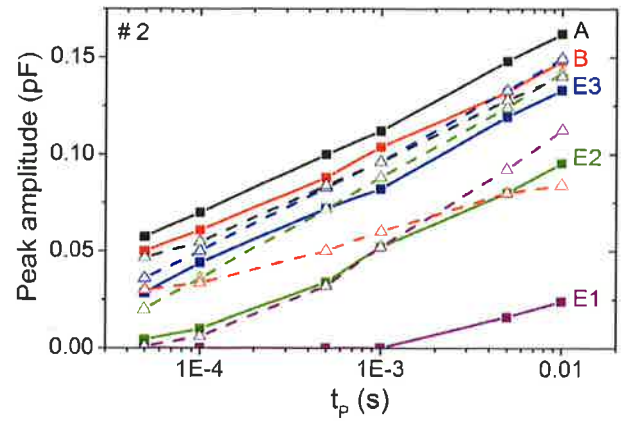


Fig. 6. Peak amplitudes of traps A, B, E1, E2 and E3 versus t_p extracted from multiple peak fits of data in Fig. 4, before (straight lines and filled squares) and after (dashed lines and open triangles) stress.

with $E_c - 0.40$ eV is unclear, it seems unlikely to be associated with C_N (0/-), C_{Ga} (+/0) and C_i (0/2-) defects. Matsubara et al. [52] suggested that the origin of the $E_c - 0.40$ eV level could be the state (0/-) of C_i and/or the state (+/0) of $C_{Ga} - V_N$ based on their theoretical calculations.

In addition, it is worth noting that the change of trap concentrations after a negative voltage stress doesn't affect significantly the sheet carrier concentration in the channel.

4.2. Traps localization

From the C-V data in Fig. 1, we derived the sheet carrier concentration N_{sh} as a function of bias according to the following equation

$$N_{sh} = \frac{1}{e} \int C \cdot dV$$

where e is the elementary charge (1.602×10^{-19} C), C is the measured capacitance per unit area and V is the voltage applied to the Schottky contact. The result is plotted in Fig. 7.

The sheet carrier concentration in the 2-dimensional electron gas channel decreases linearly when the bias change from 0 V to -1 V. In Fig. 8, the quenching of the DLTS signal when V_p is reduced from 0 V to -0.8 V (detection from the channel region to the buffer layer) is probably linked to the sheet carrier concentration reduction. However, the evolution of the amplitude of each peak versus the filling pulse

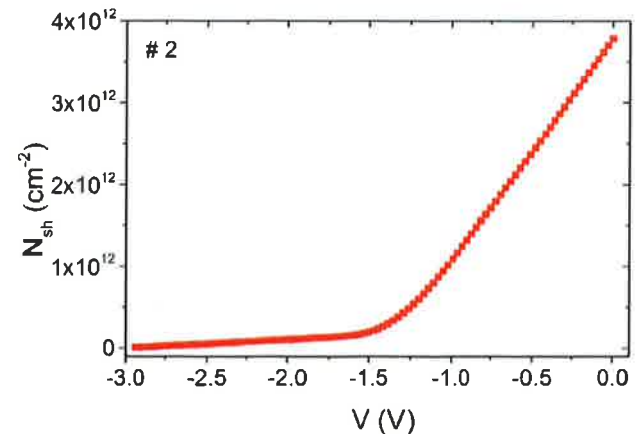


Fig. 7. Sheet carrier concentration extracted from C-V data (Fig. 1) of the SBD #2 at 300 K versus the applied voltage.

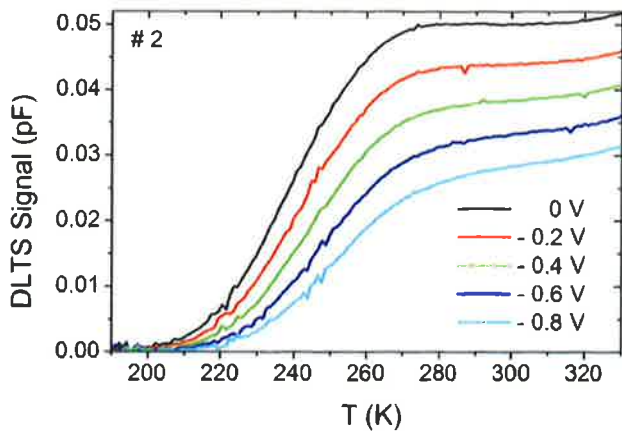


Fig. 8. DLTS spectra of diode #2 recorded with $V_R = -10$ V, $t_p = 1$ ms, $T_w = 1$ s and V_p varying from 0 to -0.8 V.

height reveals that the concentration of trap E2 decreases more rapidly as the probe zone moves further from the GaN surface (Fig. 9). Then, we conclude that trap E2 is mainly located in the channel region, close to the AlN/GaN interface.

The reverse bias $V_R = -10$ V corresponds to a space charge region width of several hundreds of nanometers. So, a large part of the DLTS probe zone is in the carbon doped GaN buffer layer. Therefore, trap E2 seems not carbon-related since it is mainly located in the channel which is free of carbon.

5. Conclusion

We demonstrated that a negative voltage stress of -600 V changes the trapping properties of the GaN layer in AlGaN/GaN SBD. After stress, a decrease in the concentration of traps A and B and an increase in the concentration of traps E1, E2 and E3 are observed. Traps E1 is expected to be carbon-related defects whereas trap E2, mainly located in the channel, seems not carbon-related. The low change in trap concentrations found after stress indicates that the modification of the trapping properties could not be significantly responsible for the reduction of the sheet carrier concentration in the channel. Consequently, electron traps with an activation energy above $E_C - 0.7$ eV and located in the top of the GaN layer are not relevant to explain a current reduction at room temperature of AlGaN/GaN power devices which have undergone a negative voltage stress.

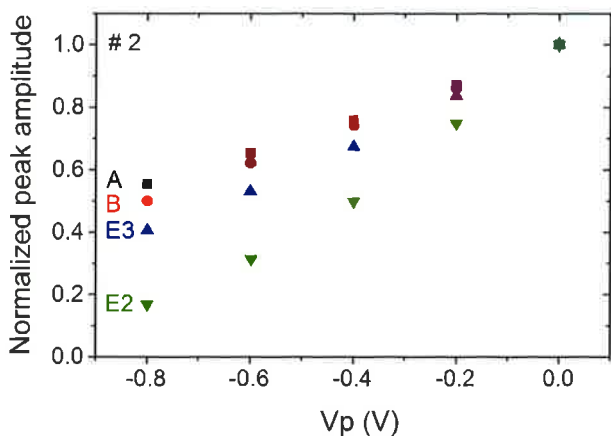


Fig. 9. Filling pulse height dependence of the trap DLTS signal extracted from multiple peak fits of data in Fig. 8.

Acknowledgments

The first author thanks Matthieu Nongailard and Stéphane Bécu for assistance in stress experiments.

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