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Radiation Hardened by Design Pipeline Analog-to-Digital Converter Blocks in CMOS HV 0.18 μ m Technology

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Abstract

In this paper, we present an approach to achieve radiation hardening by design (RHBD) for the main three blocks involved in pipelined Analog-to-Digital converters (ADCs): switches, comparators and residue amplifiers. A method to design bootstrapped switches has been devised to avoid voltage overshoots. Dual path with auto-zero techniques have been implemented for the comparators to be less prone to single effect upset (SEU). Finally, predictive switched capacitor techniques have been used for the residue amplifier in order to benefit from a simpler low-power amplifier architecture. To verify the proposed methodology, these blocks were implemented in an HV 0.18 μ m CMOS technology.

I. INTRODUCTION

CCD sensors embedded in satellites need not only to convert analog signals into digital ones with high precision and speed (11-14 bits at 5-20 MS/s) but also to be radiation hardened due to the space environment. To achieve such performances, pipeline analog-to-digital converters (ADCs) are usually employed.

The pipeline ADC is an N-step converter consisting of M stages connected in series with a few bits being converted by each stage. Usually a 1.5-bit or 2.5-bits resolution is preferred for the most significant bit stages as it allows efficient digital calibration techniques to be performed. Fig. 1 shows a classical 1.5-bit stage architecture.

As shown in Fig. 1, ADC performance relies on switched-capacitor (SC) techniques. In such SC circuits, CMOS switches, comparators and amplifiers are critical components and their characteristics directly affect the linearity, the bandwidth and the power consumption.

Regarding CMOS switches, bootstrapped structures similar to [1] are often used. This technique allows not only to use the switch with low-voltage power supply but also lessen signal distortion by strongly reducing its signal-dependent On resistance. Such an improvement is obtained by keeping constant the switch overdrive voltage independently of the signal input voltage. Further, in order to eliminate the remaining non-linearity induced by the body effect on the MOS transistor threshold voltage, different methods were proposed such as by applying a controllable input signal factor to the gate of the main switch [4] or by biasing techniques of the body if the technology process allows it. In addition to the previously mentioned advantages of such bootstrapped architectures, charge injection effects due to the

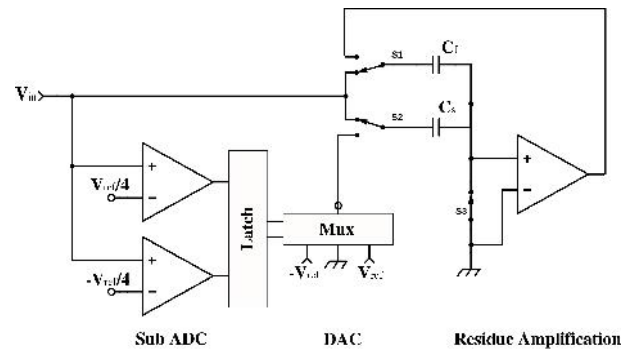


Figure 1: Pipeline stage with 1.5-bit resolution

carrier release when the MOS transistor switch is turned off, are also significantly reduced since they are less dependent on the input signal voltage to be sampled. However, to maintain a proper overdrive voltage across the gate of the MOS transistor switch, voltage higher than the maximum power supply voltage are applied. Even if the previously mentioned bootstrapped techniques also aim at maintaining CMOS process stress as low as possible, it might not be sufficient to ensure that the switch can withstand a radiative environment. In particular, three main radiation effects should be taken into account carefully: total ionizing dose, latch-up and single event gate rupture SEGR [2]. In this paper, an approach to avoid voltage overshoot greater than the power supply will be presented.

As far as the comparators are concerned, an auto-zero dual path approach has been implemented so that the architecture could be less prone to SEU [3].

Finally, to achieve high linearity, class AB high-gain amplifiers are usually employed. To enhance the amplifier open-loop gain, more or less complex architecture based on cascading techniques with two or more stages can be used. Such an inherent architecture complexity not only induces higher power consumption but also a lower reliability regarding radiation. It can thus be interesting to use SC gain-enhancement techniques to benefit from a simpler low-gain amplifier structure [4]-[6]. Here, to demonstrate such an approach in a radiative environment, a predictive technique based on correlated double sampling (CDS) has been used to reach a 66dB open-loop amplifier based on a 46dB open-loop gain amplifier.

II. PROPOSED RHBD APPROACHES FOR AN ADC PIPELINE STAGE

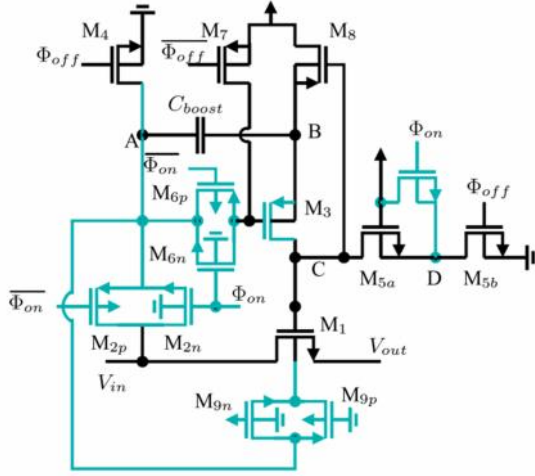


Figure 2: Proposed Bootstrapped Switch Schematic (proposed improvements in lighter tone)

A. Bootstrapped Switches

The proposed bootstrapped switch is shown in Fig. 2 where the modifications are highlighted to facilitate the comparison with a conventional bootstrapped switch. In order to use bootstrapped switches in a radiative environment, the following voltages should remain within the technology specifications (and for safety margin usually the maximum differential voltage is set to V_{dd}) at any time:

- the gate-body voltage V_{gb}^{M1} of M1. This implies that the body cannot be tied to ground but should depend on V_{in} .
- the gate-source voltage V_{gs}^{M1} of M1. A careful design should take into account the worst case with $V_{out}=0$ at the beginning.
- the V_D voltage is not accurately controlled and might be higher than V_{dd} (V_{gd}^{M5B}).
- the drain-body voltage V_{db}^{M5A} of M5A.

As in [7], the body of M1, M2 and M5 are thus tied to the source in order to alleviate voltage stress. However, those changes do not guarantee that all the voltages are lower than V_{dd} all the time. As explained in [8], the worst case corresponds to $V_{in}=V_{dd}$ and $V_{out}=0$. To ensure that V_{CA} is always lower than V_{dd} , the change rate of V_C should match the one of V_{out} . It was shown that the maximum change rate of the gate voltage of M1 can be expressed as follows:

$$\left. \frac{dV_{GM1}}{dt} \right|_{\max} = \frac{V_{dd}}{M1}$$

where the time constant $M1$ is related to the charge of the gate of M1. The size of M3 should be subsequently well defined and a method to estimate its size has been devised in [8]. Further, when the switch is turned off, the voltage change rate of the body of M1 should match the gate voltage change rate. The simulation results (Fig.3-4) highlight the importance of the size of M3.

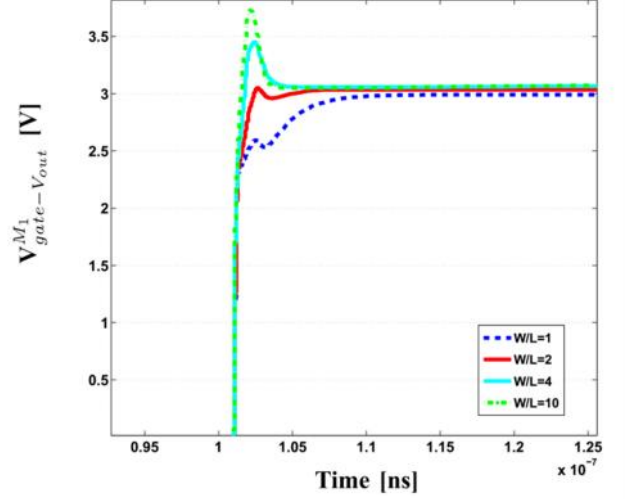


Figure 3: Simulated $V_{M1}^{gate} - V_{out}$ voltage for different size of M3

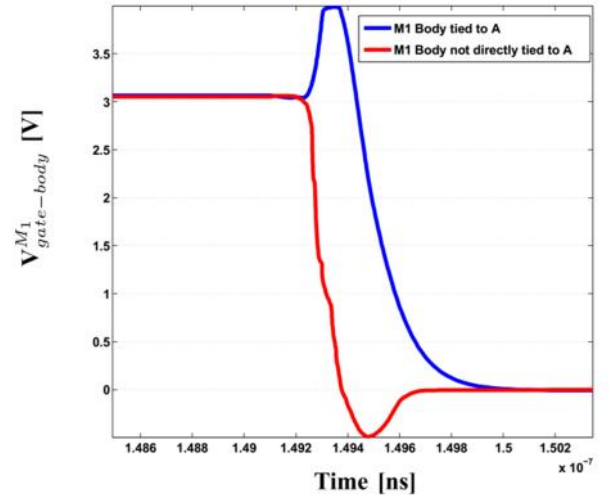


Figure 4: Simulated $V_{M1}^{gate-body}$ voltage with and without M9

B. Dual Path Comparator

To obtain a wider dynamic range, higher noise rejection, improved matching, and/or reduced power dissipation relative to their single-ended continuous-time counterparts, it is interesting to use differential switched-capacitor topologies [9]. A typical switched-capacitor CMOS comparator as commonly used in pipelined analog-to-digital converters consists of a capacitive input sampling/subtraction network, a pre-amplifier, and an output latch. These circuits compare an input voltage to a reference voltage and latch a logic '1' or '0' at the output depending on whether the input voltage is higher or lower than the reference voltage. Switched-Capacitor circuit topologies exhibit much greater single-event vulnerability than their continuous-time counterparts due to the presence of floating nodes in the signal path. Since floating nodes do not have any charge dissipation path, the charge deposited on a floating capacitor by a single-event strike remains until the next clock phase at least. We have implemented the radiation hardened approach proposed in [10] that aims to reduce the bit error rate of a comparator operating in a radiative environment (Fig.5). It relies on a dual

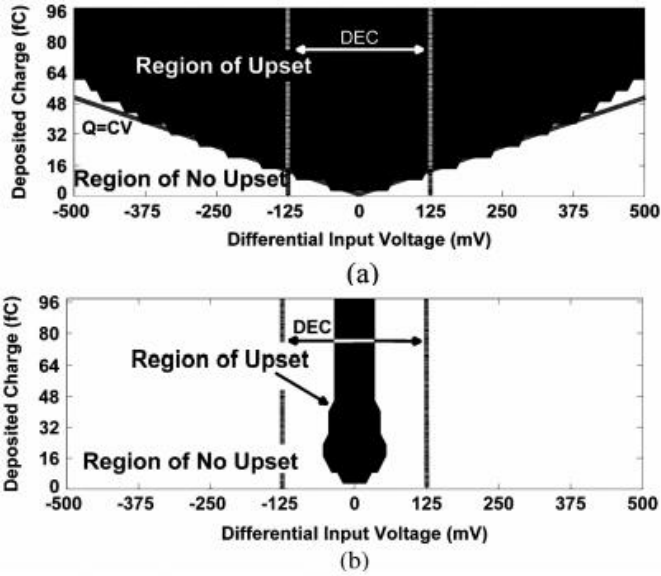


Figure 5: Simulated contour plots of differential pre-amp input voltage vs. deposited charge for (a) standard switched capacitor design and (b) dual path auto zero comparator [3].

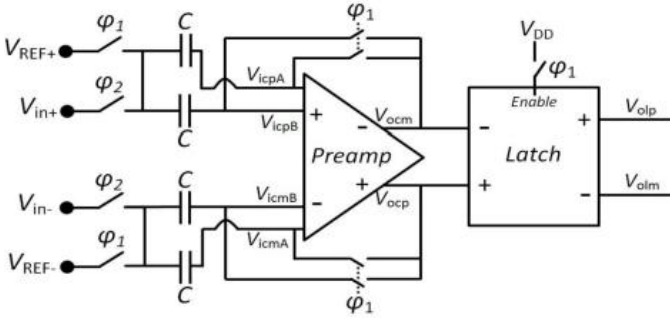


Figure 6: Auto-zero comparator with dual-path hardening around the preamplifier

path design technique to reduce the vulnerability of floating nodes in the switched-capacitor input network of the comparator. Furthermore, it has been shown that an auto-zeroing comparator design can limit the upset duration to a single clock cycle between reset phases [10]. An auto-zero approach has thus been added up to reduce both the upset duration and the comparator offset (Fig.6).

C. Predictive Residue Amplifier

In order to improve further the reliability of the main stage amplifier and reduce its power consumption, a predictive amplifier based on a fully differential class AB one-stage amplifier architecture was chosen and designed instead of a very high gain two/three stages amplifier. Fig. 7 shows the amplifier without the capacitive common mode feedback loop. Fig. 8 depicts the gain enhancement principle applied to the SC amplifier while Fig. 9 shows the required phases. During the first phase, the input voltage is sampled onto all the capacitor C_1 - C_4 . An estimation is then provided in the second phase. Finally, the last phase provides the residue amplification output.

The residue amplifier error can be significantly reduced and expressed as follows:

$$v = \frac{-1}{A_{0^2}} \left(G_i^2 + \left(\frac{C_{tot}}{C_4} \right)^2 + \frac{C_{tot}}{C_4} G_i \right)$$

where A_0 is the open-loop gain of the amplifier, $C_{tot} = C_i$ and $G_i = (C_1 + C_2)/C_2 = (C_3 + C_4)/C_4$ the desired residue amplification value. Table 1 summarized the performance that can be achieved by this gain enhancement architecture for different amplifier open-loop gains and closed-loop gains.

Here, the native gain of the designed amplifier is 46dB and the overall gain enhancement is approximately 20dB, which improves the accuracy of the pipeline stage by 2-bits.

Table 1: Estimated Error with and without gain enhancement

Amplifier Gain	40 dB		60 dB	
	Without	With	Without	With
1.5-bits stage	$\epsilon = 3\%$	$\epsilon = 0.28\%$	$\epsilon = 0.3\%$	$\epsilon = 0.003\%$
2.5-bits stage	$\epsilon = 5\%$	$\epsilon = 1.1\%$	$\epsilon = 0.5\%$	$\epsilon = 0.011\%$

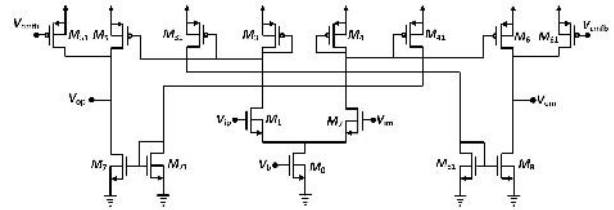


Figure 7: Class AB amplifier

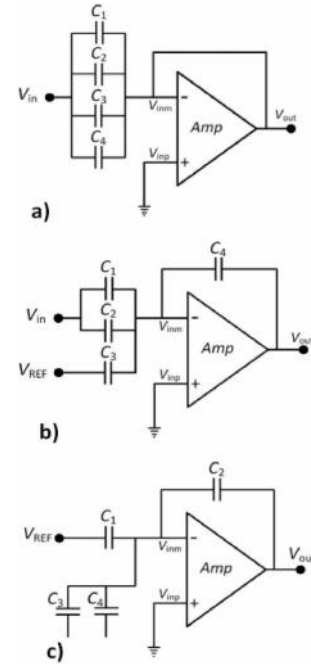


Figure 8: Predictive switched-capacitor residue amplifier: (a) Phase1: sampling, (b) Phase 2: predictive amplification and (c) Phase 3: residue amplification

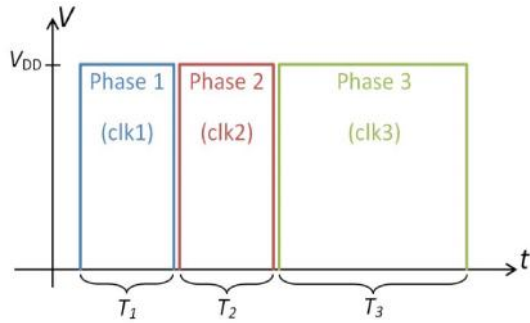


Figure 9: Phases for the gain enhancement: 1 sampling, 2 prediction (or estimated output) and 3 residue amplification.

III. CONCLUSION AND PERSPECTIVES

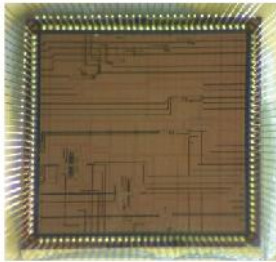


Figure 10: Die photograph of radiation Hardened pipeline ADC blocks in 0.18 μm HV CMOS technology

To validate the performances given by simulation results, a bootstrapped switch and a classical one, an auto-zero comparator with dual-path hardening and a classical one, a predictive rail-to-rail amplifier based on a CDS approach and a single rail-to-rail amplifier, have been implemented in a 3.3V 0.18 μm HV CMOS process (Fig. 10). The test bench to measure the blocks performances is still under development.

Other gain enhancement techniques should be assessed in future implementations such as correlated level shifting and iterative gain enhancement approaches in order to achieve even higher amplifier open-loop gain, lower noise and lower power consumption and lower amplifier architecture complexity.

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