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# Channeltron Detector Readout ASIC in 0.35 $\mu\text{m}$ HV CMOS for Cold Solar Wind Analysis

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**Abstract:** *Low-power analog front-end circuits for channeltron detectors (or Channel Electron Multiplier: CEMs) have been fabricated in 0.35- $\mu\text{m}$  CMOS technology to characterize low energy solar wind particles. They have been designed to readout signals for incident charges ranging from 50 fC to 20 pC. Each front end circuit consists of a charge preamplifier, an amplifier, a discriminator, a monostable circuit and a LVDS. Requirement on the complete front end is to consume less than 6.5 mW/channel for a maximum event detecting rate of 40 MHz.*

## I. INTRODUCTION

THOR (Turbulence Heating ObserveR) is a microsatellite aimed to investigate the fundamental theme “turbulent energy dissipation and particle energization”. It embarks among other instruments CSW instrument (Cold Solar Wind) which is primarily dedicated to the study of solar wind turbulence at the ion scale. The  $\text{He}^{++}$  solar wind population will be measured within the energy range of [20 eV/q – 20 keV/q]. To fulfill the requirements, the CSW instrument can be divided into two main units: the detector unit and the electronics unit. Our work is part of the detector unit comprising of a deflector, a collimator and a top-hat electrostatic analyser. Through this analyser, the energy-per-charge selected ions are focused onto the main detection plane consisting of 32 channel electron multipliers (CEMs) or channeltrons. The CEMs’ output charge (approximately  $10^7$  electrons) is collected and read-out by two 16-way ASICs for signal processing and discrimination. A prototype of the front end circuit is presented here. It consists of three ways of achieving the required performance: “cluster A”, “cluster AB” and “cluster RAB”. Each one of the design has been characterized electrically on a test board.

## II. ASIC DESIGN

The incoming charges provided by the CEM detector is firstly integrated in a charge sensitive pre-amplifier (CSA) and then further amplified without being “shaped” for “cluster A and “cluster AB” designs. The following signal processing consists of binary readouts based on comparators that detects the incoming particle if the amplified output signal amplitude is above a preset threshold [1], a monostable and finally an LVDS output driver.

Here, the targeted operating frequency is 40 MHz (which corresponds to detect one event every 25 ns) while consuming less than 6.5 mW/channel.

### A. CEMs Analog Front end architectures

Due to the low power and high speed requirements, as previously mentioned, three different architectures were designed: “cluster A”, “cluster AB” and “cluster RAB” (see Fig. 1). They were named according to the amplifier operating class, either A or AB. The cluster A relies on a conservative design which is used as reference for the cluster AB and RAB.

Note that the class A provides the lowest noise while the class AB the lowest power consumption. In addition to further reduce the power consumption and achieve higher speed, the pulse shaper stage has been replaced by an amplifier stage for the cluster A and AB while it is not necessary in the cluster RAB.

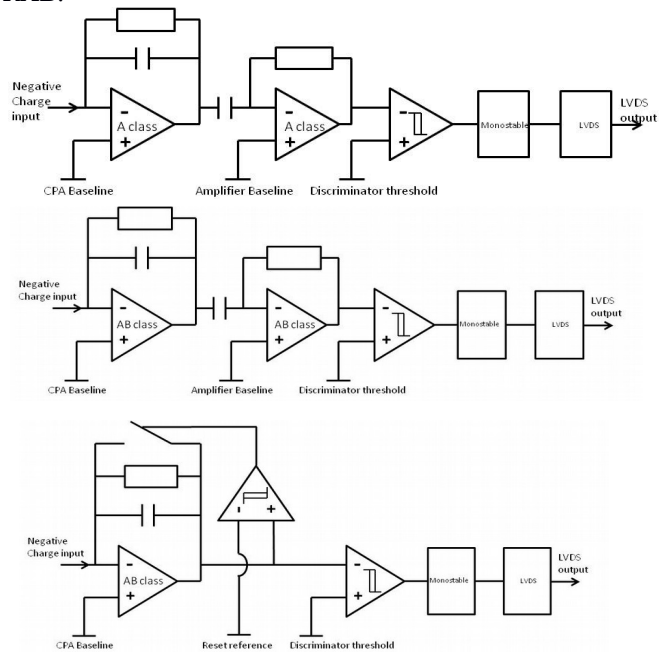


Figure 1: Front End simplified schematic: (a) cluster A, (b) cluster AB and (c) cluster RAB.

### B. CSA architectures

All the channels make use of a RC CSA for integration of the input charge. The CSA is based on a transconductance amplifier (OTA) with a feedback capacitor  $C_f$  to perform the charge integration and a resistor feedback  $R_f$  to discharge  $C_f$  and to provide a DC path for the detector leakage current. Such a differential approach improves the rejection of common mode external noise. In addition, based on the methodology extensively described in [1], sizing as well as biasing of the transistors are optimized for internal noise and bandwidth performance. The feedback  $R_f$  and  $C_f$  values depend on the required time constant.

One of the challenging requirement is on the pulse repetition rate at 40MHz (every 25ns) while the input event may last up to 13ns. The electronic needs to be fast enough to closely follow the rise of the current input pulse. It also needs to limit its discharge time in order to be quickly ready for the next pulse.

The gain bandwidth product has been evaluated to be no less than 600MHz [2] and the chosen approach for a fast recovery time is to limit the integration time ( $R_f C_f$ ) to 1ns, this value proves to be a good compromise between gain loss and recovery speed at the CPA output.

The dynamic range spanning from 50 fC to 20 pC, it becomes essential to limit any overshoot of the signal especially at 20 pC input charge as the overshoot would be treated as an incoming small event. As a result, the CSA amplifier is a first order amplifier consisting of one OTA stage only. The conservative "cluster A" channel makes use of a conventional class A amplifier while class AB amplifiers are used to boost up the performances without increasing the quiescent current for "cluster AB" and "cluster RAB" channels. Super class-AB OTAs with adaptive biasing have been designed to provide a dynamic output current scaling.

In order to further reduce power consumption, cluster RAB forces the discharge of  $C_f$  before signal saturation. This allows making even more power efficient design choices. This channel does not need another amplification stage as it is the case for the previous two designs

### C. Layout considerations

The circuit has been implemented in AMS 0.35 $\mu$ m HV CMOS technology. This technology has a triple well option allowing isolation of transistors from the bulk. This is an advantage in terms of noise and crosstalk reduction. To further reduce crosstalk, power supply of the analog part of the channel is isolated from the discriminators (comparators, monostable) and LVDS outputs. A microphotograph of the chip layout is shown in Figure 2.

A total of 9 channels are integrated in the chip: 3 channels per cluster type in order to check cross-talk effects.

### III. ASIC CHARACTERIZATION

The ASIC has been electrically characterized on a test board. A 1-nF injection capacitance driven by a signal generator has been used to generate the input charge. The ASIC input is loaded by a 10-pF capacitance representing the parasitic capacitance of the detector with its ESD protections.

The Table I summarizes the measurement results.

Table 1: Measurement Results

Parameter	Spec	Cluster A	Cluster AB	Cluster RAB
Power (mW)	<6.5	14.5	6.25	4.2
Qmin (fC)	50	50	60	50
Qmax (pC)	20	>20	>20	>20
Linearity range (fC)	50-800	50-1100	60-1000	50-2000
Frequency (MHz)	40	40	40	20

### IV. CONCLUSION

A CEM detector readout ASIC for Cold Solar Wind has been presented. Two of the designs ("A" and "AB") feature double separation pulse of 25ns for input charges spanning from 50fC to 20pC for a 10pF input parasitic capacitance. Power consumption are 14.5mW and 6.25mW per channel for each design. The last design "RAB" consumes 4.2mW per channel for a detection rate of 20MHz only.

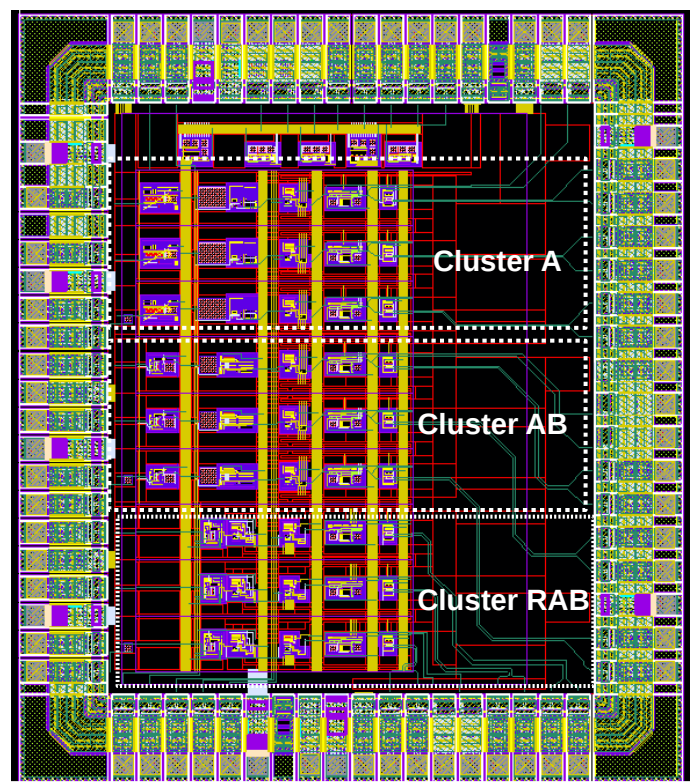


Figure 2: readout ASIC layout

### V. REFERENCES

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