Digital architecture for vibrating inertial sensors: modularity, performances, self-calibrations

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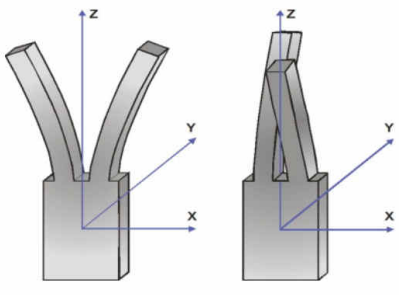
Abstract

This paper presents a fully integrated inertial instrument composed of a vibrating sensor and a Field-Programmable Gate Array (FPGA) device. This digital architecture ensures the electronic driving of the resonator and its response measurement in a reduced space. The current FPGA performances allow to easily adjust frequency, phase and magnitude of the excitation respectively better than 1 µHz, 10 µrd, and 0,01 % of full scale. Therefore, this architecture is especially suitable to the use of feedback-control loops. The instrument is connected to an On Board Computer by serial communication. The performances obtained with this architecture are 0,8 µg bias instability, 60 µg of residual thermal bias stability for the accelerometer, 1 °/h bias instability, and 0,03 $°/\sqrt{h}$ angular random walk for gyroscope.

1. Introduction

The sensors to be interfaced with this electronic are preferably resonators, thanks to the accurate resonance drive capability of the DDS oscillator inside. Especially in the case of inertial sensors, this architecture is convenient for both Vibrating Beam Accelerometers (VBA) and Coriolis Vibrating Gyroscopes (CVG).

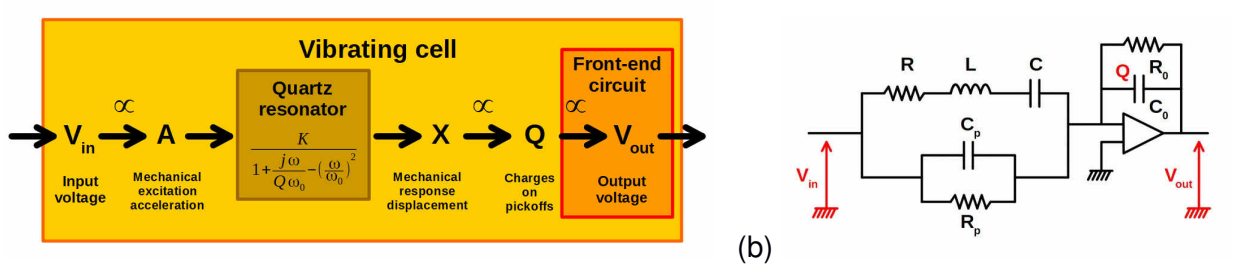
The ONERA gyroscope (see Figure 1 (a).) is a mechanical tuning-fork structure, which can be modeled by a two dimensions oscillator [1, 2]. It has two main perpendicular vibrating modes, in plane and out of plane (see Figure 1 (b).). The first one is electronically excited at its resonance, and the second is actuated by Coriolis effect to measure the angular rate of the sensor. The ONERA accelerometer (see Figure 1 (c).) is based on a micro vibrating beam driven at resonance, and attached to a proof mass. Under an external acceleration the mass pulls the beam and induces a resonance frequency shift. By tracking this resonance, the system then delivers a digital image of the input acceleration.

(a)  (b) 

(c) 

Figure 1. (a) Gyroscope head. (b) tuning fork in-plane (Drive) and out-of-plane (Sense) modes. (c) Accelerometer head.

The piezoelectric characteristics of quartz structures allow converting their oscillations from mechanical to electric domain. Indeed, the excitation force is proportional to the voltage applied on the electrodes, and in-phase and quadrature components of the displacement are proportional to the amount of charge accumulated on pickoffs electrodes. To adapt the output scale and dimension to the input, an integral amplifier on proximity circuit convert charges into voltage. Finally, the resonator is seen as a fully electronic component, voltage-voltage transfer function, equivalent to a Butterworth Van Dyke model (see Figure 2.). Every resonator following those conditions can be interfaced with the digital architecture board described in section 3.



(a) (b)

Figure 2. (a) Electromechanical resonator. (b) Butterworth Van Dyke model.

The mechanical transfer function is a second order low-pass filter, with a high Q factor. Because the measurement is concretely realized by in-phase and quadrature components of the sinusoidal signal, a suitable representation of the response of the resonator is the Nyquist diagram.

There are two kinds of curves. Steady-state oscillation amplitudes are represented by varying excitation frequency (see Figure 3.). Because of the high value of the Q factor and normalization at resonance, amplitudes are negligible at low and high frequencies. Close to the resonance, it is well known that the Nyquist path of steady-state points is a circle. In addition, transient curves can also be plotted (see Figure 3.). For example, starting from rest and applying the sine excitation at a given frequency close to resonance will make in-phase and quadrature components follow a defined curve, converging towards the corresponding steady-state point on the circle.

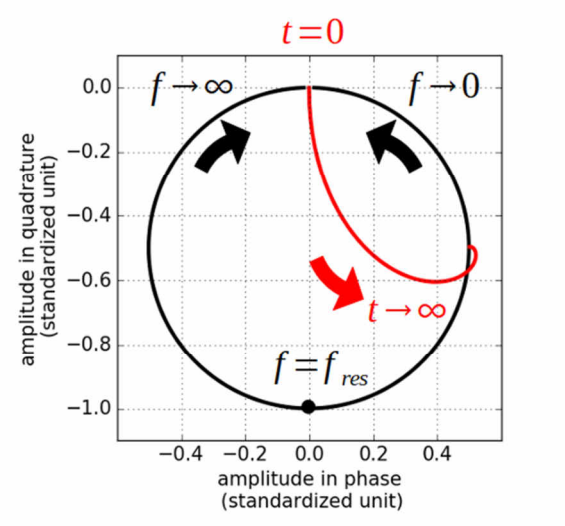
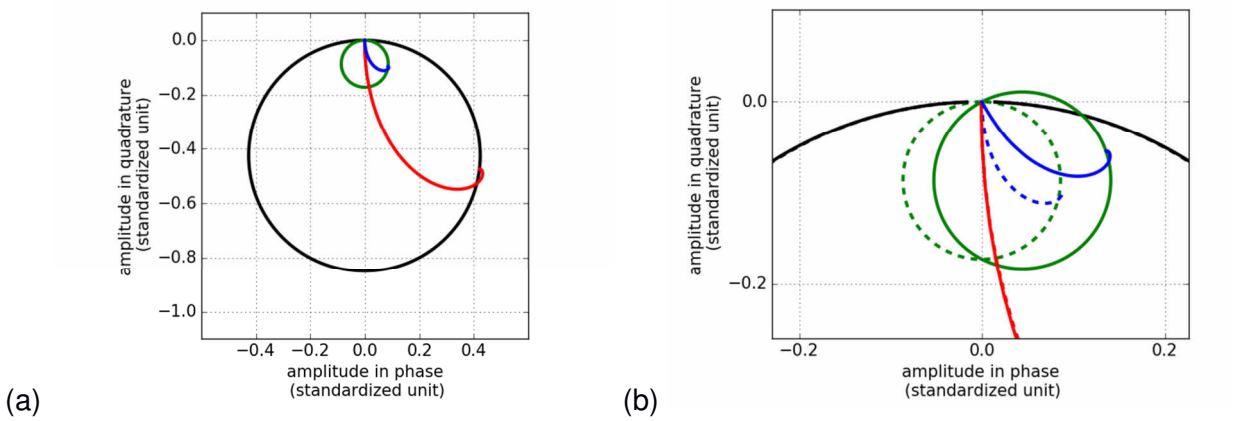


Figure 3. Nyquist representation of transfer function: steady-state (black) and transient (red).

In the accelerometer, the resonator is maintained at resonance by controlling the frequency, from which the inertial measurement is derived. In the gyroscope, two resonators are involved, so that two curves are simultaneously represented, for drive and sense modes. The two steady-state circles are proportional (see Figure 4 (a).), the sense mode circle being modified when external angular rate is applied to the sensor (see Figure 4 (b).). Thereby the gyroscopic measurement is performed by dividing sense amplitude by drive one.



(a) (b)

Figure 4. (a) Gyroscope steady-state responses (Black: Drive state for all excitation frequencies, Green: Sense steady-state) and transient responses (Red: Drive transient from rest to excitation close to resonance, Blue: Sense transient). (b) Gyroscope responses under inertial rotation (zoom on Sense circle)

2. Digital electronics on FPGA

These cells are connected to the Field Programmable Gate Array (FPGA) digital architecture through minimalist analog circuits, reduced to basic filters for digital-to-analog

and standard comparators for analog-to-digital (Figure 5 (a).). All other operations are performed inside the FPGA (Figure 5 (b).). The main advantage concentrating all calculations in a single chip is the development of portable algorithms written in a standardised language such as VHDL, suitable to most programmable devices. This digital part of the instrument is managed by serial communication with On Board Computer (OBC), processing commands of frequency, amplitude, and phase shift changes of the excitation signal. The analog response is then demodulated to obtain digital samples (Figure 5 (c).).

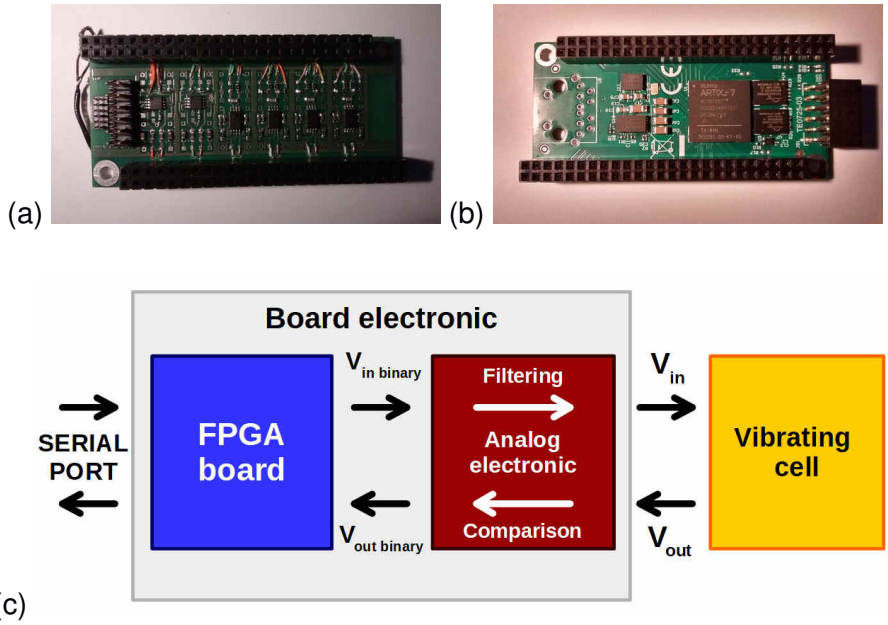


Figure 5. (a) Analog board. (b) FPGA board. (c) Functional behavior of digital interface.

The following sections detail the three main features developed and programmed inside the FPGA board, in VHDL for low level calculations requiring accurate synchronicity, and embedded C for more complex, system level operations.

2.1. Direct Digital Synthesis

Generating signal for excitation by specifying frequency, phase and amplitude is the first function of the FPGA. Logical material is particularly suitable to synthesize an accurate frequency. The core component of such a synthesizer is a phase accumulator with a fast clock source (250 MHz). The output instantaneous phase is then a periodic sawtooth wave (Figure 6 (b).), for which the frequency is proportional to its slope, and thus to the input phase increment accumulated at each sampling time. This principle is usually represented by a DDS Phase wheel (see Figure 6 (a).). Thereby, the frequency resolution is only

dependent on the number of bits used for the phase increment word, whereas the clock frequency remains unchanged.

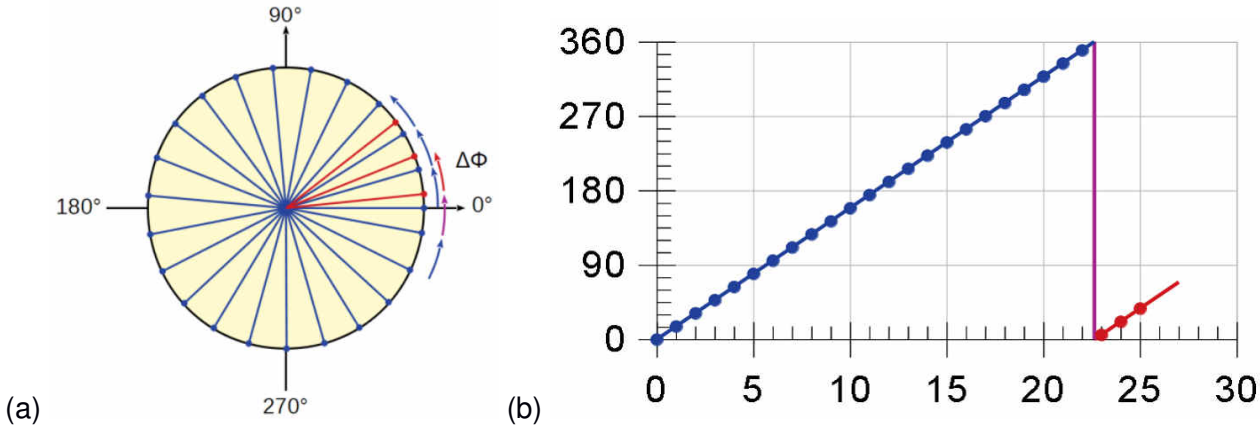


Figure 6. (a) DDS Phase wheel. One phase turn may not be necessarily an integer multiple of the phase increment, allowing fine frequency resolution. (b) Periodic phase signal.

Next, the instantaneous phase generated is used as input address of a Look Up Table (LUT), where the output waveform is stored.

2.2 Sigma-Delta modulation

The modulation function transforming digital waveform to analog one is essential for the excitation of the resonator [3]. A sigma-delta algorithm has been implemented in VHDL to first convert the sampled sine wave into a binary signal getting out of the FPGA (see Figure 7 (a).). The spectrum of the binary signal actually contains nothing but the spectral line of the desired sine wave by almost three orders of magnitude(see Figure 7 (b).). High frequency spurious harmonics are easily wiped out by passive RC filtering, thanks to the ratio of 1000 between the sampling and the target frequency.

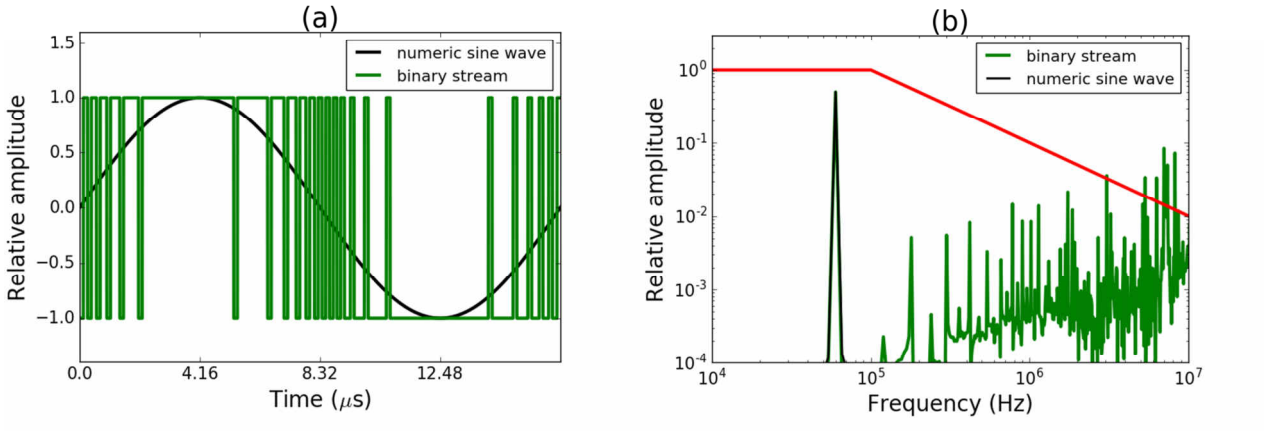


Figure 7. Sigma-Delta modulation. (a) Sine wave and binary stream. (b) Corresponding spectrum. The signal of interest (sine wave) is easily separated from the binary stream harmonics with a passive filter.

2.3. Time to digital Conversion

Analog signals from the resonator need to be acquired back into the FPGA. This can be achieved without Analog-to-Digital Converters, using simple comparators. The FPGA generates a reference sine wave provided by a second synthesizer, parallel to the excitation generator. Comparisons between the resonator response and this reference provide crossing events sampled by the internal system clock, which finally lead to a set of phase values with respect to the reference (see Figure 8.). It has been demonstrated in a recent patent [4] that this measurement is sufficient to reconstruct the response signal into the FPGA by calculating the in-phase and quadrature components. As well as for the feedback control, these low level calculations are performed in a synthesized processor inside the FPGA, much more suitable to complex operations than hardware VHDL resources.

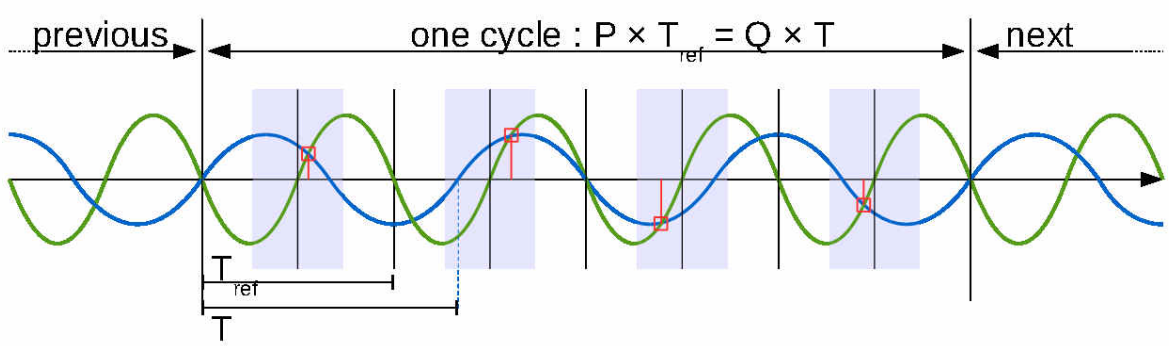


Figure 8. Measurement cycle with reference signal (green) and measured signal (blue). The red crossing events form a periodic wave over the cycle. On this example, P=4 and Q=3.

The resolution of theese phase values is mainly constrained by the sampling and the quantification of digital signals. As seen before, the quantification resolution for an instantaneous phase signal is not critical, because it corresponds to the number of bits used in DDS, which can be easily chosen up to 64 without disturbing FPGA calculation. The sampling rate deserves more carefulness. Currently, the internal clock frequency is equal to 250 MHz, which is close to the maximal rate allowed by the FPGA to respect slack time condition and gates characteristics. Despite this limit, crossing events time stamping resolution can be further improved using available phase shifted outputs of the system clock (see Figure 9.). Thus, each clock period is divided into 8 parts called sub-clocks. When a comparison event occurs, instantaneous phase from DDS accumulator is memorized, as well as the sub-clock index used to add the corresponding fractional part of the phase increment word. Finally, time stamping is achieved by a virtual 2 GHz clock system.

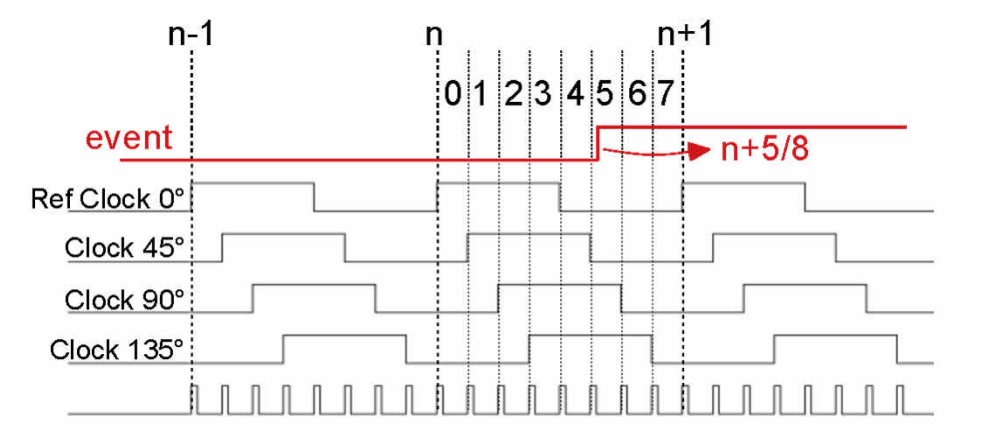


Figure 9. Sub-clock tree to improve time resolution. The equivalent dating clock is 2GHz, although it is not directly achievable on the FPGA gates.

3. Driving and calibration platform

3.1 Full control

A Python platform has been developed to drive the whole inertial instrument with its digital architecture (see Figure 10.). Commands are sent by serial communication, to adjust frequency, phase shift and amplitude of the excitation signal. Besides, data frames with amplitude values are continuously received from the FPGA, essential to realize a real-time inertial measurement. Next, the platform uses a Qt graphical interface, with a command panel to send commands, and a set of graphics to display curves representing the resonator state and inertial measurement (see Figure 11.).

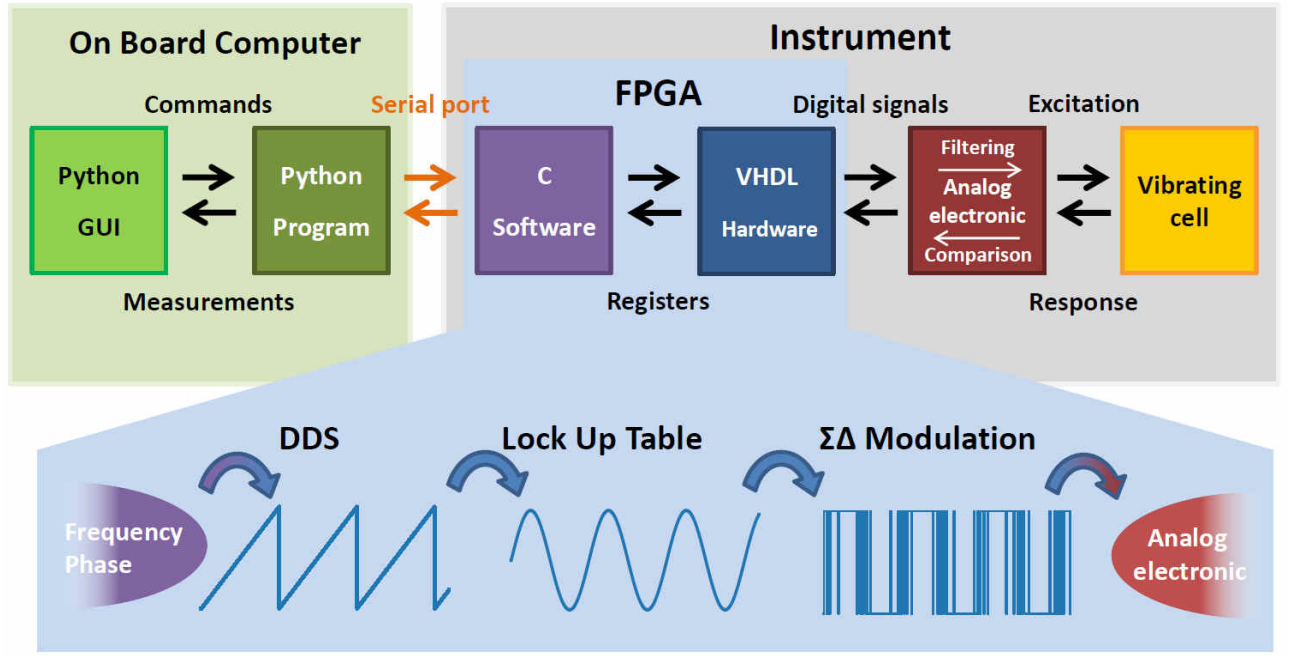


Figure 10. Full chain system

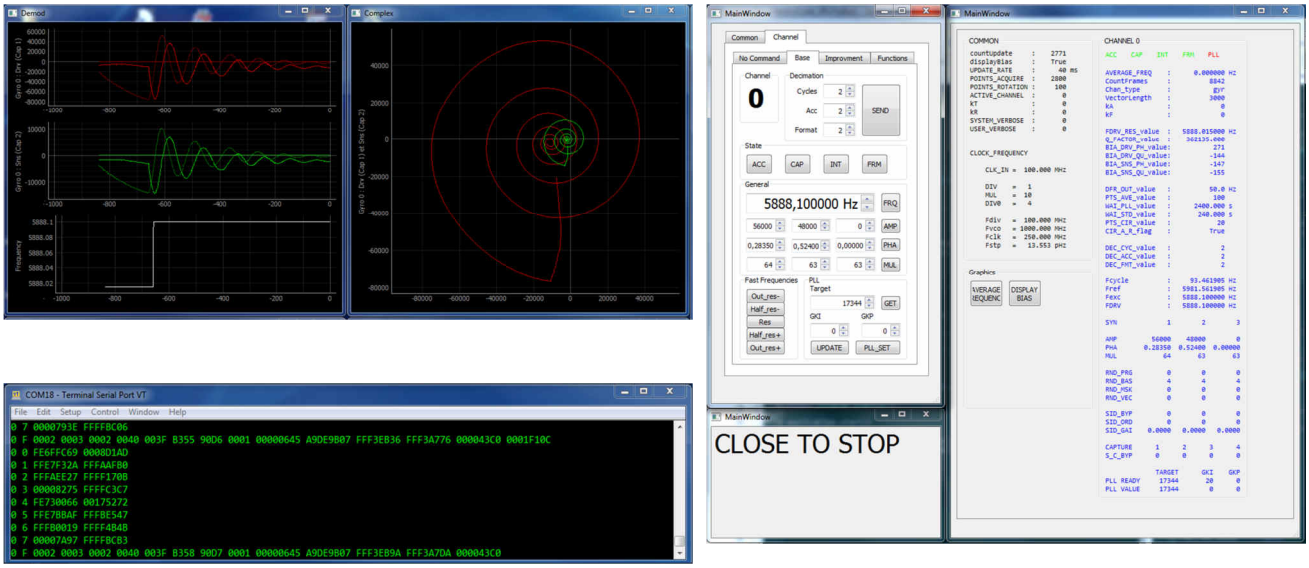


Figure 11. Qt command interface

This python interface allows to use simultaneously inertial instruments with other peripheral machines as turn tables, climatic chamber, or vacuum chamber, each of them having its own serial port. All instruments controls are centralized in one program, so various characterizations and calibrations are realized by scripts where all commands are successively sent to the different peripherals.

3.2 Self-calibrations

The main perspectives of this complete architecture are the evaluation of new operating modes, in particular based on self-calibration sequences. At least 3 resonators are required to make a complete Inertial Measurement Unit (IMU) for acceleration or rotation, but by using 4 resonators in tetrahedron shape, each set of 3 constitutes an IMU, allowing the fourth one to quit inertial mode and self-calibrate parameters dependent on temperature especially.

In the case of the VBA accelerometer maintained at its varying resonance frequency, self-calibration corresponds to open feedback loop, and to explore some steady-state around assumed resonance frequency in order to update capacitive and resistive bias, phase bias, Q factor and resonance frequency.

4. Performances

The Quartz Vibrating Beam Accelerometer has been connected to the digital electronics for characterization in instrumental conditions: the accelerometer is placed on a horizontal turn table (horizontal axis, vertical tray) to project gravity around its sensitive axis, to extract bias and scale factor [5]. This test bench is inside a thermal chamber to track possible bias drift under temperature. Bias residuals during temperature cycles (10°C steps) are evaluated to 60 µg rms (see Figure 12.), but the performance of the accelerometric head alone (without electronics) had been previously observed as low as 33 µg rms, with external frequency meters.

Actually most of the residuals in the figure are due to a hysteresis at low temperatures, when subject to frost and condensation. A better packaging of the electronics will solve this issue, as bias repeatability between cycles at given positions in the cycle yield a 30 µg rms dispersion.

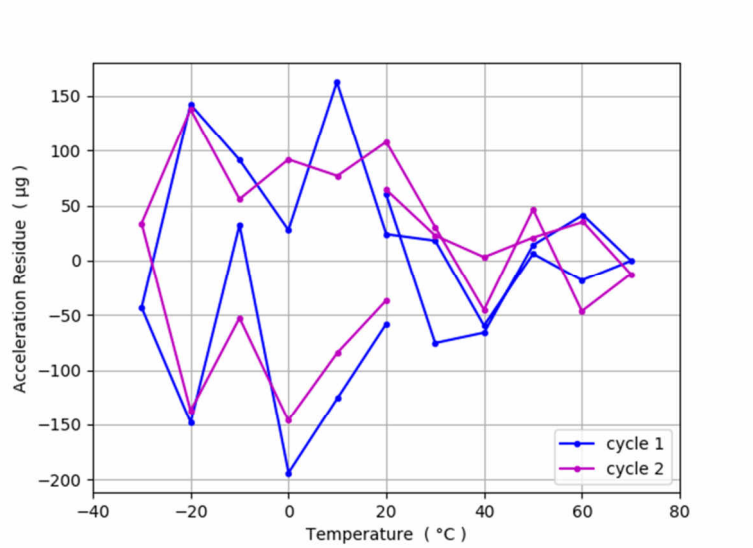


Figure 12. Accelerometer bias stability over temperature

Noise characterization is performed by acquiring long sequences in stabilized conditions, in order to record only the instrument noise, without drift. The resulting Allan standard deviation (in µg rms) is plotted versus integration time and gives a minimum of 0,8 µg (see Figure 13.).

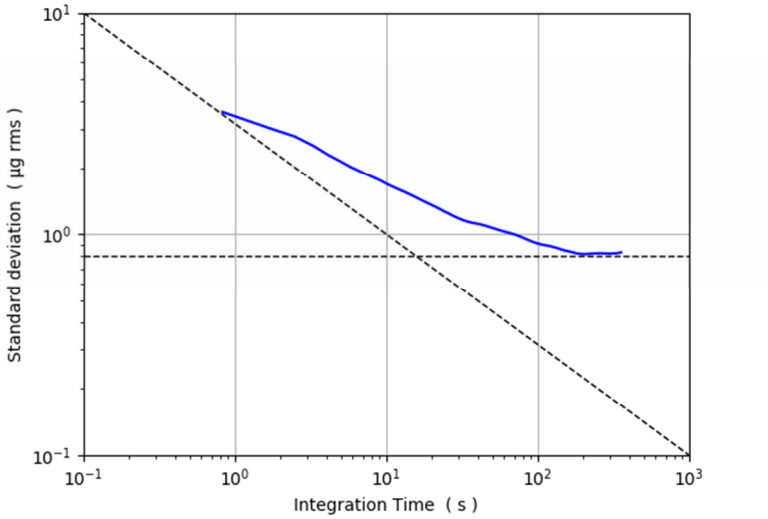


Figure 13. Allan standard deviation as a function of integration time. Flat asymptot is the Allan minimum at 0.8 µg rms.

In the case of the Coriolis Vibrating Gyroscope (CVG), the sensor is set on a vertical turn table (vertical axis, horizontal tray), which operates several angular rates to extract sensor parameters : bias, scale factor…. Next, noise characterization is performed with the Allan standard deviation again, in °/h (see Figure 14.). The minimum is 1.5 °/h, and angular random walk is 0,03 $°/\sqrt{h}$ (equivalent to $2\,°/h/\sqrt{Hz}$ on the spectral density).

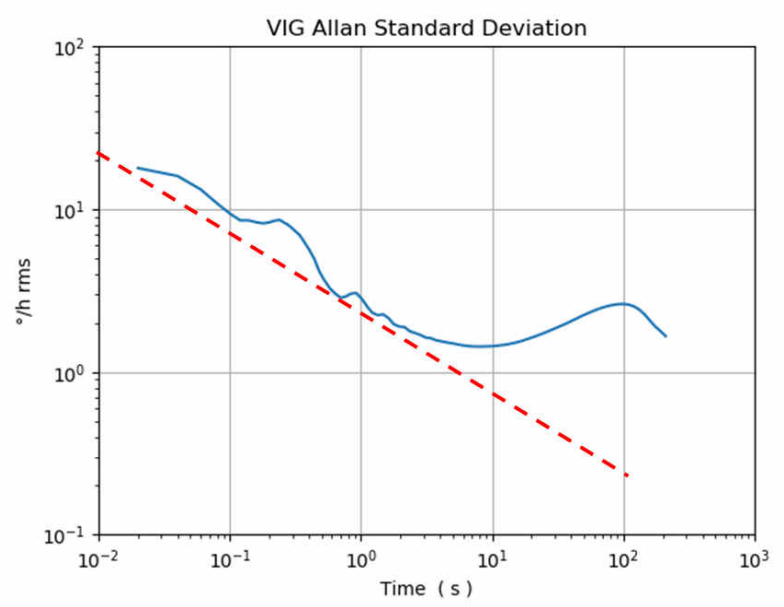


Figure 14. (a) Allan standard deviation. Flat asymptot is the Allan minimum at 1.5 °/h rms.

The noise figure is degraded by spurious spectral lines which are a signature of aliasing, and shall be filtered out by increasing the sampling rate before decimation.

5. Conclusion

We now recover almost the same performance obtained with the former electronics [6], with a more generic design, non dependent on specific components like Analog to Digital Converters. The new digital architecture is portable and synthesizable on several FPGA targets, as well as ASIC targets at low cost since most of functions are essentially digital. In addition, this structure is particularly suitable to self-calibration algorithms development, which is the main perspective of this work.

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