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From Spintronic Devices to Hybrid CMOS/Magnetic System On Chip

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Abstract—“Beyond CMOS” is today one of the major research directions in semiconductor industries to address current integrated circuit issues. Many alternative technologies are currently under investigation to deal with the scaling limits of CMOS technology. This paper presents the design of a full system on chip based on a hybrid CMOS/Magnetic process. Spin-transfer-torque magnetic tunnel junctions are used to design different functions such as logic, memory, security and analog IP blocks.

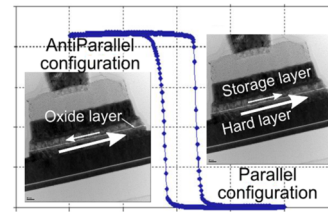


Fig. 1. Magnetic tunnel junction

I. INTRODUCTION

The number of connected devices around the world is growing fast with a forecast of 30 billion connected objects by 2020 [1]. The key requirements are ultra-low power, high processing capabilities, fast/dense storage, wireless communication, heterogeneous integration, and autonomy. Although it has been serving the industry well for several decades, CMOS technology has more and more obstacles to continue scaling into the future [2]. The main issue of the scaling limit of CMOS is the energy efficiency which is essential for battery-powered smart systems. New technology directions are being explored to continue providing denser, cheaper, faster and low power integrated circuits. This paper focuses on the spintronic device option. Unlike CMOS, they have the benefit of being non-volatile. This non-volatility can be integrated inside the logic devices to enable new computing paradigms and provide better energy efficiency. In this work, 200-nm spin-transfer-torque magnetic tunnel junctions (STT-MTJ) are used as elementary blocks in addition to 180-nm CMOS transistors to design a full system on chip (SoC) including multiple functions such as logic, memory, security and analog intellectual property (IP) blocks. The rest of the paper is organized as follows: Section II presents the STT-MTJ device and different STT-MTJ based IP blocks. Section III describes in details the architecture of the hybrid CMOS/magnetic SoC designed in this work. Section IV discusses the considered application scenarios for power analysis. Conclusions are finally given in Section V.

II. STT-MTJ DEVICE AND RELATED IP BLOCKS

A full design flow has been established for hybrid CMOS/Magnetic circuits based on STT-MTJ devices. On the one hand, physical and behavioral compact models have been created for circuit simulators such as SPICE. On the other hand, a process design kit (PDK) compatible with the standard design tools has also been developed to design IP blocks and chip-level systems based on a CMOS/Magnetic process. This section gives the basics of the STT-MTJ device and the related compact models before presenting different STT-MTJ based IP blocks used in the design of the SoC.

A. STT-MTJ device

1) **Basics:** Magnetic tunnel junctions (MTJ) are nanostructures composed of two ferromagnetic layers separated by a thin insulator (Figure 1). The resistance of the stack depends on the relative orientation of the two layers. A parallel (anti-parallel) state of the MTJ causes a low (high) resistance value which can be characterized as a logic zero (one). The tunnel magneto resistance (TMR) ratio gives the relative variation of resistance between the two states, which is typically around 150% to 200%. While the magnetization of one of the two layers is pinned to one direction (reference layer), the magnetic orientation of the other one (storage layer) can be flipped by applying a sufficient current through the MTJ, with a hysteretic behavior. The magnetization switching is driven by the spin-transfer-torque (STT) effect [3] where the current gets spin polarized by the reference layer and transfers the magnetic moment to the storage layer. Reading the magnetic state consists in measuring the resistance of the device.

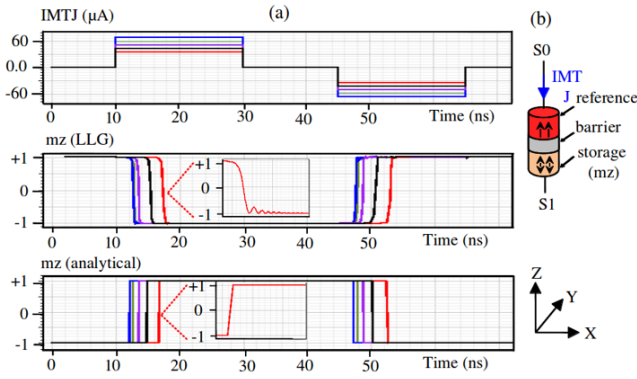


Fig. 2. Magnetization switching simulation with physical (middle) and behavioral (bottom) compact models

2) **Compact models:** Two main approaches have been considered to model the magnetization switching of the MTJ : physical [4] and behavioral [5]. The former uses the Landau-Lifshitz-Gilbert equation which gives an accurate dynamic evolution of the magnetic state driven by the STT effect, with a precessional behavior. However, this model is relatively slow and not adapted to the simulation of complex circuits such as memory arrays. The latter does not model the magnetization dynamics and needs a calibration of the parameters of the MTJ to fit the actual behavior of the device. As a result, this model allows much faster simulations. Regarding the resistance of the MTJ, both models take into account the dependence of the resistance upon the magnetic state and the polarization voltage, the dependence of the transport and magnetic parameters upon the temperature and the heating of the MTJ due to Joule effect.

Figure 2 shows the magnetization switching behavior of the STT-MTJ using the physical and the behavioral compact models.

B. STT-MTJ based IP blocks

1) **Non-volatile Flip-Flop:** Thanks to the PDK developed in this work for CMOS/Magnetic design, a non-volatile flip-flop (NVFF) is proposed as an extra standard cell (Figure 3) to give the possibility to make more complex circuits (e.g. processor) non-volatile. The NVFF is based on a standard CMOS flip-flop with additional MTJs together with their read/write circuits. The layout of the NVFF is shown in Figure 4. This cell has been intensively characterized for timing and power through electrical simulations including worst case corners and Monte-Carlo analysis. Furthermore, all necessary files are available to use the NVFF in each step of the standard design flow including synthesis, digital simulations and physical implementation.

2) **STT-MRAM:** The STT-MTJ device has been used as a memory cell to design a full magnetic random access memory (MRAM). A memory compiler approach was used to easily provide memories of different sizes (up to 16kB) according to the specifications. Figure 5 and 6 respectively show the memory architecture of a 16kB STT-MRAM and

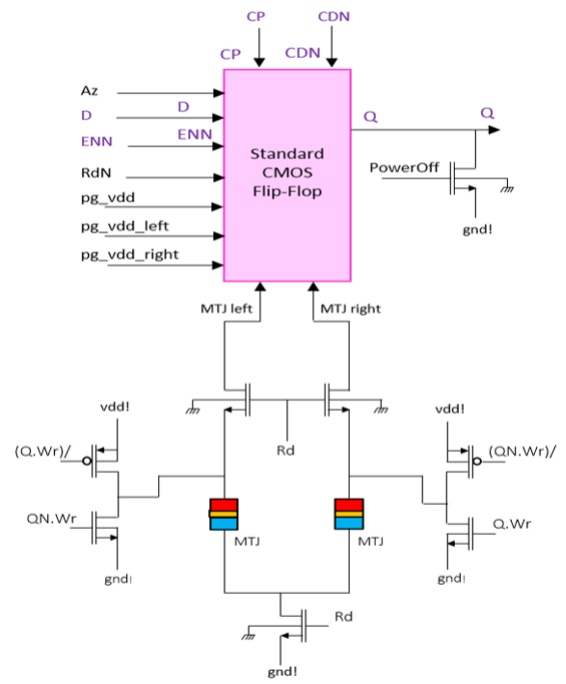


Fig. 3. STT-MTJ based non-volatile flip-flop architecture

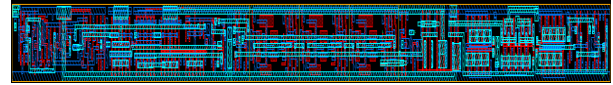


Fig. 4. Layout of the Non-Volatile Flip-Flop

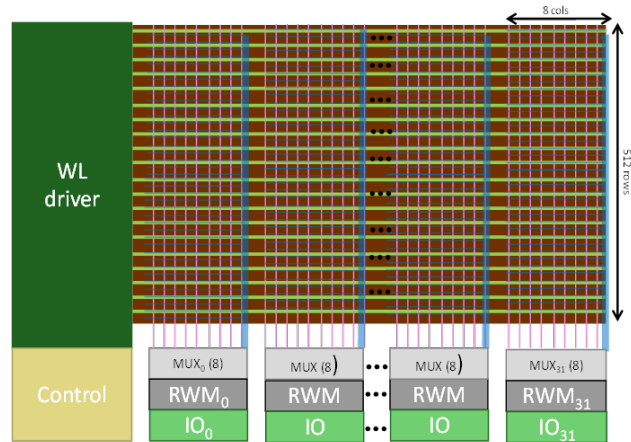


Fig. 5. STT-MRAM architecture

the corresponding layout. This memory is designed with a synchronous single-port SRAM-like interface and uses a 32-bit word organization. Electrical simulations were also performed to characterize this memory circuit for timing and power in order to use it in the digital design flow.

3) **True Random Number Generator:** This work includes the design of a building block for security applications. The

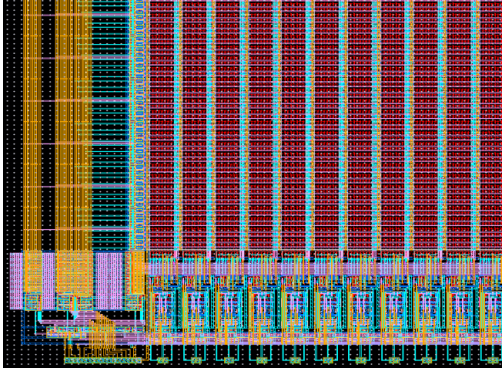


Fig. 6. STT-MRAM layout

developed IP is a true random number generator (TRNG) based on STT-MTJ to generate random cryptographic keys for high secure data encryption. TRNGs use non-deterministic physical events to generate random numbers with a very high entropy and zero correlation. This STT-MTJ based TRNG uses the stochastic nature of the STT switching as a source of randomness to generate 1-bit random numbers by applying a write current with 50% of success rate.

4) Analog-to-Digital and Digital-to-Analog Converters:

Two additional IP blocks have been considered for processing analog signals. On the one hand, a 1-bit delta-sigma analog function is proposed where the active bridge is used in a feedback structure to convert a relative variation of resistance into a digital word [6]. A frequency divider, whose configuration is stored in STT-MTJs, is implemented to control the sampling rate and therefore the signal bandwidth. On the other hand, a current output digital-to-analog converter (DAC) has been designed. The design has a segmented architecture with a R2R Ladder and a thermometer topology using STT-MTJs as resistors.

III. HYBRID CMOS/MAGNETIC SYSTEM ON CHIP

A. Architecture

Based on the building blocks presented in Section II-B, a full SoC has been designed to evaluate the co-integration of digital and analog IP blocks using STT-MTJ devices. The overall architecture is depicted in Figure 7. The design corresponds to a microcontroller including a processor core, memories and peripheral devices.

1) **Non-volatile processor:** The microcontroller is based on the Secretblaze [7], a 32-bit 5-stage pipeline RISC processor compatible with Xilinx’s MicroBlaze instruction set architecture. The Wishbone bus interface is used to allow the connection of external memories and peripheral devices.

The Secretblaze core has been made fully non-volatile by using the non-volatile flip-flop (NVFF) presented in Section II-B1. The hybrid architecture of the NVFF gives the possibility to backup/restore the processor state into/from the STT-MTJs while the CMOS part is used during normal operation for high performance. This non-volatility inside the microarchitecture is a valuable benefit for energy efficiency

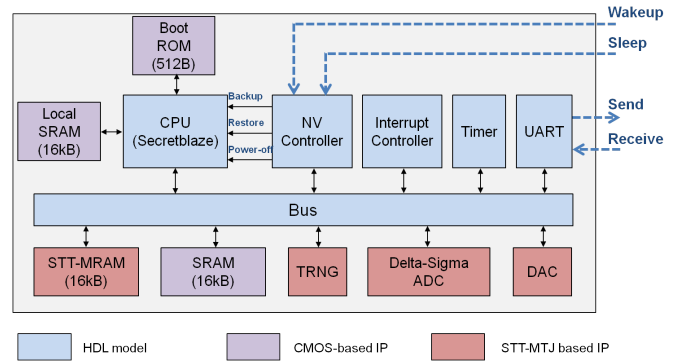


Fig. 7. SoC architecture

since aggressive low-power mode is possible with near zero leakage power. In addition, the wakeup time is significantly reduced as the system state is preserved after a shutdown.

2) **Memory organization:** The memory subsystem consists of a 512B read-only memory (ROM) for the boot process and three 16kB random access memories (RAM) to store instructions and data. Several RAMs have been implemented for comparison purposes. During normal operation, only one RAM is actually used to execute the application. On the one hand, a local SRAM directly connected to the processor is available with a dual-port interface to allow simultaneous read/write operations. On the other hand, a SRAM and the STT-MRAM presented in Section II-B2 are accessible via the Wishbone bus interface. The objective is to compare the SRAM-based microcontroller with the STT-MRAM based microcontroller on the same platform.

3) **Peripheral devices:** A set of peripherals has been integrated into the SoC including digital IP cores (interrupt controller, timer, UART) and the analog IP blocks presented in Section II-B3 and II-B4 (TRNG, Delta-Sigma ADC, DAC).

Moreover, a specific controller (“*NV Controller*” in Figure 7) has been developed to manage the backup/recovery of the system state. Before entering into sleep mode, the *NV controller* backs up all the NVFFs of the processor. To avoid electrical integrity issues due to the high write current during this operation, the NVFFs have been arranged in several clusters. Thus, a sequential backup is performed. To wake up the system, the NVFFs are also restored in a sequential way.

B. Operation

After the power is switched on, a normal boot consists in loading the binary code of the application via the UART interface and copying it into the local SRAM, or the SRAM or the STT-MRAM. Then, the processor fetches the first instruction to be executed. Alternatively, the system can restart from a known state in the case of returning from sleep mode.

Regarding the power modes management, the *NV controller* is called for placing the system in sleep mode either by software or by an external signal (“*Sleep*” in Figure 7). Returning to active mode is possible either by an external signal (“*Wakeup*” in Figure 7) or further to an event from the interrupt

controller. Above scenarios have been validated through post-layout simulations considering several applications.

C. Layout and features

A full layout of the SoC is shown in Figure 8 and some features are given in Table I. This non-volatile microcontroller can run at 20MHz with a backup/recovery time of about $4\mu\text{s}$. The energy costs are respectively 437nJ and 98.7nJ . It is worth noting that the current implementation of the SoC aims at giving a proof of concept instead of an optimized design. For instance, this work has made all the flip-flops of the processor non-volatile while this is not mandatory to preserve the system state after a shutdown. Thus, optimizations are still possible for the backup/recovery time and energy. Moreover, considering a more advanced technology node would further improve the overall performances.

IV. APPLICATION SCENARIOS

Typical application scenarios of the internet of things (IoT) are under development to analyze the power consumption of the SoC. IoT objects essentially do three actions: sensing, processing, sending. The system first captures information from the external environment thanks to a sensor followed by an analog to digital conversion. Second, the measured data are stored in memory and minor or more complex computations

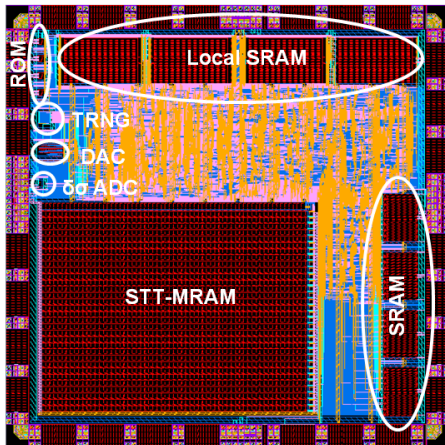


Fig. 8. SoC layout

TABLE I
SOC FEATURES

Die Area	23mm^2
Process	180nm CMOS / 200nm STT-MTJ
Supply Voltage	1.8V Core / 3.3V IO
Frequency	20MHz
Number of NVFFs	2126
Backup time	$4.15\mu\text{s}$
Recovery time	$4.15\mu\text{s}$
Backup energy	437nJ
Recovery energy	98.7nJ

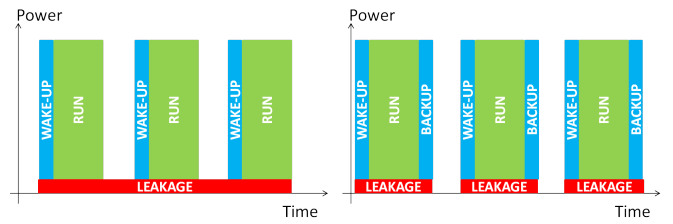


Fig. 9. Current solution (left) vs normally-off computing (right)

are performed. Finally, data are sent to a data center wirelessly. Once the wireless transmission ends, the system can go into sleep mode and wake-up later to restart the overall process.

The objective is to demonstrate how the normally-off computing (Figure 9) will allow better energy efficiency for a set of a real applications. Preliminary experiments show that staying in sleep mode for several milliseconds is sufficient to optimize the power consumption.

V. CONCLUSION

This paper presented the design of a full system on chip based on a hybrid CMOS/Magnetic process, from the STT-MTJ device to the design of the entire chip by way of STT-MTJ based IP blocks. A non-volatile microcontroller has been developed to enable new computing paradigms and provide better energy efficiency for beyond CMOS circuits. Future work will consider more advanced technology nodes to evaluate the potential of spintronic technologies.

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