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Repetitive short-circuit measurement on SiC MOSFET

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Abstract. A robustness study for 1.7 kV SiC MOSFETs is presented in this article. After evaluation of the critical energy required for failure, devices went under repetitive short-circuits conditions. Because those power switches went under very stressful mode, the monitoring of key parameters is required to analyze failures which in all occurrence seems to be related to the gate oxide. The strong impact of drain to source voltage on critical energy during short-circuit mode is also investigated. Additionally, test bench and protocols are detailed.

Introduction

In power electronic applications, the use of Silicon Carbide (SiC) material is now largely common. Its potential is superior to Silicon (Si) [1]. For example, it has a wider bandgap of ~ 3.2 eV against 1.12 eV for Si and a critical field strength around ten times stronger resulting in that SiC transistors sustains a much higher voltage with lower static and commutation losses.

4H-SiC MOSFETs as power switches are used on numerous studies to improve efficiency and performances of power converters. However, a weakness of their gate oxide technology [2][3] is a major drawback when it comes to robustness analysis [1]. Those transistors are voltage controlled thus any threshold voltage shift during ageing is a worrying phenomenon for many industrials. Short-circuit especially is a undesirable state in which the device is under considerable stress [4], [5]. This may be destructive for the device. Unfortunately, short-circuits may occur in real-life converters

This article reports on experimental repetitive short-circuit “RSC” tests on 1.7 kV 45 m Ω Silicon Carbide MOSFET to assess the robustness of those devices. Key parameters are monitored and presented, like the threshold voltage shift ΔV_{th} or the gate leakage current. Complementary tests are performed to check the gate oxide integrity, such as modified three terminal charge pumping.

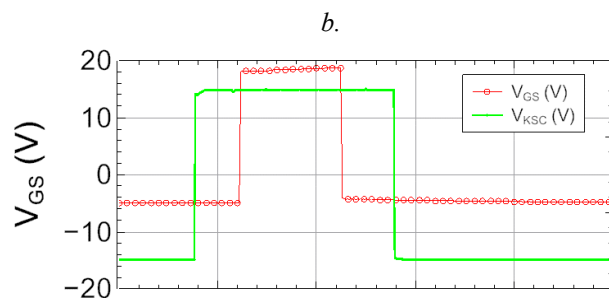
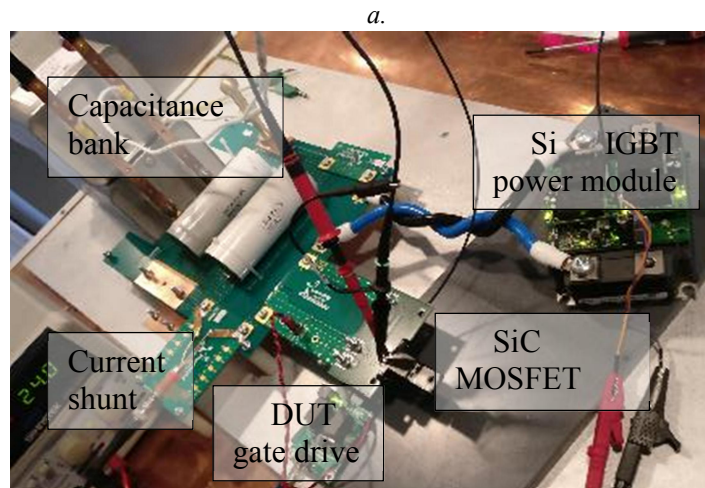


Fig.1- a. Short-circuit test bench b. DUT and IGBT gate signals

Short Circuit Test Bench Overall Description

The test bench showed on Fig. 1a. is capable of performing short-circuit up to 10 kV. It is based on classical short-circuit test benches [3]. A high voltage power supply is charging the capacitor bank. Then the Si IGBT power module low side is switched ON. A very short time after, the DUT is also switched ON as depicted on Fig. 1b. Under those conditions, current is flowing through the device as the DC capacitance is discharging, only limited by the component on-state resistance. Yet between drain and source there is still high voltage, the device under test is on short-circuit conditions during a brief period of time. Nominal value on the gate control is $t_{sc} = 10 \mu s$ and can be adjusted to control short-circuit energy.

Critical energy estimation

Critical energy is the maximal energy the device can withstand before failure. As described in [6], short circuit duration is increased until failure occurs. This value gives us precious data on short-circuit parameters as short-circuit current, drain to source voltage and short-circuit time withstanding are all linked by the following equation

$$E_C = \int_0^{t_{sc}} V_{DS} \cdot I_{SC} \cdot dt \quad (1)$$

Fig. 2 shows how to compute the short-circuit energy just before failure on #cc1. E_C is computed at approximately 1.5 J. This value is to be taken with a cautious as we figured out later than it can change greatly from one device to another. This figure also shows also the evolution of the saturation current $I_{sc} = 450 A$ as a function of the short-circuit duration for a Drain to Source bias of 500 V. I_{sc} great value was a surprise as it is nearly 6 times the nominal current of the device. However, the curve is typical of a short-circuit condition as it rises quickly and then slows down as saturation current value is decreasing due to self-heating. A further analysis shows a critical aspect of SiC MOSFET behavior under short-circuit condition. JEDEC standard [7] stated that repetitive short-circuit test must be performed at 80% of V_{BR} (breakdown voltage). On a 1.7 kV MOSFET, $80\% \cdot V_{BR} = 1.36 kV$ and the saturation current is still considered equivalent to 450 A.

With a similar critical energy of 1.5 J the short-circuit duration has to be reduced to roughly $t_{sc} = 2.7 \mu s$, which is very difficult to measure.

To better analyze the short-circuit current, we performed 2 complementary tests. The first one is repetitive at 80 % of E_C , and the other one investigate the influence of the drain to source voltage on the critical energy.

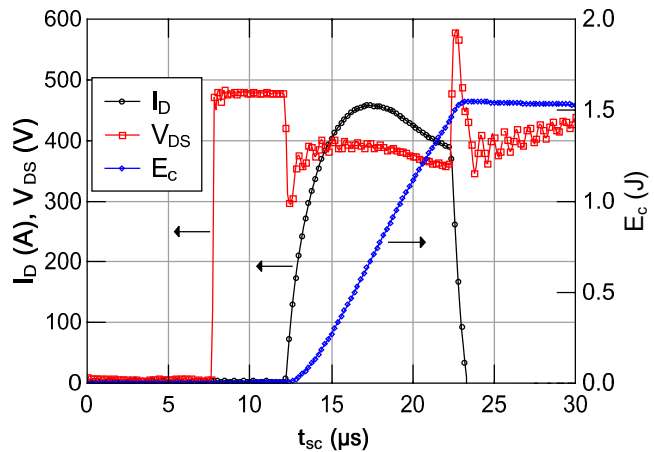


Fig. 2. Drain to source bias and drain current as a function of time on #cc1. The critical short-circuit energy is deduced from area of $I_D \cdot V_{DS}$ curve.

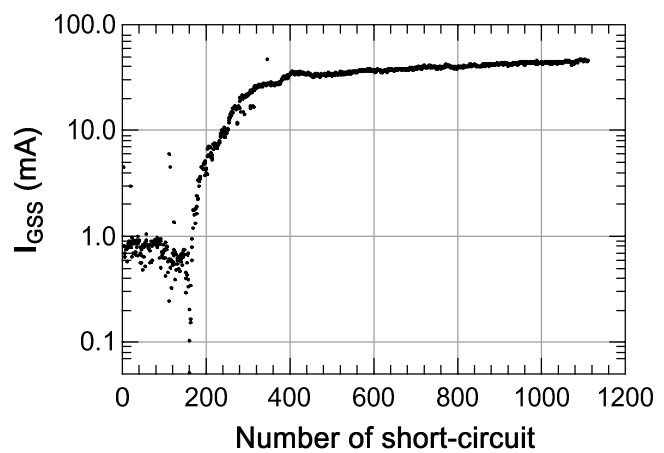


Fig. 3. Evolution of „cc2“ DUT I_{GSS} as a function of the number of repetitive short-circuits ($V_{DS} = 500 V$, $I_D = 450 A$, $t_{sc} = 11 \mu s$, $E = 1.6 J$ ($0.8 E_C$))

Repetitive Short-Circuit Tests Measurements

#cc2 went under repetitive short-circuits and the evolution of the gate current I_{GSS} is shown on Fig. 3. The maximum value on the datasheet is 1mA and a typical characterization gives $I_{GSS} < 1nA$. During short-circuit tests its value is way higher because it is capacitive current. Nonetheless, it can be seen that the 1.7 kV SiC MOSFET cannot withstand more than 167 short-circuits before degradation. The rise of the gate current shows that the gate is perforated.

Some of the main parameters changes are resumed on Table 1 below. Gate leakage current, threshold voltage, on state resistance, internal gate resistance are all impacted.

A charge pumping curve (Fig. 4) shows that the gate oxide degradation is severe, the waveform doesn't show pumped charged current anymore. Unfortunately, C-V curves cannot be used.

To manage the large variation of the critical energy we propose a step protocol: increasing steps of E_{SC} each 300 short-circuits. Fig. 5 shows the result on one component. Fig. 6 shows the results obtained on several devices used for those tests. The purpose of this test protocol was to decrease the incertitude on the critical energy, which can vary from 1.5 J to 2 J on some components.

Drain to Source Voltage Impact on Critical Energy

We also investigated the impact of the V_{DS} value. The more V_{DS} is increased, the lower the critical energy is. For example, for $V_{DS} = 600 V$ ($\sim 35\% V_{BR}$) the critical energy is now only of 1.2 J. at the beginning, $E_c = 2 J$. it is interesting to see that this device as a critical energy of 2 J, versus 1.7 J for #cc2 presented in the beginning of this article. The stronger the electric field between drain and source is, the lower the energy required to kill devices is.

Table 1-Evolution of device parameters after RSC

Parameters	Before RSC	After 1000 RSC
I_{GSS}	39.4 pA	>1 mA
V_{th}	2.86 V	2.98 V
R_{DSon}	40 m Ω	80.5 m Ω
R_g	1.95 Ω	19.8 Ω
V_{BR}	2.21 kV	2.21 kV

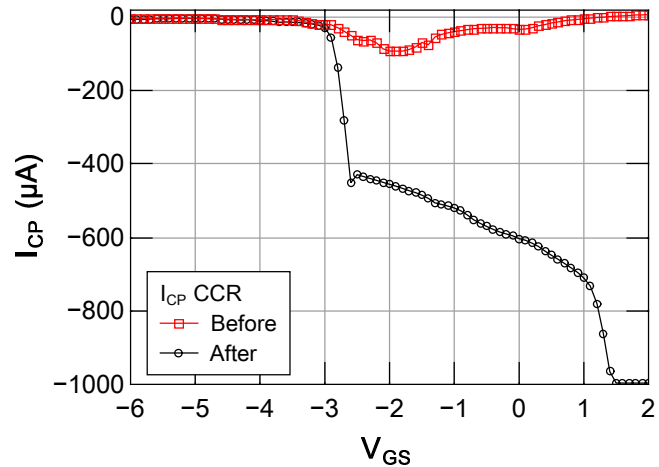


Fig. 4-Charge pumping measurement

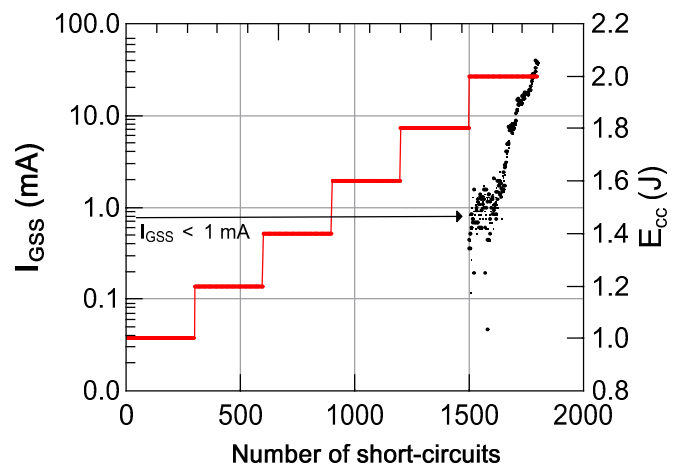


Fig. 5-Gate leakage current evolution for $V_{DS} = 500 V$

at the beginning, $E_c = 2 J$. it is interesting to see that this device as a critical energy of 2 J, versus 1.7 J for #cc2 presented in the beginning of this article. The stronger the electric field between drain and source is, the lower the energy required to kill devices is.

Conclusions

Short-circuit on SiC MOSFET is a behaviour that is quite worrying. The results presented on this study shows that the withstand time is quite low ($\sim 10 \mu\text{s}$), and become even lower ($\sim 3 \mu\text{s}$) if the $80\% \cdot V_{BR}$ condition is respected. Moreover, there is some critical energy spreading between devices of the same references: from 1.5 J to 2 J on the components used for the tests presented here.

The gate oxide is the weakness of SiC MOSFET technology, the electric stress under short-circuits and the temperature results in a degradation that kills the gate oxide which end up perforated. For the measured devices, 1.7 kV SiC MOSFETs, they can only withstand some hundreds short-circuits at $V_{DS} = 500 \text{ V}$. Clearly it can be said that from the results presented here, the repetitive short-circuit test is the more stressing scenario of the classical robustness tests.

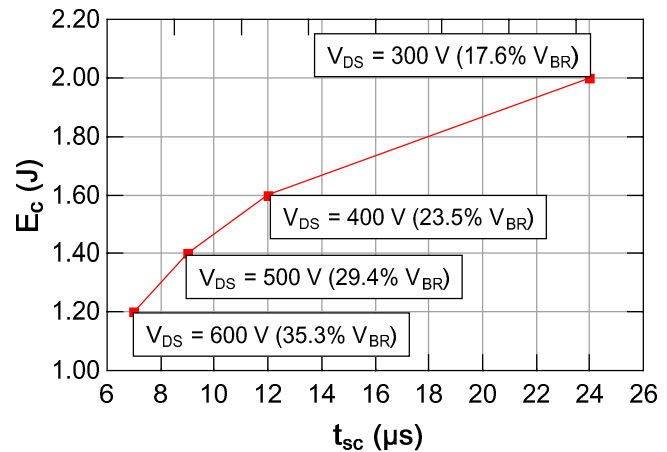


Fig. 6- E_c as a function of different short-circuit withstanding time, for several V_{DS} on #cc6

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