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► **To cite this version:**

Guillaume Prenat, Kotb Jabeur, Gregory Di Pendina, Olivier Boule, Gilles Gaudin. Beyond STT-MRAM, Spin Orbit Torque RAM SOT-MRAM for high speed and high reliability applications. Weisheng Zhao; Guillaume Prenat. Spintronics-based Computing, Springer International Publishing, pp.145-157, 2015, 978-3-319-34661-8. 10.1007/978-3-319-15180-9\_4 . hal-01976635

**HAL Id: hal-01976635**

**<https://hal.science/hal-01976635>**

Submitted on 3 Jan 2022

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# **Beyond STT-RAM, Spin Orbit Torque (SOT) RAM for high speed and high reliability applications**

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## **1 Introduction**

For 40 years, microelectronics has been following the Moore's law, stating that the density and speed of integrated circuits would double every 18 months. However, this trend is presently getting out of breath, because of incoming insurmountable physical limits. Due to decreasing devices size, leakage current is becoming the main contributor to power dissipation of CMOS. The increased density and reduction in die size lead to heat dissipation and reliability issues. Moreover, the dynamic power keeps on growing up with both clock frequency and global capacitance while the power supply is not scaled down accordingly. Several solutions are investigated to try to push forward these limits at technology, circuit or architecture levels. The "more than Moore" concept consists in using new devices beside or in replacement of standard CMOS transistors. For instance, the use of non-volatile devices is seen as a promising solution to reduce power consumption, improve reliability and offer new functionalities. Several technologies are intensively investigated like Phase Change Random Access Memory (PCRAM), Ferroelectric RAM (FeRAM), RedoxRAM and Magnetic RAM (MRAM). In its 2010 report, ITRS identified RedoxRAM and STT-MRAM as the two most promising technologies for embedded memories at technology nodes below 16nm. The combination of non-volatility, fast access time and endurance in MRAM technology paves the path toward a universal memory. Although an expanding attention is given to two-terminal Magnetic Tunnel Junctions (MTJ) with writing based on Spin-Transfer Torque (STT) switching as the potential candidate for future memories, it suffers from weaknesses. Thus, two main shortcomings are still limiting the reliability and endurance of STT-MRAMs: i) The high current density required for writing can occasionally damage the MTJ barrier, specially for switching on the nanosecond time scale ii) It remains a challenge to fulfill a reliable reading without ever causing switching for very advanced technology nodes, since writing and reading operations share the same path, through the junction. Indeed, the smaller the MTJ is, the lower the writing current is, without having the possibility to re-

duce the reading current to maintain a reliable sensing. Three-terminal MTJ with writing based on Spin-Orbit Torque (SOT) approach revitalizes the hope of an ultimate RAM. It represents a pioneering way to triumph over current two-terminal MTJ's limitations by separating the reading and the writing path.

## 2 MTJs written by Spin Orbit Torque (SOT)

Recently, a new effect was discovered, leading to new devices with three terminals. This effect is called Spin Orbit Torque (SOT), a generic term encompassing in reality different possible mechanisms originating from the bulk of the material and the interfaces between the different layers. These mechanisms issued from the spin orbit interaction are often named the Rashba effect and the Spin Hall Effect (SHE) [1], [2], [3] for the contribution of respectively the interfaces and the bulk. However this denomination is often a shortcut since the contribution from interfaces and bulk are intricately. SOT allows switching the magnetization of a magnetic Storage Layer (SL) by passing a current in the plane of the conductive contact line below it, instead of through the MTJ itself (Fig.1). This allows separating the reading and writing paths with great benefits: firstly, since no large writing current is passing through the tunnel barrier which can damage it, the endurance can be truly infinite. Secondly, risks of accidental writing during reading are much less. Moreover, the switching duration using this scheme can be very fast, typically some hundreds of picoseconds, providing the injection of relatively large current densities. Compared to STT [4], [5] the fast SOT-switching is deterministic and does not show any precessional behavior [6]. Today, the current density is higher than for STT (typically  $5 \cdot 10^7 \text{A/cm}^2$ ), but since it flows through a very thin line (5nm for instance), the resulting writing current can be very small. Moreover, since the writing time can be very short, the resulting energy can become very interesting. The main limitation of this technology compared to STT is apparently the area density because of the additional terminal. However, this picture is not so simple considering a complete memory since i) transistors can be shared ii) the area of MRAM is often limited by the size of the addressing transistors more than that of the single magnetic cell. However, since the writing current decreases proportionally to the lateral dimension of the device and not with its surface, the scalability is weaker than for STT writing, but remains much better than for magnetic field writing. An important feature of the device is the thermal stability of the device is ensured down to 20nm.

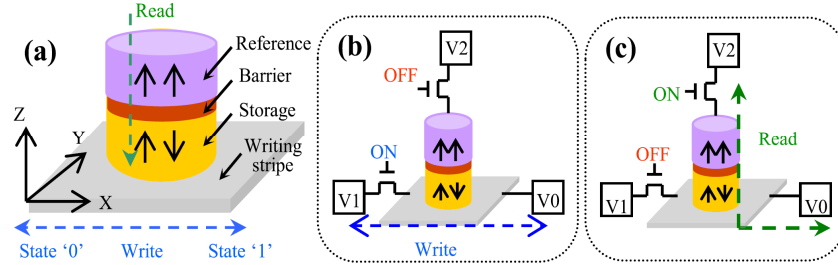


Fig.1: (a) Schematic of the three-terminal SOT device and the two independent paths for (b) write and (c) read operations. In-plane current injection through the write line (writing stripe) induces the perpendicular switching of the storage layer.

Another specificity of this writing scheme is that a small static magnetic field is required to avoid stochastic switching: without it, for a given direction of the writing current, the magnetization can switch randomly in either P or AP configuration. Adding an external magnetic field makes the switching deterministic, with a direction of the current writing the P state and the opposite direction the AP state. This field can be generated by a magnetic layer, which could be part of the MRAM process and integrated to the pillar stack, with a static magnetization, acting like a permanent magnet, with no additional power consumption. This particularity can be turned into an advantage. Indeed, if the direction of the magnetic field is switched, the operation of the device is inverted: the direction of the current previously used to write a logic '0' will write a logic '1' and vice-versa (Fig.2). It can be useful for reconfigurable computing. In this case, the magnetization of the layer generating the magnetic field could be chosen using a current line to generate a magnetic field, like in original Field Induced Magnetic Switching (FIMS) writing schemes. The corresponding power consumption would then depend on the reconfiguration frequency.

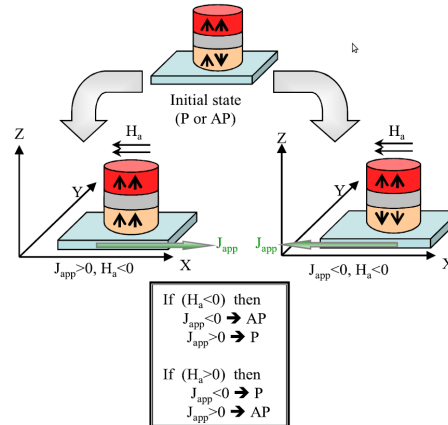


Fig.2: Switching dependence on the external applied field  $B_a$  and current direction

Although this technology is at very early stage development, these properties make it particularly interesting for high speed applications that do not require very high densities. Typically, it can be suitable for low-cache levels replacement in processors, which is not possible with classical STT. Since this technology solves some of the major issues of STT, a lot of academic organisms and industrial companies are intensively working on it and we have good confidence that it can have a predominant place in the future of spintronics, for a lot of applications.

### **3 Applications of SOT-RAM**

#### ***3-1 Introduction in the memory hierarchy of processors***

As seen in the previous chapters, a lot of studies have been recently carried out to introduce STT-RAM in the memory hierarchy of processors. Indeed, it is the only technology that offers an intrinsic non-volatility together with a speed suitable for use as a working memory and a quasi-infinite endurance. Adding non-volatility in the memory hierarchy has a lot of advantages, in particular the ability to ease the power gating techniques, which consist in cutting off the power supply of unused blocks to drastically reduce the leakage. Indeed, having a local non-volatility allows directly cutting off the power supply without having to save the content of the memory in distant non-volatile or very low-leakage storage devices. The first and more obvious approach consists in directly replacing the parts of the memory hierarchy whose operating speed is compatible with those of STT-RAM (DRAM main memory, or L2 cache level). Going deeper into the memory hierarchy seems difficult since STT-RAM cannot compete with fast SRAM in terms of writing speed. However, some works have shown that the better density of MRAM allows having a larger L1 cache capacity, which can compensate the loss of speed for some applications [7]. This approach requires rethinking the architecture of processors and memory hierarchy and is adapted only to some specific applications. Other works propose the use of a hybrid SRAM/MRAM memory. Several architectures have been proposed, allowing using the memory as a standard SRAM in operation, but with the capability of backing-up the content in MTJs and restore it at any moment. This allows bringing non-volatility in low levels of cache, but with a loss in terms of density.

Since SOT have a writing speed approaching that of SRAM, it is possible to consider directly replacing L1 cache by SOT-RAM. The result would be the introduction of non-volatility in L1 cache, without penalty in terms of speed. Moreo-

ver, thanks to its density which remains much better than the one of SRAM, bigger caches could be used, resulting in probable performance improvement.

### ***3-2 Non-volatile Flip-Flops, normally-off/instant-on computing and Memory-in-Logic***

The architecture of latches and Flip-Flops (FF), distributed memory containing the active data of the logic part of the circuit, is very similar to that of SRAM. It is thus possible to introduce non-volatility in the logic itself, in the same way that SRAM can be made non-volatile [8], [9], [10]. It is particularly interesting since it allows freezing the state of the processor or any digital / mixed signal IC, and restart in the same state. It allows developing new paradigms like normally-off and instant-on computing [11], in which the circuit is off by default and power supplied only when required. It can be switched-off instantaneously and restarted in the same state. This still reduces the power consumption but also improves the reliability. It is possible for instance to implement a checkpoint for rollback operation in processors, to restore the system state with a snapshot taken in the past. Thanks to its high speed, low-energy writing and infinite endurance, SOT allows saving the context more often, even possibly at each clock edge, without energy overhead or performance loss and thus still improving the reliability.

Although the intrinsic non-volatility of MTJs naturally encourages using them as memory elements, it is also possible to intrinsically mix logic and memory to shorten and multiply the communication between them, leading to a new paradigm in logic architectures. This concept, called “logic-in-memory” has been proposed in [12]. Examples of circuits based on Current Mode Logic (CML) have been proposed and implemented in silicon demonstrators giving encouraging results [13]. For this purpose, the SOT MTJ has another advantage thanks to its third terminal offering an additional degree of freedom and the possibility to reverse its behavior by changing the direction of the external magnetic field.

## **4 Design tools and environment for the design of hybrid CMOS/SOT-RAM components**

### ***4-1 Compact electrical model of SOT-MTJ***

As the semiconductor industry is progressively going toward “hybrid CMOS” Integrated Circuits (ICs), compact model development has become a cornerstone in the circuit/system design and verification tool flow.

Recently, a compact model of the SOT MTJ has been proposed by Spintec [14]. The most significant physical phenomena involved in the writing (SOT) and the

reading (TMR) are taken into account and realistic parameters, obtained from characterization of single cells SOT-RAM [15] were used to calibrate the model. This model is written in VerilogA language and based on physical equations modeling the behavior of the device. The dynamics of the magnetization is described, based on the Landau-Lifshitz-Gilbert (LLG) equation [16], including additional SOT terms [1], [2], [3], [15], [17], [18]. The dependence of the resistance upon the magnetic configuration (Tunnel Magneto-Resistance or TMR, relative resistance variation of the stack between Parallel and Anti-Parallel resistance states) and the applied voltage is described using Julière's model [19] and Simmons's model [20]. Moreover, for an improved accuracy, we integrate the dynamic conductance given by the Brinkman model [21] and we take into consideration the dependence of TMR upon bias voltage. In this model, all the physical quantities, such as the magnetization components ( $m_x$ ,  $m_y$ ,  $m_z$ ) are represented by voltages. Fig.3 shows a physical view and a block diagram of the model, with two modules, one dedicated to the computation of the dynamics of the magnetization and the other dedicated to the TMR.

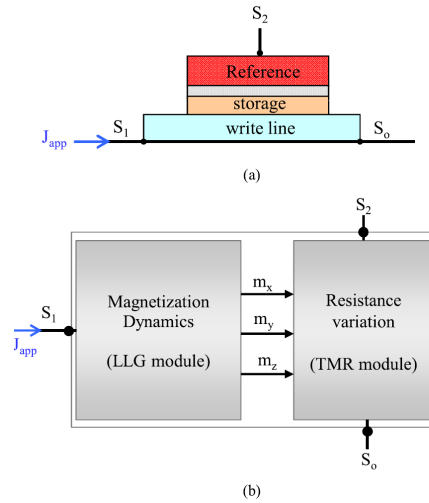


Fig.3: Modeling strategy of the three-terminal SOT-MTJ. (a) Physical view of the SOT-MTJ (cross section). (b) Block diagram of the compact model.

Fig.4 shows a simulation result using the SPECTRE electrical simulator of Cadence. It illustrates the operation of the device, by showing the dynamics of the  $m_z$  component of the magnetization for different values of the writing current density  $J_{app}$ . In this particular case, the magnetization of the two magnetic layers constituting the MTJ is oriented perpendicularly to the layers. The value of  $m_z$  is then 1 for P state and -1 for AP state. Intermediate values correspond to transient steps during the switching process. The duration of the writing pulse is 3ns. We see that during the application of the current pulse, the magnetization aligns in the plane of the layers ( $m_z=0$ ). Once the magnetization is stabilized, the current is removed and the magnetization switches in its final state according to the direction of the cur-

rent. For  $J_{\text{app}} = 10^{12} \text{A/m}^2$ , the SOT is not strong enough to initiate the switching and the MTJ remains in its P state. For  $J_{\text{app}} = 2 \cdot 10^{12} \text{A/m}^2$ , the 3ns pulse is not long enough for the magnetization to stabilize and the MTJ switches back to its initial P state. For higher values of  $J_{\text{app}}$ , switching occurs, with a duration decreasing with the increase of the current density, allowing a trade-off between speed and power consumption. In the same way, increasing the pulse duration allows improving the reliability of the switching. We see that for high current density values ( $4 \cdot 10^{12} \text{A/m}^2$  for instance), the switching time can be less than 1ns. In Fig.5, we see the influence of the external magnetic field on the switching. Without it, the switching is stochastic. When the field is applied, the switching becomes deterministic, with a switching time duration decreasing with the increase of the magnitude of the field.

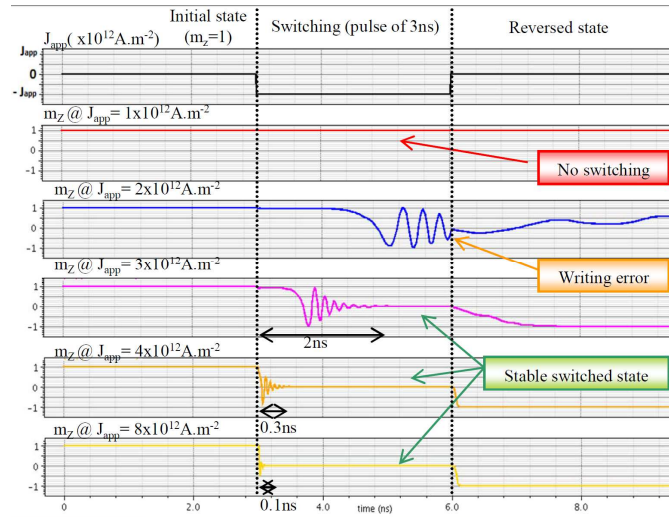


Fig.4: Simulation of the dynamic behavior of the SOT-MTJ perpendicular magnetization  $m_z$  according to the current



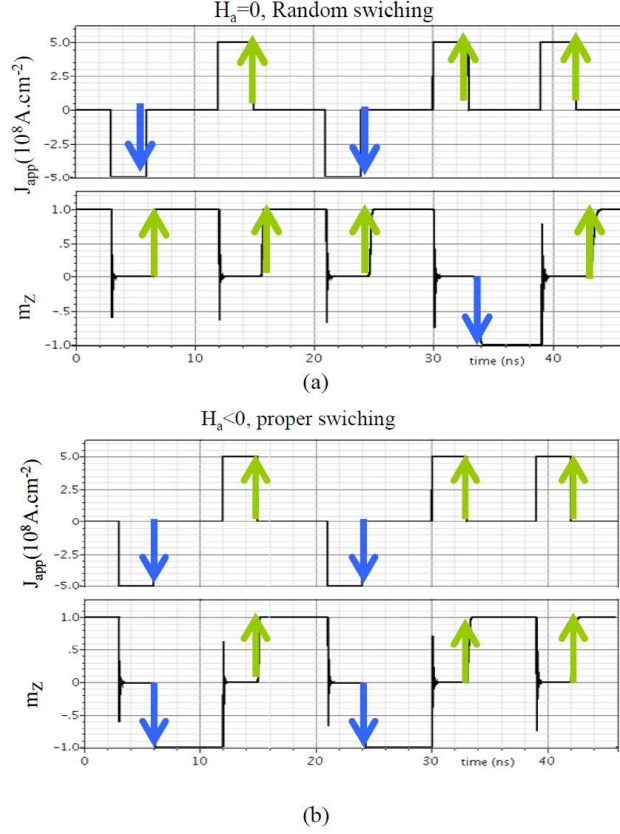


Fig.5: Study of the dynamic behavior of the perpendicular magnetization  $m_z$  according to the value of the external applied field  $H_a$

#### 4-2 Ultra-fast SOT-MTJ based Non-Volatile Flip-Flop

In order to illustrate the potential of SOT, we describe here a Non-Volatile Flip-Flop (NVFF) architecture based on this technology (Fig.6), developed at Spintec [22]. It is composed of a master latch made nonvolatile using a pair of SOT MTJs (Fig.6(b)) connected to a standard slave latch (Fig.6(c)). The operation is managed by a non-overlapping two-phase clock signal generator (ck1, ck2). Four transistors are used to generate a bidirectional current flowing in the SLs of the SOT-MTJs devices in series. The direction of the current is determined by the input data D. The current is generated during the first phase clock ck1. During the second phase clock ck2, the master latch reads the data of the SOT-MTJs and transfers it to the output Q. This operation is illustrated in Fig.7, showing a simu-

lation of the FF using the compact model presented in the previous section. In this work, the technology node is 40nm, for both CMOS and SOT. In these conditions, the writing current is extrapolated to 60uA, comparable to perpendicular STT-RAM. But as seen in inserts, the switching time is 250 ps, four times faster than STT, dividing the energy by four.

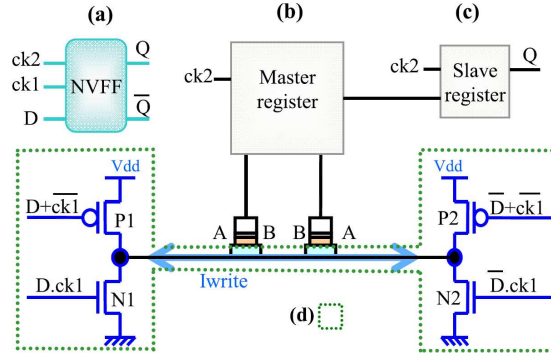


Fig.6: SOT-MRAM based NVMFF (a) symbol, (b) master register architecture (c) slave register, (d) writing circuit

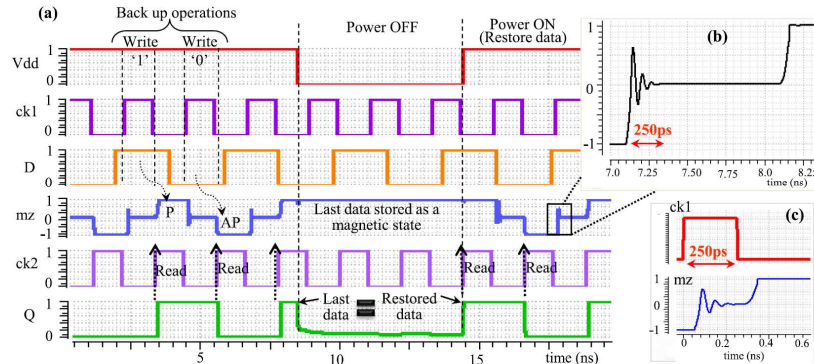


Fig.7: SOT-MRAM based NVMFF simulation results (a) write and read operations (b) perpendicular magnetization  $m_z$  behavior of the SOT-MRAM during a 1ns current pulse to switch from AP ( $m_z=-1$ ) to P ( $m_z=1$ ) (c) SOT-MRAM switching with only a 250ps pulse (exactly after oscillations stabilization)

The operation of this FF fundamentally differs from those presented so far [8], [9], [10]: the magnetic part is written at every clock cycle contrary to the previous cases, where the data was backed up in the magnetic part only when required, on demand. This is made possible because of the high writing speed and low-power consumption of the SOT technology. It means that with such a device, the power supply can be cut-off at any moment, without further action and restarted in the same state. This opens the door to the concept of “normally-off” or “instant-on” circuits [11]. This flip flop can be used as a primitive cell into the ASIC design li-

brary allowing the design of non-volatile, high speed and low-power digital circuits [23], [24].

### 4-3 System level integration

To evaluate the benefice that can be expected from integrating MRAM and in particular SOT-RAM in the different levels of hierarchy of processors, it is necessary to carry-out system level simulations, using processors simulators, like Gem5 or simple scalar. These tools take as inputs the architecture of the processor, including the memory hierarchy and the models of the memory blocks. It allows running an application and evaluating the performance in terms of CPU time, number of cycles, memory transactions (read/write, cache hit/miss...). The models of the memory can be provided by characterization of an existing memory (by test or simulation) or using a memory simulator, like NVSIM tool (specific for non-volatile resistive memories). This work is currently carried out for MRAM in general [7] and for SOT-RAM in particular, giving encouraging preliminary results [25].

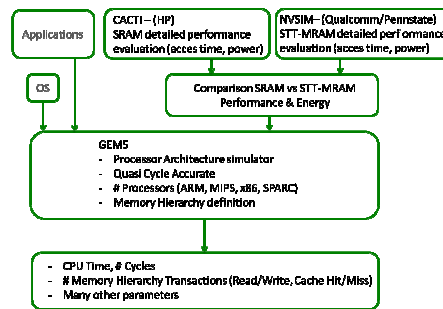


Figure 8: System level design flow to evaluate the performance of processors embedding MRAM

## 5 Conclusion

The advent of new MRAM generations has led to a keen interest in the microelectronics world for this technology as a possible solution to push forward the limits of microelectronics. A several tools are developed to allow exploring new circuits and system architectures using MRAM devices. As seen in this chapter, each both STT-RAM and SOT-RAM technologies has their own strengths and limits and is thus suitable for a given set of applications. A wide field of investigation is open which covers technology developments to improve the existing devices and discover new ones, and design of innovative circuits and systems. Two paths must be

followed in parallel: identifying relevant target applications for each technology and adapting the system architectures to gain maximum benefit.

The performance of the most recent technologies and in particular SOT-RAM, in terms of speed and power consumption which could compete with SRAM, paves the way towards a true “universal” memory. It allows dreaming of a new paradigm consisting in introducing non-volatility at all levels of the memory hierarchy and possibly writing the data in the MTJs at every clock cycle, opening the door to real normally-off/instant-on circuits.

### ***Acknowledgement***

This work has been partially funded by the European Commission under the spOt project (grant agreement n318144) in the framework of the Seventh Framework Program.

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