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***Abstract*—Many works are dedicated to power electronic transformers in order to replace line frequency transformers. These new converters offer many degrees of freedom to the designer (switching frequency, magnetic material, rated voltage for switches...). This paper presents a methodology to optimize the sizing of such power converters in order to compare different topologies for a given application. The proposed procedure maximises the efficiency of the converter under a limited volume. In this paper, the methodology is applied to compare different topologies of power electronic traction transformers (PETT) for railway applications. The considered case is a 2 MW converter supplied by a 25 kV-50 Hz catenary. The procedure is illustrated in simulation on a converter with 3.3 kV SiC switches. The best obtained efficiency is 98.9 % with 23 medium frequency transformers (MFT) of 28.6 L each.**

***Index Terms*—power electronic traction transformer (PETT), solid state transformer (SST), AC-DC multilevel converter, railway, traction, medium frequency transformer (MFT), optimisation, comparison**

I. Introduction

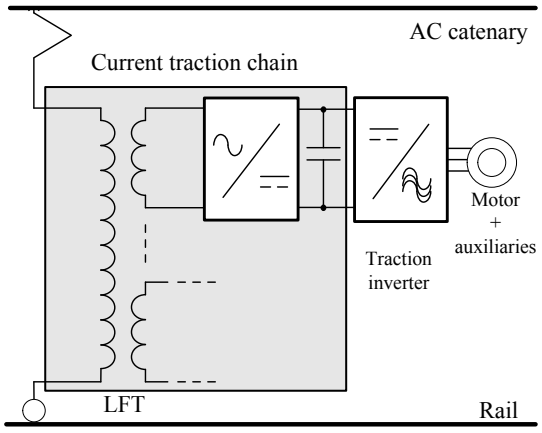
Currently, on-board converters on AC railway infrastructures are generally constituted by a low frequency step-down transformer (LFT), insulating the converter from the infrastructure voltage and lowering the supply voltage [1]. The output low AC voltages are transformed, by rectifiers connected on each secondary of the low frequency transformer, into DC voltages on the traction DC buses. Then, three phase inverters supply the traction motors and auxiliaries from the traction DC buses (Fig. 1(a)).

However, because of its low operating frequency (typically 16,7 Hz or 50 Hz), the input transformer is quite bulky and has a limited efficiency [1]. In order to increase the space for passenger accommodation, in particular on regional trains, a reduction of the converter volume is expected. As smaller transformers can be obtained with higher operating frequencies, new architectures of on-board converter including MFTs, called PETT (Fig. 1(b)), are studied to replace the current on-board converters [1]–[5]. However, to our knowledge, no procedure to size and compare different structures has been developed in the literature. Moreover, thanks to the development of high voltage SiC MOSFETs [6], SiC MOSFETs can be used instead of Si IGBTs in PETT topologies to increase the operating frequency without reducing the efficiency of the converter [7]. Thus, a methodology has to be developed to size PETT topologies in order to compare them, and, in particular, to confirm or refute the relevance of SiC MOSFETs utilisation in this application.

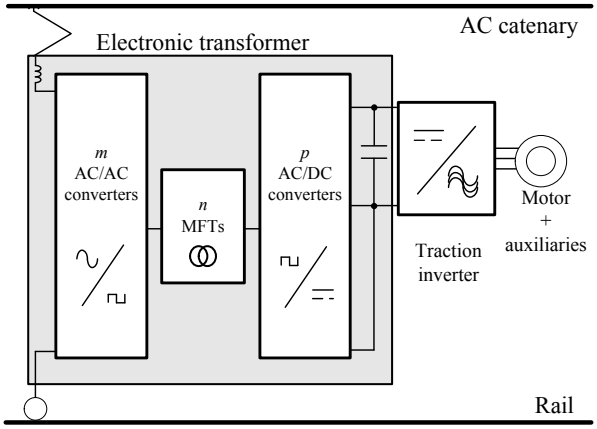
Different topologies of PETTs can be used to replace the converter with low frequency transformer. The classical diagram, shown on Fig. 1(b), is composed by an AC-AC conversion, elevating the frequency of the supply voltage to a few kilohertz. To withstand the supply voltage (typically 15 kV or 25 kV), several converters have to be connected in series on the catenary side. Then, the insulation of the converter and the step down in voltage are realised by a medium frequency transformer. On the secondary, the medium frequency AC voltage is transformed by a rectifier to supply the traction bus.

PETT topologies can be realised by different types of variants, defined by several structural elements:

- the general structure, usually sorted into direct or indirect topologies [3]. In direct topologies, the AC-AC conversion between the AC supply and the medium frequency transformer is achieved without intermediate DC buses, typically using matrix converters [8]. On the contrary, in indirect topologies, the AC-AC conversion is composed first by AC-DC converters in series on the AC side, such as cascaded 4Q converters, delivering DC-voltages on intermediate buses. DC-AC converters, such as H-bridges [9], [10] or half bridges [11], [12], then, convert the DC bus voltage into AC medium frequency voltage, supplying the primary of MFTs.
- the technology and the rated voltage of switches for every sub-converter: SiC MOSFETs, Si IGBTs...;
- the numbers of subdivisions (Fig. 1(b)): *m*, the number of AC/AC elementary converters connected in series on the catenary AC side, *n*, the number of MFTs and *p*, the number of AC-DC elementary converters connected in parallel on the traction bus. *m*, *n* and *p* can be different if multiwinding transformers are used. For example, $m = 6$ and $n = p = 3$ in [10] or $m = 8$ and $n = p = 1$ in [13];
- the structure of elementary converters, e.g. two or three levels, full or half bridges...;



(a) with low frequency transformer (only one rectifier shown)



(b) with medium frequency transformers

Fig. 1. Diagram of on-board converter topologies

- the structure of the AC-link of the insulated DC-DC converters: non-resonant, resonant, single-phase, multi-phase;
- the reversibility of the DC-DC converters: either dual active bridge (DAB) [14], when both primary and secondary are controlled, or "single active bridge" when only one bridge is controlled (primary bridge in traction mode and secondary bridge in braking mode).

One of the main limits of on-board converters is the losses, and thus, the cooling system requested to dissipate them. Thus, in the optimisation presented in this paper, the main criterion is the efficiency of the converter. In regional applications, as the converter is either under the frame or rooftop-mounted and, therefore, impinges on the space for passengers, its volume is also critical.

For direct topologies, the handling of the zero crossing of the current makes the control complex, in particular at low load [5]. Moreover, soft switching operations can be achieved in indirect topologies. Thus, the following study and comparison of PETT topologies for railway applications will be focused on indirect topologies, only.

The optimisation process is limited to indirect topologies with $m = n = p$, to focus on modular structures. Only full bridges are also considered, because of the rating of the available power modules. Afterwards, an insulated AC-DC elementary converter will be called a power electronic building block (PEBB). The general diagram of these topologies is shown in Fig. 2.

In this paper, a methodology to size PETTs in order to compare different topologies is developed. In a first section, the process to analyse and size the different variants and compare them will be detailed. The assumptions and equations used for the calculations will, in particular, be defined. The last section is dedicated to an application case. Some conclusions and perspectives will then close the paper.

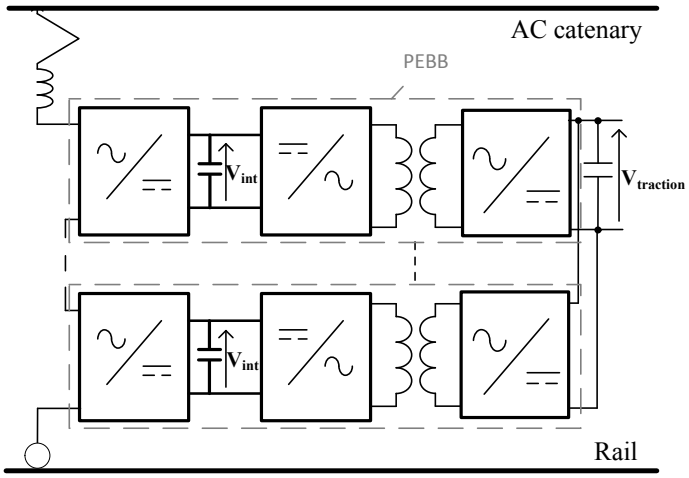


Fig. 2. Diagram of indirect topology of PETT with $m = n = p$

II. Topology optimisation methodology

A. General approach and hypothesis

The general approach of the sizing of each variant is described in Fig. 3. Each step will be developed in the following subsections. The losses in the capacitors will be neglected for the optimisation.

First of all, the nominal voltage of the intermediate buses, V_{int}, is determined in function of the highest admissible failure in time (FIT) rate of the switches of the input AC-DC converter, called an active front end converter (AFEC) afterwards. The number of PEBBs, m, is calculated in function of V_{int}, the maximum infrastructure voltage, $V_{AC,max}$, given by standard [15], the redundancy, and a margin, including the voltage at the terminals of the input filter.

Then, the frequency of the DC-DC converter, f_{DC-DC}, is optimised to minimise the losses both in the switches and in

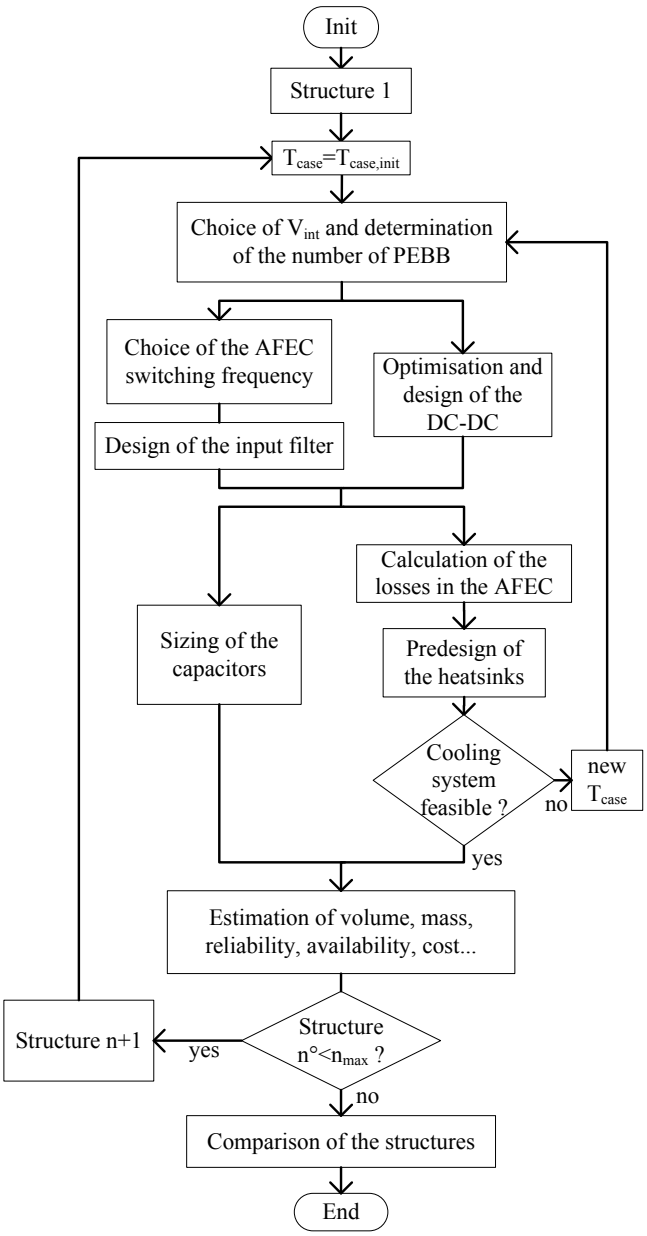


Fig. 3. Global flowchart of the comparison of PETT topologies

the MFT. Next, the capacitors on the intermediate buses are sized and the losses in the AFEC are calculated.

Afterwards, appropriate heatsinks and the cooling system have to be sized roughly to ensure the desired case temperature. If this phase results in an aberrant or infeasible cooling system, the study is carried out a second time with a higher case temperature corresponding to a feasible cooling system.

The global efficiency of the structure is then calculated. The mass and the volume of the structure are estimated. After that, the same methodology is applied on the other topologies. Once all the components of the structures are sized, they can be compared on different criteria.

Once the topologies of electronic transformers are sized to optimise the efficiency, the cost, volume, mass, intrinsic reliability, and availability have to be estimated thanks to a "bottom-up" approach. Thus, breaking up the converter into elementary sub-systems and basic components, a rough estimation of the cost, the availability and the mass of each component can be made.

In power applications, the components with the highest failure rates are power modules, gate drivers and capacitors [16], [17]. Thus, the intrinsic reliability can be only evaluated for these components, analysing their FIT rate and the number of each of them.

Contrary to the mass of the converter, it has little sense to consider only the individual volumes of the components, as the volume is mainly constraint by the insulation distances. However, the first step is to assess the volume of each component, either from manufacturer data or calculations. Then, some insulation distances can be taken into account by filling coefficients to estimate roughly the volume of the converter.

B. Insulated DC-DC optimisation

1) MFT sizing: The first step of the DC-DC optimisation is the sizing of the MFT for each frequency. To do this, the tolerated range of the leakage inductance, L_{MFT}, is calculated in function of the power of the DC-DC, P_{DC-DC}, and either the realisable phase-shift, δ in radian or the corresponding time $t_\delta = \frac{\delta}{\omega}$, in term of control, between the primary and secondary bridges in DAB mode (see (1) in resonant mode [18] and (2) in non resonant mode [19]) or the tolerated increase of the intermediate DC buses voltage otherwise, as developed in [18], [20].

$$P_{DC-DC} = \frac{8 V_{int} V_{traction}}{\pi^2 k_t Z_{R-DAB}(\omega)} sin(\delta) \tag{1}$$

$$P_{DC-DC} = \frac{V_{int} V_{traction}}{k_t Z_{NR-DAB}(\omega)} \delta \left(1 - \frac{\delta}{\pi}\right) \tag{2}$$

where ω and ω_{res} are respectivelly the switching frequency of the DC-DC and the resonant frequency of the AC-link in resonant mode, $Z_{R-DAB} = \omega L_{MFT} \left(1 - \left(\frac{\omega_{res}}{\omega}\right)^2\right)$ and $Z_{NR-DAB} = \omega L_{MFT}$ are respectively the impedances in the resonant and non resonant DABs, $V_{traction}$ is the traction bus voltage (Fig. 2) and k_t is the transformer turns ratio.

Then, several pre-designs of MFT are analytically calculated thanks to the improved generalized Steinmetz equations [19], [21] and taking into account skin and proximity effects in the windings thanks Albach 1D models described by equations (27) and (28) from [22]. The inputs are the frequency, the insulation voltage depending on the catenary voltage [15], the voltage and current waveforms, analytically calculated in function of the power, the DC-DC structure and the optimal leakage inductance (1) or (2). Each pre-design corresponds to a different set of values of induction inside the material, current density inside the windings and number of turns. A selection is applied on the results to eliminate unacceptable

designs in term of volume, power density, leakage inductance or maximum temperature. Finally, the MFT with the best efficiency validating these criteria is selected.

2) Calculation of the losses in the switches: Once the medium frequency transformer has been sized, the losses in the switches can be calculated. The insulated DC-DC converter is controlled to operate in zero voltage switching (ZVS) mode [18]. As switches have not been dynamically tested in soft switching, the turn-on losses will be neglected in ZVS mode.

The junction temperature is initialised at the case temperature. For this temperature, the switching and conduction losses are calculated in function of the characteristics of the switches, the switching frequency and the switched and RMS currents, which depend on the structure of the DC-DC converter (resonant/non-resonant, two/three levels, full/half bridges…) [23], [24].

The thermal power corresponding to the heating of the switches is then estimated both at the primary and at the secondary of the insulated DC-DC converter. To do that, it is assumed that the case is maintained at a constant temperature, T_{case}, by the cooling system. Then, the theoretical maximal dissipated power, P_{th}, can be calculated in function of the thermal coefficient, $R_{th,jc}$, between the junction of the die and the case (3).

$$P_{th} = \frac{T_{junction} - T_{case}}{R_{th,jc}} \tag{3}$$

If the calculated theoretical power, P_{th}, dissipated at the junction temperature is lower than the losses in the switches, the junction temperature is increased and the calculation of the losses in the switches reiterated until the thermal steady state is reached. If the junction temperature oversteps a maximum temperature, defined in function of the switches, two power modules are connected in parallel and the calculation is computed again.

3) Optimisation of the DC-DC frequency: Once the DC-DC converters has been sized for all the frequency range, the switching frequency assuring the highest efficiency of the DC-DC converter is determined.

C. Calculation of the losses in the AFEC

The AFEC switches are controlled by phase-shifted pulse width modulation (PWM) to reduce the total harmonic distortion (THD) [25]. Thus, harmonics are rejected into the catenary at frequencies centred around multiples of $2mf_{AFEC}$, where f_{AFEC} is the switching frequency of the AFEC. In order to comply with standards [26] and railway company templates, f_{AFEC} has to be chosen to eliminate harmonics at some frequencies, such as frequencies used for track signalling.

Once the DC-DC converters is sized, the losses in the AFEC switches are calculated for the maximum current, i.e. at nominal power and minimum supply voltage [23], [24].

As for the sizing of the DC-DC converters (see subsection II-B2), the calculations are carried out until thermal steady state is reached.

D. Sizing of the intermediate capacitors

On the AC side of the AFEC, the instantaneous power supplied to the converter is the sum of a constant term and an alternating component at twice the network frequency. On the DC side, the power drawn by the DC-DC converters is constant. Thus, the fluctuating power has to be absorbed by the intermediate capacitors, resulting in ripple in the DC bus voltage.

These ripples rejected into the catenary by the AFEC switchings, generates low frequency harmonics. Moreover, if the ripple is too important, the reliability of the AFEC switches can be reduced due to overvoltages. Thus, to comply with harmonic standards [26] and to avoid lowering the reliability, the capacitance, C_{int}, has to be sized to assure a minimum voltage ripple ΔV_{int} on the intermediate buses (4) and (5).

$$P_{2f} = P_0\sqrt{1 + \left(\frac{2Z_{filter}P_0}{mV_{AC}^2}\right)^2} \tag{4}$$

$$P_{2f} = 2\omega_0\Delta E_{2f} = 2\omega_0 m C_{int} V_{int}\Delta V_{int} \tag{5}$$

The capacitance, C_{int}, is sized in steady-state, i.e. for a power factor of 1. P_0 and P_{2f}, are respectively the nominal and ripple powers of the converter, ΔE_{2f}, the ripple energy, V_{AC}, the supply RMS voltage, Z_{filter}, the impedance of the input filter, either a inductor (Fig.2) or a LCL filter [27], ω_0, the network frequency, and m, the number of elementary AC-DC converters in the AFEC.

III. Application

A. Presentation of the considered variant

The optimisation process presented in section II is illustrated on a variant. The cost, reliability and availability are not estimated in this paper. The AFEC is composed by cascaded two-level H-bridges. The DC-DC converters are resonant DAB (R-DAB) with a resonant frequency, f_{res}, smaller than the switching frequency f_{DAB} $\left(\frac{f_{res}}{f_{DAB}} = 0.85\right)$. Both primary and secondary are realised by two-level full-bridges. 3.3 kV SiC MOSFETs without anti-parallel diodes are used both in the AFEC and in the DC-DCs. The drain-source on-state resistance and the switching energies used for the calculations come from [6]. The repartition between turn-on and turn-off energies has been extrapolated from the values at 450 A given in Table 3 of [6].

The targeted converter is a 2 MW electronic transformer converting a 25 kV-50 Hz voltage into a 1.8 kV DC voltage.

B. Optimisation results

To comply with 3.3 kV MOSFETs FIT rates, the intermediate bus voltage has been chosen equal to the traction voltage, i.e. 1.8 kV. Thus, a minimum of 23 PEBBs is requested to withstand the supply voltage.

First of all, different designs of MFTs with Litz wires, resin insulation, forced air cooling and either nano-crystalline or ferrite core, have been compared for frequencies from 1 kHz to 15 kHz. Designs with a volume higher than a maximum

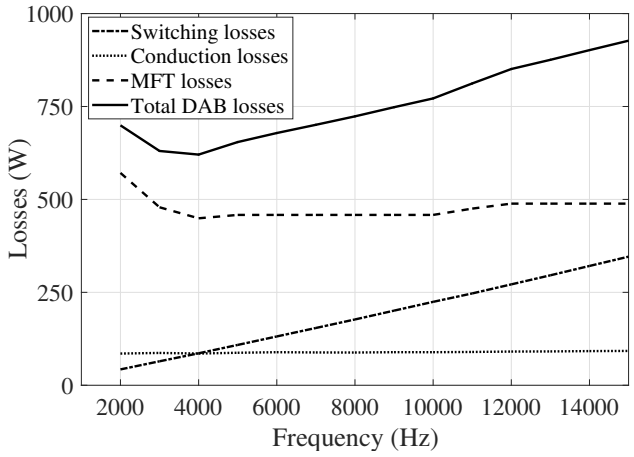
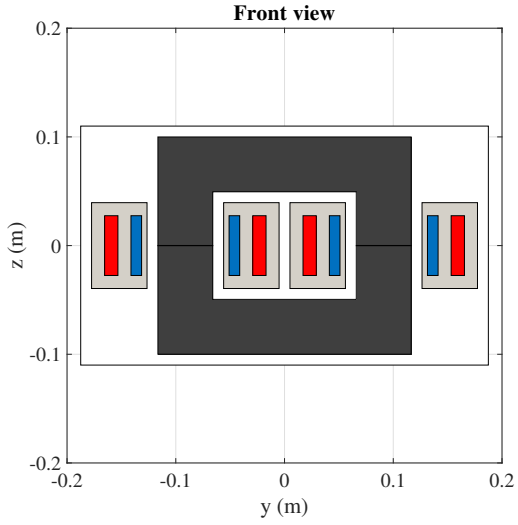


Fig. 4. Losses in the R-DAB in function of the frequency at the nominal power ($P_{PEBB} = 87\ kW$). For each frequency, the MFT with the best efficiency, complying with the constraints, has been chosen.

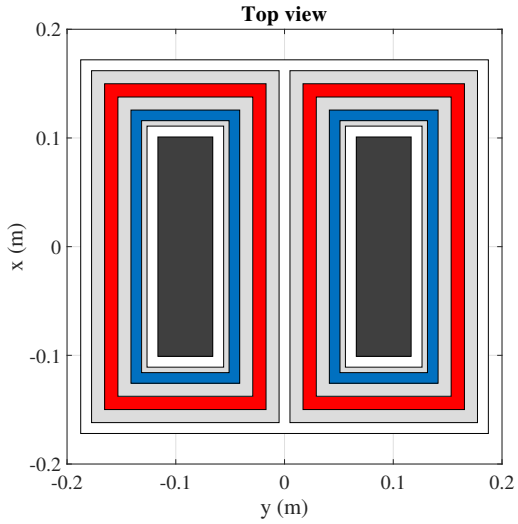
volume defined to comply with the reduction of the total volume of the converter, i.e. 30 litres each transformer in this application, have been eliminated. Only designs with a leakage inductor for a t_δ higher than 2 μs (1), have been kept. Then, for each frequency, the design with the highest efficiency at nominal power, satisfying these constraints has been selected. At the lowest frequencies, the MFTs with the best efficiencies have a nano-crystalline core. At higher frequencies, ferrite core MFTs give the best efficiency but operate at lower induction. The losses in the selected MFTs are shown in Fig. 4 for frequencies between 1 kHz and 15 kHz. The efficiency of the transformer is limited by the volume constraint at low frequency. One can, in particular, notice that no design of MFT complied with the constraints for an operating frequency of 1 kHz: either the MFT was too bulky or the leakage inductor did not satisfy the specification.

Then, the losses in the primary and secondary bridges of a DAB are analytically calculated for every frequency in function of the leakage inductor of the selected MFTs and the resonant capacitor. The calculations are validated in simulation. An example of the current in the primary of the MFT is shown in Fig. 6. The switching and conduction losses and the total losses in a DAB are shown in Fig. 4 in function of the frequency. The conduction losses in the switches are dependent on the junction temperature. However, even if the total losses increase with the frequency, the increase of the temperature is rather small. The conduction losses are thus almost constant. On the other hand, as leakage inductances are constrained, the switching currents do not vary much in function of the switching frequency. As the junction temperature is not taken into account to calculate the switching losses, they rise nearly linearly with the frequency.

In low frequency, the volume constraint on the MFT limits the total efficiency of the DAB. For higher frequency, on the other hand, the efficiency is limited by the switching losses in the primary and secondary bridges. The frequency matching



(a) front view



(b) top view

Fig. 5. Diagram of the chosen MFT. Core in dark grey, primary and secondary windings respectivelly in blue and red, resin in light grey.

the best efficiency of the DAB is then a compromise between the power density of the MFT and the increase of the switching losses with the frequency. This frequency, i.e. 4 kHz in this case, will be used afterwards.

Schematic front and top views of the chosen medium frequency transformer are represented in Fig.5. One can especially notice the important share of resin compared to windings. This is due to the fact that every MFT has to withstand the whole catenary voltage.

The losses in the AFEC for a switching frequency of 450 Hz, and then the total losses in the converter are calculated at the nominal power. Fig. 7 shows the repartition of the losses in one PEBB of the converter. The parameters of the optimum PETT are listed in Table I.

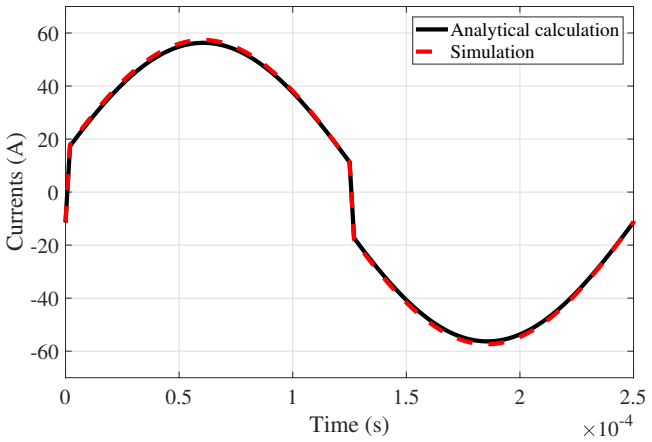


Fig. 6. Current at the primary of the R-DAB obtained analytically and in simulation ($P_{PEBB} = 87\ kW$ and $f_{DC-DC} = 4\ kHz$).

One can notice conduction losses much higher in the AFEC than in the DAB primary and secondary. This is due to the higher RMS current in the AFEC (i.e. 80 A_{RMS} in the AFEC compared to 43 A_{RMS} in the DAB), as the ripple power flows through the AFEC but not through the DAB for well-chosen intermediate capacitances (see subsection II-D). The gap between AFEC and DAB conduction losses is wider, as the MOSFET on-state resistance increases with the temperature. One can also see that the switching losses in the AFEC and the DAB primary or secondary are commensurable, even if the AFEC switching frequency (i.e. 450 Hz) is almost nine times smaller than the DAB switching frequency (i.e. 4 kHz). However, as the DAB operates in ZVS mode contrary to the AFEC, only the turn-off losses contribute to the DAB switching losses. As the currents in the primary and secondary switches are the same, the small difference between the switching losses in the primary and the secondary of the R-DAB is only due to the fact that the primary do not switch at the same moment, thus do not switch the same current than the secondary.

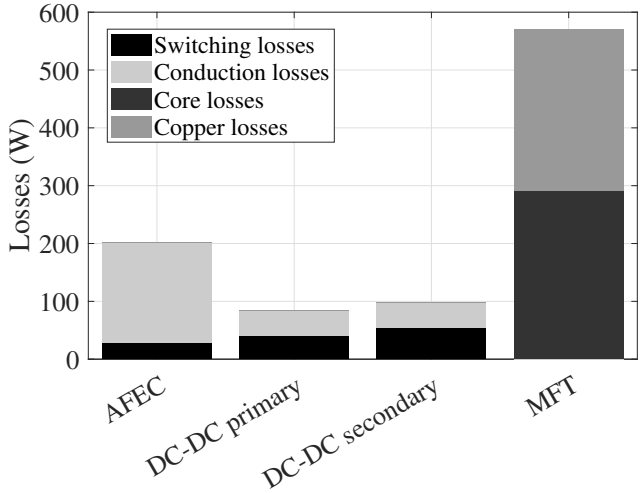


Fig. 7. Repartition of the losses in one PEBB at the optimum frequency ($f_{DAB} = 4\ kHz$) and the nominal power ($P_{PEBB} = 87\ kW$)

TABLE I
CHARACTERISTICS OF THE CHOSEN DESIGN OF PETT

Number of PEBBs	$m = n = p = 23$
Intermediate capacitances	$C_{int} = 1.7\ mF$
AFEC switching frequency	$f_{AFEC} = 450\ Hz$
DAB optimum switching frequency	$f_{DAB} = 4\ kHz$
MFT materials	Nano-crystalline
Diameter of a strand of a Litz wire	$0.1\ mm$
Number of strands in a Litz wire	3000
Maximum induction	$B_m = 0.8\ T$
Number of turns	$N_1 = N_2 = 32$
MFT leakage inductance	$L_{MFT} = 239\ \mu H$
Resonant capacitance	$C_{res} = 9.2\ \mu F$
Total efficiency of the converter	$\eta = 98.9\ \%$

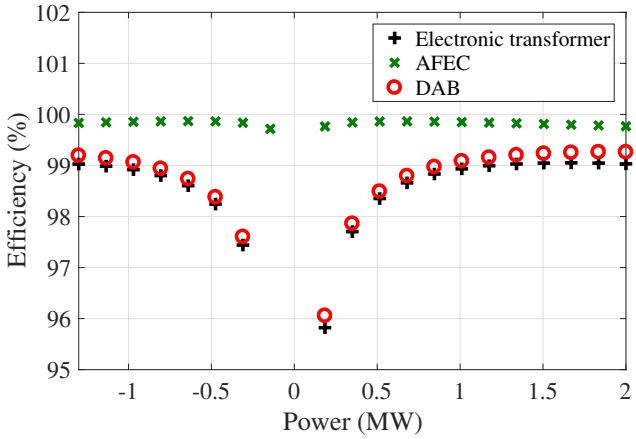


Fig. 8. Efficiency of the converter at the optimum frequency ($f_{DAB} = 4\ kHz$) in function of the power drawn by the converter

Then, the efficiency of the PETT has been calculated for different power levels from the nominal traction power, i.e. 2 MW (1.65 MW for traction and 350 kW for the auxiliaries) to nominal braking power, i.e. -1.3 MW. The results are shown in Fig. 8.

The minimum capacitance on the intermediate buses has been calculated in steady state, i.e. for a power factor of 1, and for a maximum ripple of 5 % of the nominal intermediate voltage (5). The resulting 1.7 mF capacitor can be realised thanks to film capacitor technology with a typical volume and a mass of approximatelly 9 L and 15 kg, respectivelly [28].

Table II gathers the number of elements and a rough estimation of the volume and the mass of the main components for a further analysis.

IV. CONCLUSION

A methodology to design and compare on-board power electronic transformers for railway applications has been presented. The specifications and the range of the study have been exposed in introduction. Then, the process proposed to optimise the design of every topology variant has been developed.

TABLE II
ESTIMATION OF SOME PARAMETERS OF THE CHOSEN DESIGN. THE VOLUME AND MASS ARE GIVEN FOR ONE COMPONENT AND FOR ALL COMPONENTS IN BRACKETS.

Components	Number of components	Volume	Mass
SiC power modules (3.3 kV MOSFET) and gate drivers	276	$0.7\ L$ $(193\ L)$	$0.8\ kg$ $(221\ kg)$
Intermediate capacitances	23	$9\ L$ $(207\ L)$	$15\ kg$ $(345\ kg)$
MFTs	23	$28.6\ L$ $(658\ L)$	$44.8\ kg$ $(1030\ kg)$

The first step consists in determining the switching frequency of insulated DC-DC converter to optimise its efficiency under volume constraints. Then, the losses in the total converter are calculated and other criteria, such as volume and the mass have been estimated to compare PETT variants.

An example is then presented on a 2 MW electronic transformer built with 3.3 kV SiC MOSFETs. In particular, the repartition of the losses in the optimum design is exposed.

V. PROSPECTS

In this paper, the optimisation of the design is made for the nominal power of the converter. However, for some typical railway applications, such as regional trains, the power drawn by on-board converters can be highly variable. Thus, it could be interesting to optimise the design of PETT taking into account the variations of the power on a typical route.

It has been considered that, when in soft switching, the turn-on losses in ZVS mode can be neglected. However, this hypothesis should be validated or improved by soft switching characterisations of MOSFETs. Moreover, to improve this study, the case when the DC-DC converters operate in hard switching mode, i.e. when the current drawn by the converter is not sufficient to ensure ZVS operation, should be taken into account. Thus, the impact of the magnetizing current, which was neglected here, should be analysed [29].

The input filter, typically a LCL filter [9], [27] or an inductor, has also to be sized to comply with the circuit breaker, control specifications, harmonic standards and the tolerated psophometric current [26], [30].

The SiC MOSFETs with high breakdown voltages, which are considered in this study, are still being developed. Thus, only few data are currently available and the results of this methodology are highly dependent on the validity of these data and the approximation made from them. Hence, it has to be taken into account when comparing the results.

Then, the cost performance analysis should be carried on each structure to determine some characteristics of the converter, such as the cost, the availability, the reliability or the volume.

VI. ACKNOWLEDGEMENT

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