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Yann Deval, Andrés Asprilla, David Cordova, Herve Lapuyade, Francois Rivet. DLL-Enhanced PLL Frequency Synthesizer with Two Feedback Loops and Body Biasing for Noise Cleaning. IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Oct 2018, Qingdao, China. hal-01964932

HAL Id: hal-01964932

<https://hal.science/hal-01964932>

Submitted on 10 Jan 2019

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DLL-Enhanced PLL Frequency Synthesizer with Two Feedback Loops and Body Biasing for Noise Cleaning

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Abstract - This paper presents the relevant aspects of the design of an ultra-low-power frequency synthesizer based on the combination of two feedback loops, a Phase-Locked Loop (PLL) acting together with a Delay-Locked Loop (DLL) to perform fine and coarse tuning of the desired output frequency, respectively. The objective of the circuit is to achieve a power consumption lower than 100 μ A to generate a 2.5 GHz output frequency, improving the poor phase-noise of ring oscillators with the usage of the DLL circuit as an auxiliary feedback loop to cancel the phase noise and adjusting the VCO frequency through the body bias feature, available in the 28 nm FDSOI technology from STMicroelectronics.

1. Introduction

Frequency synthesizers are essential building blocks of Integrated Circuits. They are used in a variety of applications such as clock generators, local oscillators, demodulators, etc. Nowadays, with the rise of the Internet of Things (IoT), power consumption is becoming a critical concern for battery-powered and energy-harvested devices, because power and performance requirements are highly constrained [1]. Typically, frequency synthesizers made-up by Phase-Locked Loops (PLL) operate in the milliwatt range of power consumption, which is critical for battery-powered devices, whose battery life is reduced by the operation of synchronous circuits [2].

On the other hand, Phase-Locked Loops can use two types of voltage-controlled oscillators (VCO) in order to generate the desired output frequency: an LC resonator which uses a negative-resistance component to compensate its energy losses during the oscillation and to ensure the Barkhausen criteria [3]. These types of oscillators have low phase noise; however, they consume an important amount of power and area, being expensive to be integrated. The other family of VCOs is composed by tunable ring oscillators, which occupy less area into the chip because they only use CMOS devices and positive feedback to generate the oscillation condition, being easier to be integrated into low-area circuits. They also consume less power compared to the first family of oscillators. However, the phase noise is high and, they are more susceptible to process variations, affecting their output frequency after fabrication due to undesired intrinsic parasitic components [4].

In this paper, a novel architecture for frequency synthesis based on a DLL-enhanced PLL is presented. The developed architecture takes the advantage of low-power consumption feature of VCOs composed by ring oscillators and improves the phase noise through the usage of two feedback loops: the first one is composed by a Delay-Locked Loop (DLL) that helps to cancel the phase noise of the output frequency of the ring oscillator and performs a coarse tuning of the desired output frequency, and the second one is a Phase-Locked Loop (PLL), which uses the back body biasing technique, exclusive of the FDSOI devices to perform the fine tuning of the output frequency. The designed unit consumes around 100 μ W of power, being suitable for ultra-low-power applications.

An initial version of the frequency synthesizer was sent to fabrication and its performance was measured, detecting some possible improvements that were done to ensure the correct locking of both loops, to improve the phase noise of the output and to reduce the requirements of the reference frequency, reducing the number of external components required to test the circuit. The proposed improvements will be presented in this paper, along with simulation results.

The structure of this work is presented as follows: Section 2 introduces the circuit architecture, showing the most important building blocks of the proposed architecture. Then, in Section 3, the first measurement results and analysis are presented, introducing the detected drawbacks of the first version sent to fabrication. Section 4, shows the proposed improvements of the first version, also presenting the results of transient simulations of the improved circuits, and finally, some conclusions of this work are drawn.

2. Circuit Architecture

The developed frequency synthesizer is composed mainly of two feedback loops: A Phase-Locked Loop (PLL), whose VCO is pre-biased by an auxiliary feedback loop, a Delay-Locked Loop (DLL). Figure 1 shows the block diagram of the circuit. In general terms, the DLL loop performs a pre-tuning and noise cleaning of the output frequency, and the PLL block sets the output frequency to the correct value.

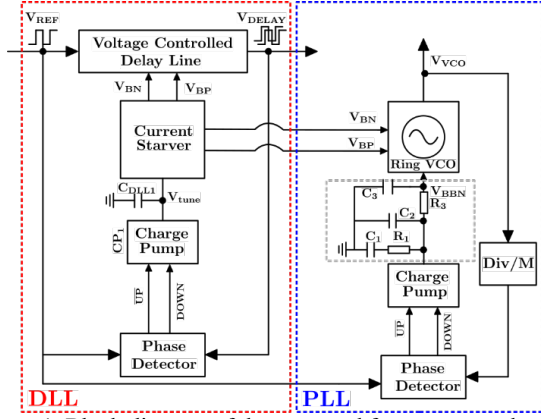


Figure 1. Block diagram of the proposed frequency synthesizer

As seen in Figure 1, the reference frequency (V_{REF}) is used in both feedback loops. The first loop, the DLL, receives the input signal and synchronizes the delay of the voltage-controlled delay line (VCDL) to be one period of the input signal. Also, the PLL uses the reference frequency to synchronize the VCO frequency, which is pre-tuned using the biasing voltages from the VCDL and finally tuned by the PLL. The system is designed to have a 2.5 GHz output frequency using a 48 MHz reference, being the relation between the output and input frequency $M = \frac{f_{out}}{f_{in}} = 52$.

To generate the desired output frequency, a VCO based on an adjustable ring oscillator is used. The oscillator consumes low power and is area-efficient, however, its phase noise is high [4] [5]. For this work, the noise is previously cleaned using the DLL, increasing the performance in terms of phase noise and compensating the process variations.

As the output period is $2 \cdot \Theta_0 = 400$ ps, the VCDL block is composed of 104 cascaded delay elements. Each delay element is an odd chain of current-starved inverters, as seen in Figure 2. When the loop is locked, the biasing voltages in the VCDL are used to set the bias voltages for the VCO of the PLL, which is a self-looped delay element tuned to have 400 ps of oscillation period. The fine frequency tuning is done through the PLL, which adjusts the frequency of the VCO through the body bias technique, available in FDSOI devices. As seen in Figures 1 and 2, the oscillation frequency of the VCO is controlled by three voltages: V_{BN} , V_{BP} , and V_{BBN} .

The PLL feedback loop contains a phase-frequency detector (PFD), a charge pump, a loop filter composed by an RC network, and finally an integer frequency divider, which divides the output frequency by the factor M in order to generate a signal that will be compared to the reference in phase and frequency. The error signal, controlled by the loop filter is the body bias voltage.

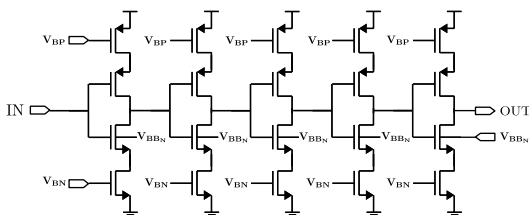


Figure 2. Delay element used for the VCDL of the DLL and the VCO of the PLL

3. Detected issues

The circuit was sent to fabrication using the 28 nm FDSOI technology from STMicroelectronics and its performance was measured, detecting some issues in the locking of the DLL. The first issue was related with the transition time of the reference clock. The rise time of the reference should be 200 ps maximum to be compared with the output signal coming from the VCDL. With a slow rising edge, the DLL is not able to be synchronized with the signal coming from the delay line and the reference through the PFD block, causing problems with the locking of the loop and degradation of the output signal, as shown in Figure 3.

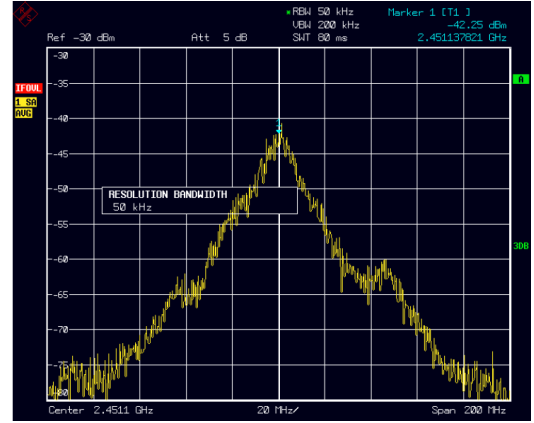


Figure 3. Output signal spectrum of the fabricated chips

Another important issue related with the locking of the DLL is related to the transient behavior of the circuit. At the beginning of the operation, a rising edge of the reference enables the 'UP' signal of the charge pump, charging the loop filter capacitor at the rate $\frac{\Delta V_{tune}}{\Delta t} = \frac{I_{cp}}{C_{LF}}$. A rising edge coming from the VCDL deactivates the 'UP' signal, keeping the tuning voltage (V_{tune}) constant. If the tuning voltage starts high, the initial 'UP' signal is enabled, the capacitor keeps its voltage and the VCDL remains in the lowest delay. An initial condition should be added to the loop filter to tune the VCDL in the highest delay and avoid locking issues due to the loop filter initial voltage.

4. Improvements and Simulations

Based on the issues described previously, some improvements to the architecture were proposed and a new version of the circuit was sent to fabrication. For the first detected issue, two input buffers were added before the phase comparator input of the DLL and the PLL respectively. With these buffers, the electrical constraints for the reference frequency were reduced and sinusoidal input signals can be used to test the circuit.

The second issue related with the initial voltage of the DLL loop filter was solved using an NMOS in series to the loop filter capacitor. When an external control signal is enabled, the loop filter is discharged and the VCDL will start correctly. Also, a third-order loop filter for the PLL was designed to decrease the jitter of the output frequency due to high-frequency spurs caused by the ripple of the loop filter voltage of the PLL.

Figure 4 shows the transient simulation results for the DLL, where the loop filter voltage, the reference, and the VCDL voltages are plotted to see the correct locking of the circuit using the correct initialization sequence.

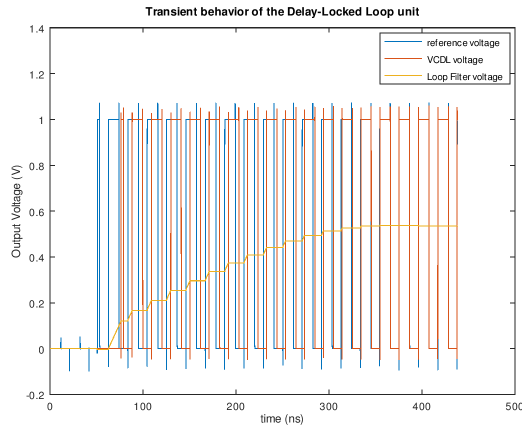


Figure 4. DLL block transient simulation

Figure 5 shows the loop filter voltage response for the PLL, showing the influence of the third-order loop filter in the VCO tuning voltage. Also, Figure 6 shows the power spectrum of the output frequency.

5. Conclusions

An alternative frequency synthesizer based on the combination of a double-feedback loop to improve the VCO performance was presented in this work. The circuit is intended to work in ultra-low-power applications, being an interesting option to be integrated into low-power circuits. The usage of double-feedback ring oscillators gives a versatile solution for reducing the phase noise of the oscillation frequency, being a suitable solution for local oscillators and clock generation units.

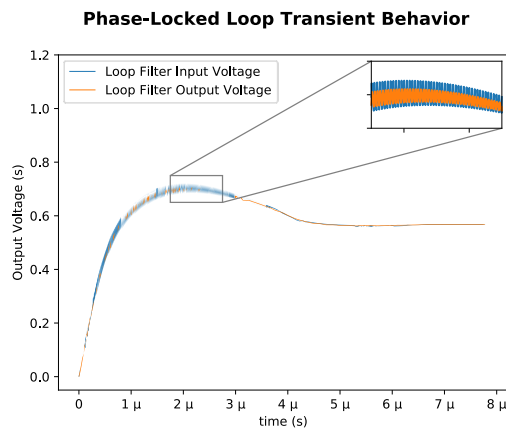


Figure 5. PLL loop filter transient simulation

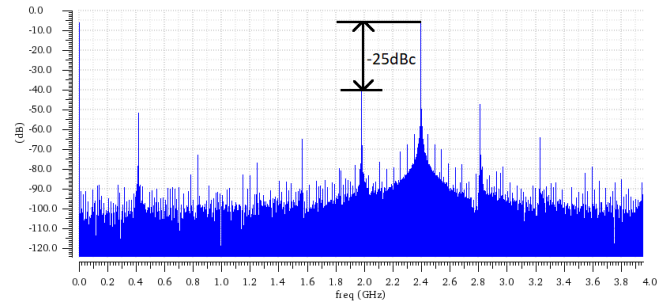


Figure 6. Output frequency power spectrum

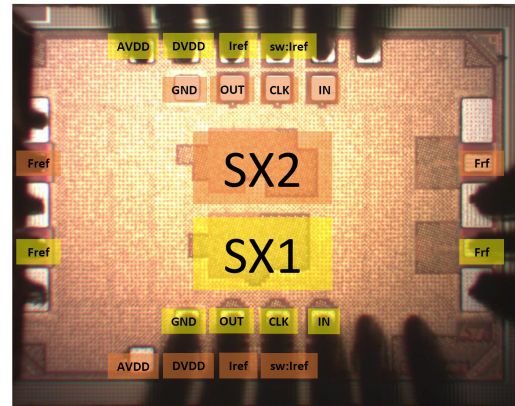


Figure 7. Die photography

Acknowledgments

The authors would like to express their acknowledgment to the THINGS2DO project for the financial support, also to STMicroelectronics, for the fabrication of the circuits presented herein.

6. References

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