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An Optimal Design for a MOS Varactor using Artificial Bee Colony Algorithm

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Voltage Controlled Oscillators (VCOs) are the important blocks in such circuits as Phase Locked Loops (PLLs) used in telecommunication systems [1]. Some characteristics of a VCO, like low phase noise or high quality factor performances, depend on the characteristics of the varactors. To have powerful features, the VCO requires an optimal design of the varactors. For this purpose, we use the EKV transistor model [2] as an analytical simulation model for the C-V characteristics of the varactor and Artificial Bee Colony (ABC) algorithm [3] as an optimization tool.

Artificial Bee Colony algorithm is nature-inspired metaheuristic, which imitates the foraging behavior of bees, and we chose it over other metaheuristic because is easy to implement, has fewer control parameters, and could easily be modified and hybridized with other metaheuristic algorithms. The ABC consists of three groups of artificial bees: employed bees, onlookers and scouts.

The onlooker bees select a food source with the probability given in (1):

$$P_i = \frac{fit_i}{\sum_{j=1}^N fit_j} \quad (1)$$

In order to produce a candidate food position from the old one, the ABC uses the following expressions (2) and (3):

$$V_{ij} = x_{ij} + \phi_{ij}(x_{ij} - x_{kj}) \quad (2)$$

$$X_{ij} = X_j^{\min} + (X_j^{\max} - X_j^{\min}) * \text{rand}(0,1) \quad (3)$$

The circuit that we use in our work is an inversion mode NMOS varactor [4], it realized from MOS transistor (Fig.1). So in order to evaluate the quality of the varactor design, an objective function that's the quality factor (Q) is defined in the following expression.

$$Q = \frac{1}{2\pi fRC_{\text{Total}}} \quad (4)$$

The total varactor capacitance can be determined by:

$$C_{\text{Total}} = C_{\text{GS}} + C_{\text{GD}} + C_{\text{GB}} + C_{\text{extrinsic}} \quad (6)$$

And,

$$R = R_{\text{poly}} / \text{square} \frac{1}{N_f^2} \frac{W}{L} \quad (5)$$

With W is the transistor width, L is the transistor length and N_f is the number of fingers, should be optimized in order to maximize the quality factor Q.

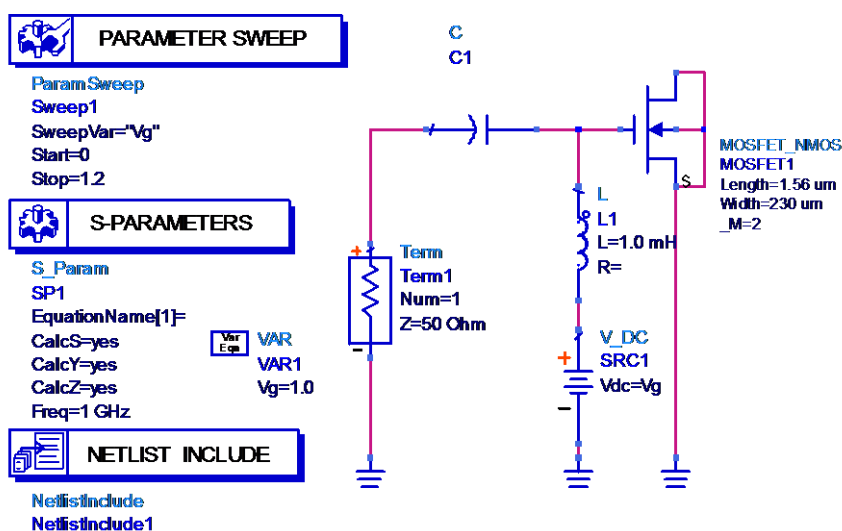


Figure 1. Bias circuit design of NMOS varactor

The following table shows the optimization results given by the ABC technique and a comparison with the already published work results. Figures 2 show the C-V characteristics of the varactor under the ADS tools for 1.0 GHz and the figure 3 the simulation of the Q factor.

Table 1. Results & Comparison

Design Parameters	ABC Algorithm	Evolutionary Algorithm [5]
W (μm)	230	233.68
L (μm)	1.56	1.44
Nf	40	39
C_Model (pF)	1.78	1.78
Q	127	110

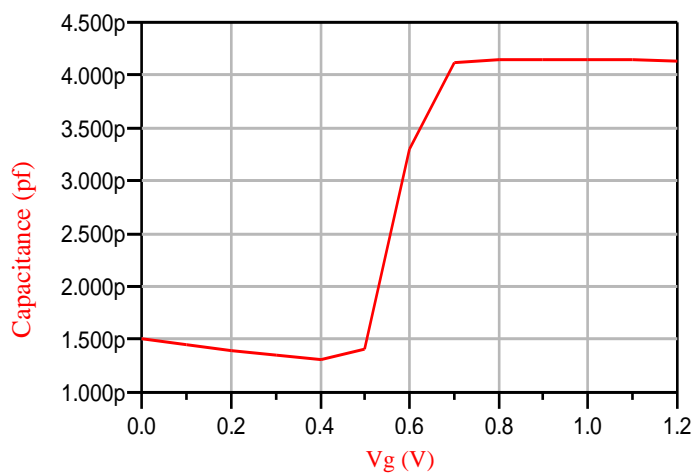


Figure 2. Capacitance behaviour of varactor

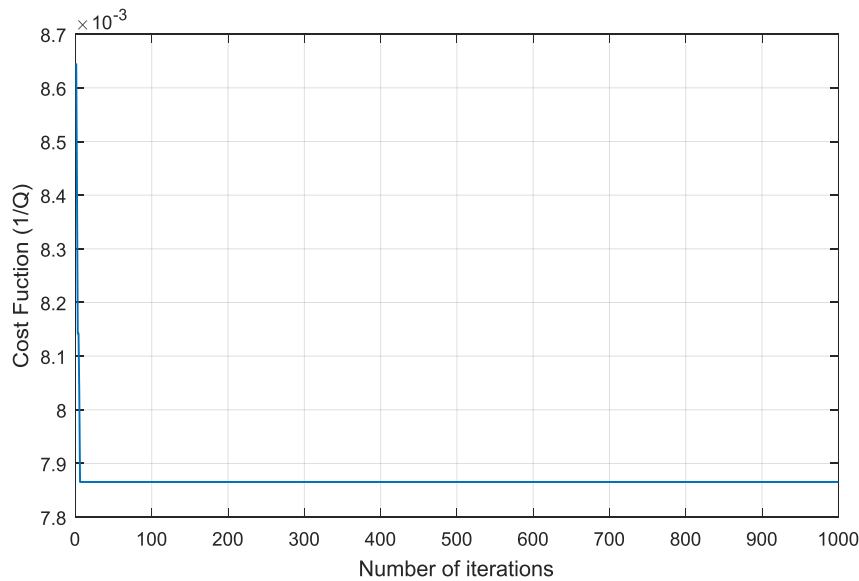


Figure 3. Cost Function Vs. Number of iterations

The optimization values obtained using ABC method are similar to those obtained using the evolutionary algorithm (GA) [5] with a slightly higher coefficient of quality factor.

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