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Compact Modeling of Single Event Latchup of integrated CMOS circuit

A. Al Youssef, L. Artola, S. Ducret, G. Hubert

Abstract - This paper presents a compact model of latchup taking into account design and process dependence. This model was used to confirm the SEL robustness of DFFs used in Readout Circuit of Infrared-sensors developed by Sofradir.

Index Terms— SEE prediction, TCAD simulation, SPICE simulation, Single Event Latchup, compact modeling, cross section, design, CMOS

I. INTRODUCTION

LATCHUP vulnerability in electronics devices used in spacecraft for space applications has become a real constraint since the 80's. For this, the development of SEL modeling was essential in order to study the Latchup sensitivity of CMOS gates and its evolution trend [1] [2].

The latchup phenomenon is due to an inherent parasitic structure in the CMOS technology. This structure can be modeled electrically as a parasitic thyristor. In the literature, two electric modeling approaches of the latchup phenomenon were developed. The first one is based on a set of diodes and connected resistors [2]. This approach models the PNP structure as PN / NP diode junctions and the resistors which represent specific silicon volumes. The other latchup modeling approach is based on a modeling of the PNP structure as thyristor structure [1]. This classical electric approach is the most known for modeling latchup at present. The electric model of the latchup phenomenon consists in two bipolar transistors (NPN and PNP) associated and a set of resistors representing the different silicon regions in the CMOS inverter structure. This method is based on the calculation of all the external resistors from the electrical equations according to four characteristic of the Latchup: the triggering point (V_{trig} , I_{trig}), and the holding point (V_{hold} , I_{hold}). It is therefore necessary to have this key latchup characteristics to be able to calculate these resistors. In this modeling approach [1], the two models of bipolar transistors are the conventional BJT models with assumptions of electrical characteristics of the parasitic bipolar transistor (such as the threshold voltage, order of about 0.7V. The main weak point of such approach is that no real modeling of the intrinsic behavior of parasitic transistors is performed, and there its behavior can not takes into account design and process parameters.

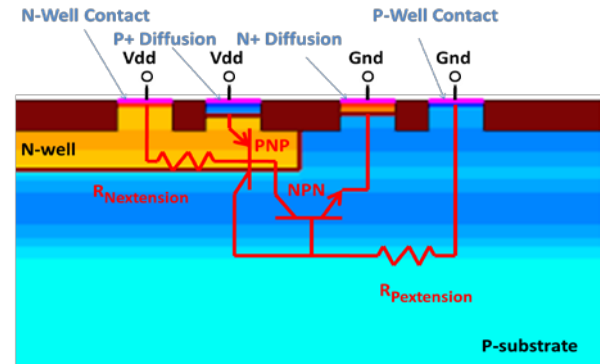
The goal of the paper is to present a new approach which proposes a more realistic compact model in order to be representative of latchup phenomenon. This approach also makes it possible to study the impact of the design and technological parameters on the Latchup sensitivity as it's not

the case in the classical approach [1]. This compact model was used to confirm the Single Event Latchup (SEL) robustness of DFFs used in Readout Integrated Circuit of Infrared Image sensors developed by Sofradir. The SEL prediction was obtained by the mean of the Monte Carlo SEE tool MUSCA SEP3 [3] and the Transient ERROR Injection Framework for Integrated CMOS (TERRIFIC) devices [4] applied to the new compact model of Latchup.

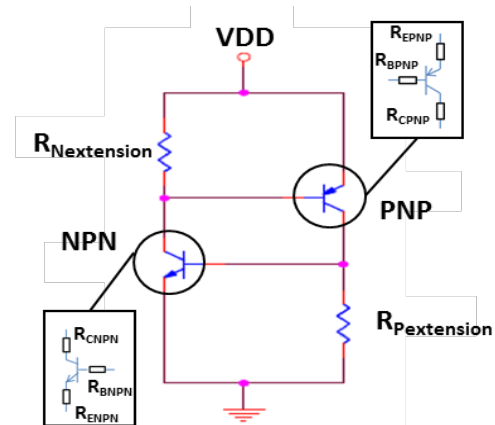
II. LATCHUP MODELING BY COMPACT ELECTRICAL MODEL

A. General presentation of the compact bipolar transistor modeling

The compact electric Latchup model was inspired from the same idea of classical electric model developed by Bruguier et al [1], but with a real modeling of bipolar transistors. First of all, in this modeling approach, it was necessary to redefine the signification and the role of the six resistors in the classical electric model. Fig. 1 illustrates the new compact model.



(a)



(b)

Fig. 1: (a) Compact electric model of Latchup on 2-D CMOS inverter structure, (b) Simple presentation of Compact electric model of Latchup

In this way, the classic resistors R_{EW} , R_{CS} and R_{BW} are respectively considered as the internal resistors of the PNP transistor: the emitter resistor R_{EPNP} , the collector resistor R_{CPNP} and base resistor R_{BNPN} . In the same way, the resistors R_{CW} , R_{ES} and R_{BS} are respectively considered as internal resistors of the NPN transistor: the collector resistor R_{CNPN} , the emitter resistor R_{ENPN} and the base resistor R_{BNPN} . R_{CNPN} and R_{BNPN} are interconnected in N-well region as shown in Fig. 1 (a). The silicon area in the N-well which represents the extension zone between the interconnected zone base-PNP/Collector-NPN and the TOP of N-well, is represented in this new modeling by the resistor $R_{Nextension}$ as shown in Fig. 1 (b). The sum of the resistors $R_{Nextension}$, R_{BNPN} and R_{CPNP} must be equal to the resistor of N-well R_{N-well} . The resistors R_{BNPN} and R_{CPNP} are interconnected in the P-well region as presented in Fig. 1. The silicon area in the P-well which represents the extension zone between the interconnected zone base-NPN/collector-PNP and the TOP of P-well, is represented in this new modeling by $R_{Pextension}$ as shown in Fig. 1 (b). The sum of the resistors $R_{Pextension}$, R_{BNPN} and R_{CPNP} must be equal to the resistor of the P-well R_{P-well} . Therefore, the compact Latchup electrical model shown in Fig. 1 (b) consists in two bipolar transistors and two equivalent resistors, $R_{Nextension}$ and $R_{Pextension}$, which represent the silicon volumes making the connection between the two bipolar transistors with the Top of the CMOS cell.

The first step was to develop the new compact modeling of bipolar transistors. This development was performed by the mean of TCAD and SPICE simulations. Then, the $R_{Nextension}$ and $R_{Pextension}$ resistors are involved to get the all elements of electrical Latchup modeling presented in Fig. 1.

B. Development of the compact bipolar transistor modeling

It should be noted that the TCAD simulations are considered as reference in this approach. The structure used in this study is a CMOS inverter designed by Sofradir, and defined in previous paper [5]. The behavior of the CMOS structure modeled by TCAD simulation was validated by the PDK (Process Design Kit) used by Sofradir as done in previous work [5]. The physical TCAD simulation models used hydrodynamic simulation approach [5].

First, each bipolar transistor is modeled by TCAD simulation in a distinct way as shown in Fig. 2. TCAD simulations were performed in order to get the reference electric characteristic of each bipolar transistor. However, in order to keep a relevant representativeness of the CMOS structure, only the implant of the complementary bipolar transistor was removed. This allows for getting a realistic modeling of a compact model dedicated to the Latchup parasitic structure. Each bipolar parasitic transistor was characterized with build only its inherent structure as presented in Fig. 2. (a) and Fig. 2 (b) for the NPN and PNP transistor respectively. For the NPN transistor, as mentioned, the P-diffusion implant was removed from the complete structure of inverter. In the same way, PNP transistor was characterized without the N-diffusion implant. The goal of this step was to find the I-V characteristics of each bipolar transistor separately.

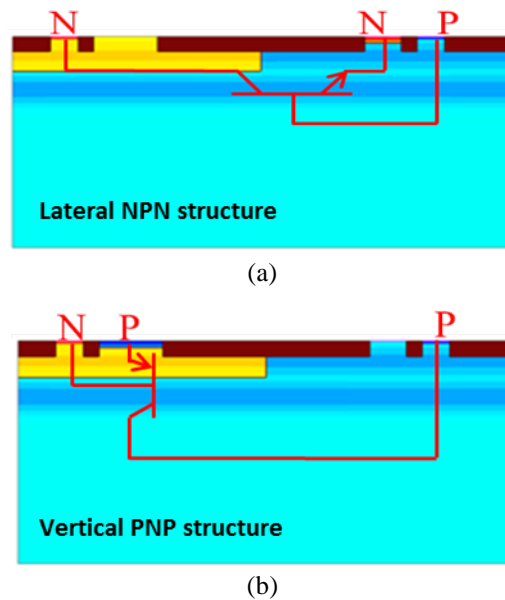


Fig. 2: Bipolar transistors built in TCAD simulation, (a) NPN transistor structure (b) PNP transistor structure.

The I-V characteristics were obtained at the nominal voltage of the CMOS inverter of the DFF cell, i.e., 5V. The I-V characteristics are presented in red in Fig. 3.

Before going to perform the SPICE simulations of bipolar transistors and get their electrical characteristics, it was necessary to find the values of the internal resistors of each pole of bipolar transistors by TCAD simulations.

In TCAD simulation, each pole of inherent bipolar transistors was modeled in 3D. For example, the N-well in Fig. 1 (a) is the base of PNP transistor and in same time the collector of NPN transistor. Ohm's law was applied at the nominal voltage (5V) on N-well block in order to determine its resistance. Each pole resistor of bipolar transistors was found in the same way.

The second step in bipolar transistors modeling was based on the development of model card of each bipolar transistor by SPICE simulation. At this level, the model card in SPICE simulation of each bipolar transistor was updated by using all the internal resistors issued from the previous TCAD simulation. On the other hand, the optimization in the threshold voltage region is obtained by the update of the saturation currents of the different junctions of the parasitic transistors based on TCAD simulation extractions. More details about card models parameters will be added in the final paper.

C. Validation of the compact bipolar transistor modeling

In order to validate the new compact model of bipolar transistor, a comparison was performed. Fig. 3 shows the I-V characteristics for NPN obtained by TCAD simulation (red dashed-line), by SPICE simulation of compact model card (blue line) and obtained by SPICE simulation of standard BJT model [6] (blue dashed-line). In order to perform a fair comparison, the standard (classic) BJT model card was calibrated in order to be representative the design specificities

of the CMOS inverter. The same approach was done for the PNP transistor. The details will be presented in the final paper.

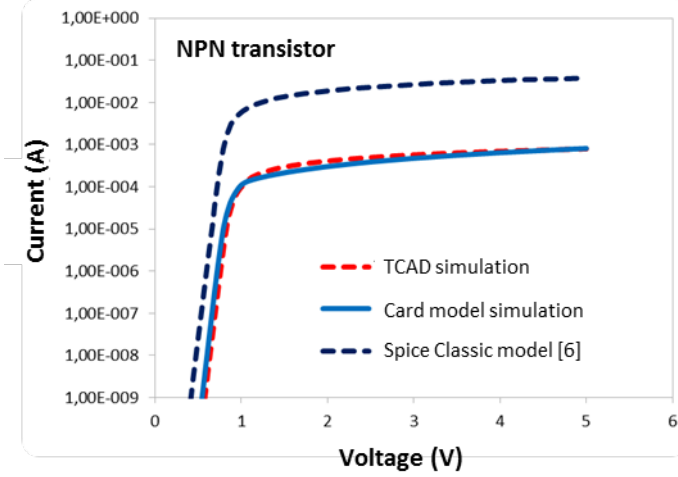


Fig. 3 :I/V characteristics of NPN bipolar transistor, TCAD curve is plotted in red dashed-line and two SPICE curves, curve dressed in blue line represent SPICE simulation with Card model developed and the curve plotted in blue dashed-line represent the classic card model

The comparison shows a very good correlation of the new compact model of bipolar transistor with the reference TCAD simulations. Moreover, the comparison with classic model (blue dashed line) highlights the improvement of the modeling and the interest of the presented work.

D. Validation of the Latchup modeling

The final step of this modeling approach was to build the complete compact electric Latchup model (Fig. 1) consisting in the two bipolar transistors (presented in II.B) and the two equivalent resistors $R_{N\text{extension}}$ and $R_{P\text{extension}}$ presented in section II.A. During this step, a specific work was carried out to determine the distribution of these resistors (equation 1 and equation 2) in order to obtain a good correlation between the Latchup characteristic modeled by the SPICE simulations and the Latchup characteristic obtained by the TCAD simulations.

$$R_{N\text{-well}} = R_{N\text{extension}} + R_{BNPN} + R_{CNPN} \quad (1)$$

$$R_{P\text{-well}} = R_{P\text{extension}} + R_{BNPN} + R_{CNPN} \quad (2)$$

Fig. 4 shows the latchup characteristic of each bipolar transistor obtained by TCAD simulation (red dashed-line), by SPICE simulation of the compact Latchup electrical model (blue line) and the classical modeling [6] (blue dashed line). As previously, in order to perform a fair comparison, the classic spice model (BJT and resistances) was calibrated in order to be representative the design specificities of the CMOS inverter.

The comparison shows that the compact Latchup model is in good agreement with the TCAD reference simulation as well in terms of latchup metrics (V_{trig} , I_{trig} , V_{hold} , I_{hold}) but also in term of shape. This comparison shows the pertinence of compact Latchup modeling. More details will be described in the final paper.

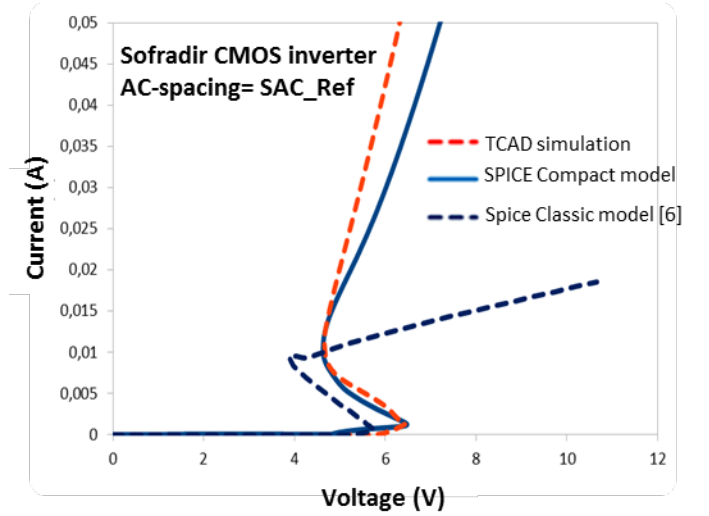
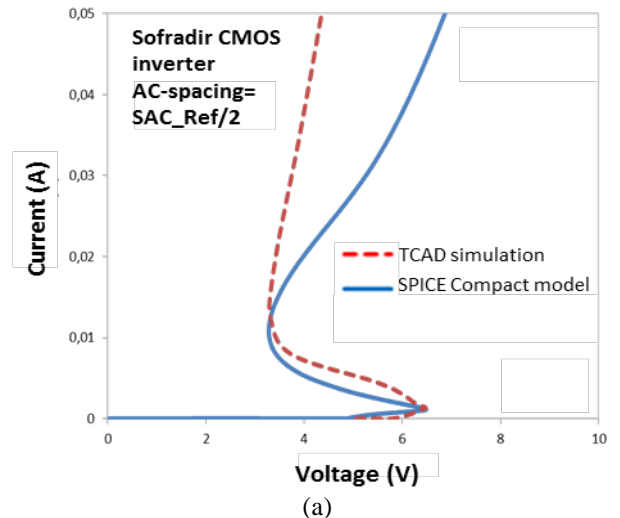


Fig. 4: Comparison of compact SPICE model, classical SPICE and TCAD simulation of Sofradir CMOS inverter reference structure.

An important point of the proposed work, is the capability of the compact latchup model to taken into account the effects of the design. An example is presented for the parameter AC-spacing (SAC). The SAC is the distance between n-MOS transistor and p-MOS transistor in CMOS inverter structure. The increase in the SAC is known to improve the robustness to SEL of CMOS cell [8]. From an electrical point of view, the reduction of SAC distance leads to a modification of the N and P-well resistors. These two resistors are characterized in the card model of one of the bipolar transistors PNP or NPN. For confidential reasons, the reference value of the SAC is not provided.

The comparison of I-V characteristics obtained by compact modeling and TCAD simulation is presented for two values of SAC: SAC/2 and SAC/5. The corresponding I-V characteristics are presented in Fig. 5 (a) and Fig. 5 (b). The two figures highlight the robustness of the compact modeling to take into account the effect of the SAC as well in to term of shape as and in terms of Latchup key characteristics (the trigger point and the hold point).



(a)

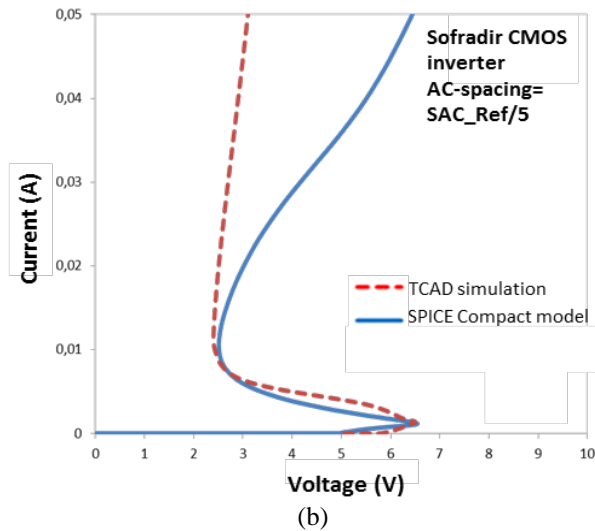


Fig. 5: Comparison of I-V characteristics from issue TCAD simulations (red dashed line) and latchup compact model (blue line) of the CMOS Inverter Structure with two values of SAC: (a) $SAC = SAC_{ref} / 2$ and (b) $SAC = SAC_{ref} / 5$. The CMOS inverter designs are issued from a DFF used in a ROIC developed by Sofradir

The next section presents an application of compact modeling in order to determine the single event latchup sensitivity under heavy ions with according to different design configurations of Sofradir CMOS inverter used in D-Flip-Flop of a ROIC developed by Sofradir for their Infrared Image Sensor, as described in [5].

III. SINGLE EVENT LATCHUP ESTIMATION OF DFF USED IN ROIC FROM SOFRADIR

In order to valorize this relevance of the compact modeling of Latchup, the Monte Carlo SEE prediction tool, MUSCA SEP3, was used to calculate the transient perturbation induced by heavy ion on the source of inverter of a DFF.

First, the SET databases induced by heavy ions were calculated by the MUSCA SEP3, for different LET values [6]. The complete description of the tool was presented in previous works [3]. More details will be presented in the final paper. Next, the injection of the SET in the compact latchup circuit was performed by the injection platform called TERRIFIC (Transient ERROR Injection Framework for Integrated CMOS) [4]. The automatic injection tool allows for interfacing MUSCA SEP3 and the circuit simulator. In this work SPECTRE was used to simulate the latchup compact model.

The cross-section trend shows an increase in the SEL sensitivity with a decrease in the SAC distance. No Latchup event was observed for the reference value of SAC of the CMOS (SAC_{ref}). This trend will be presented in final paper. This immunity is depicted by an arrow to the down. This trend confirms the observation already observed by TCAD simulations in this work and previous works [6].

In order to have a more general view, Fig. 6 shows the global SEL cross-section as a function of LET for the tree value of SAC (SAC_{ref} , $SAC / 2$ and $SAC/5$). As expected, the SEL cross-section increases as the LET increases. This is entirely

consistent with what exists in the literature [6] [5]. Compact modeling is used to improve the Latchup immunity of the reference structure of Sofradir. The reference structure of Sofradir (SAC_{ref}) was tested under heavy ion beam at 67 $MeV.cm^2.mg^{-1}$ at UCL in Belgium and it was demonstrated a Latchup immunity of Sofradir technology [7]. This confirms the relevance of the SEL modeling presented in this work.

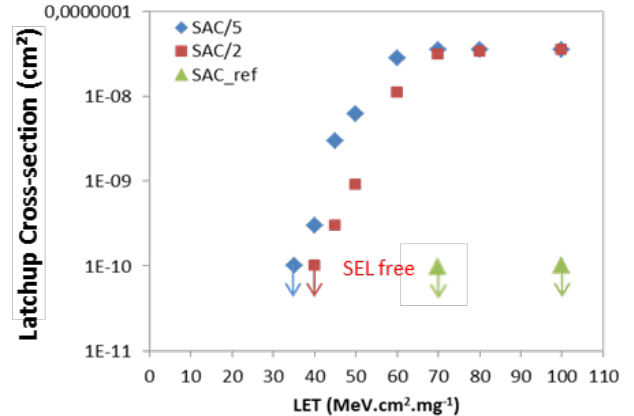


Fig. 6: The SEL cross-section of CMOS inverter for various SAC values: reference value (green triangles), $SAC / 2$ (red squares) and $SAC / 5$ (blue diamonds)

IV. CONCLUSIONS AND PERSPECTIVES

In this paper, a new compact modeling approach to the latchup phenomenon was presented. This compact modeling was validated at three levels: transistor level by PDK simulation, at compact level by electrical stress TCAD and at device level by heavy ion tests. This modeling approach has shown its effectiveness in representing Latchup key points, trigger point and Latchup hold point. The Latchup sensitivity study was performed with an application case of the Sofradir design and technology. Moreover, this work has shown in relevance to take into account the design effects on the SEL sensitivity. This point was presented for the AC-spacing parameter. The results confirmed the Latchup sensitivity trend in terms of SAC distance effect and the relevance of such a modeling approach to provide design optimization support to Sodrafir's ROIC development team. This method offers a more realistic modeling of the parasitic latchup structure induced by the CMOS technology. This approach is able to study the Latchup sensitivity for any technology and go up to the estimation of the SEL cross sections while considering the risk of the events non-destructive such as SET or SEU.

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