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# A new methodology for EMC prediction of integrated circuits after aging

C. Ghfiri, A. Boyer, A. Bensoussan, *Senior Member, IEEE*, A. Durier, S. Ben Dhia, *Member, IEEE*

**Abstract**—EMC of integrated circuits represents a major constraint for the qualification of electronic circuits. Today, there are existing standardized models such as ICEM-CE that allows the prediction of conducted emission generated by an IC at a PCB level. However, the EMC levels may change after a certain period of operation due to the aging of components. On the other hand, no existing model or tool can predict the long-term EMC levels. This paper presents a new methodology for modeling of integrated circuits in order to construct an EMC model which takes into account the aging based on a new reliability model called M-STORM.

**Index Terms**— Integrated circuits, modeling, reliability, aging, ICEM-CE standard, FPGA.

## I. INTRODUCTION

WITH the development of the nanoscale integrated circuits (ICs) and their strong integration in the different embedded application areas, the EMC constraints become more and more important. Simulation becomes mandatory to predict the EMC levels of electrical and electronic systems, from component to equipment level. The International Electrotechnical Commission (IEC) has proposed several standards to model and predict EMC performances of ICs, such as the ICEM-CE model for modeling the conducted emission (CE) level published in the IEC 62433-2 [1]. The approach followed is a black box approach that does not require knowledge of the internal structure of the circuit.

On the other hand, deep submicron circuits in embedded systems working in harsh environment are weakened by intrinsic physical degradations and may impair the functional safety. Some characteristics of MOS transistors such as mobility, threshold voltage, saturation current [2], transconductance [3], and the leakage currents in the substrate

or oxide capacity are drifted due to aging [4], which degrade the overall performance of ICs. In fact, the EMC performances of an IC depend closely on the electrical and physical parameters of the circuit. Thus the aging of electronic devices can contribute to a significant variation of EMC before a complete wearout of the applications, as demonstrated by some recent studies. For example, in [5], the aging of filtering passive devices led to an increase of conducted and radiated emission produced by a switch-mode power supply. CMOS IC aging induces also a drift of the electromagnetic emission, as demonstrated by experiments in [6] and simulation [7]. Aging may also impair susceptibility of ICs such as digital circuits [8], I/O buffers, phase-locked loop [9], voltage regulator [10] or operational amplifiers [11].

These aging-induced drifts lead to a new consideration in EMC called long-term EMC [12]. Its purposes are multifold: evaluating the drifts of EMC levels of an electronic equipment or circuit during its lifetime in a given environment, estimating the risk of non-compliance to EMC limits, determining adequate margins to ensure EMC compliance during the lifetime.

The applied procedures for the long-term EMC characterization are based on temperature stresses based on HTOL (High Temperature Operating Life test) and LTOL (Low Temperature Operating Life test), which are standard accelerated aging tests that simulate the aging behavior of internal structures of electronic components. The accelerated aging tests consists in applying high or low temperature (e.g. 150°C or -40°C) on circuit for a certain time duration to activate intrinsic degradation mechanisms. However these tests only allow the assessment of EMC drifts after aging in a given stress condition and long-term EMC prediction in other conditions cannot be estimated without a reliability model.

To study the reliability of ICs, there are existing standard models for the prediction of the lifetime of ICs dedicated to the different industrial applications. The most traditional standards for reliability modeling are the MIL-HDBK-217F [13] and FIDES [14], but they have been proposed considering only one dominant constant failure rate mechanism and do not take into account multiple simultaneous stresses applied and the possible combination of several degradation mechanisms. Hence, the need of new multi-stress reliability models for advanced ICs has been felt and recent researches are dealing with their development, such as Multi-physSics mulTi-stressOrs predictive Reliability Model (M-STORM) [15]. The

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prediction of the long-term EMC levels must link such advanced reliability model to an EMC model. This should be performed following a specific accelerated aging test strategy in order to precisely identify the aging parameters and perform the tests in a reduced time to fulfill industrial requirements.

This paper presents a new methodology to predict long-term EMC drifts in harsh environment for any operating conditions. It combines both EMC and multi-stress reliability models (resp. ICEM-CE and M-STORM). The reliability model is extracted from the Multiple Temperature Operational Life (MTOL) method, used to characterize efficiently IC failure rate in different combinations of stress conditions. In this study, only high temperature, current and voltage stresses are considered and the prediction is focused on CE of a digital IC. A brief state-of-the-art about prediction of IC reliability is provided in Section II. The M-STORM model is described in Section III. After the presentation of the case study in Section IV, the methodology used to extract the reliability model is explained in Section V. Finally, the construction of the long-term EMC model of the tested IC is presented in Section VI with prediction results of CE level evolution.

## II. RELIABILITY OF INTEGRATED CIRCUITS

### A. Overview on the reliability of ICs

The reliability is the ability of an item to perform a required function under stated operation and maintenance for a specified period of time. From an operational point of view, the reliability of an electronic component is described with a “bathtub curve” which represents the three stages of evolution of the failure rate  $\lambda(t)$  in time for an electronic system or component.

During their lifetime, CMOS devices are affected by specific degradation mechanisms that lead to the random wearout of electronic devices. The intrinsic mechanisms are due to internal causes of the IC, inherent to the design, the biasing conditions and the used materials. The four main degradation mechanisms activated in CMOS devices are: Electromigration (EM), Time Dependent Dielectric Breakdown (TDDB), Hot Carrier Injection (HCI) and Negative Bias Temperature Instabilities (NBTI). Their activation depends on the environmental conditions as the temperature and the power supply voltage and the current density. All these degradation mechanisms are described in numerous publications and standards, such as JEDEC JEP122H [16].

### B. Reliability standards

On the basis of the Constant Failure Rate (CFR) model, the military handbook known as MIL-HDBK-217 standard has been developed [13] and became the reliability prediction reference for industry but now abandoned by the DoD. Several updates of the military standard have been published until 1995; that results on MIL-HDBK-217F version. Since then, the standard has not been updated but is still widely used by military industry. In 2004, a consortium of eight French

aeronautical and military industries has developed a new guide for reliability prediction named FIDES [14]. It allows a realistic assessment of the electronic equipment reliability, including electronic systems operating in harsh environments (defense, aeronautic, industrial electronics, transport...) also based on return of experience (RETEX). However, it requires confidential data such as information on the manufacturing process which are generally not available.

Furthermore, these reliability prediction approaches are based on separating the stress parameters. They consider a single stress at a time and a single preponderant failure mode and mechanism at a time. This is due to the fact that the present guidelines are supposed to accelerate only one mechanism at a time. New approaches should be studied to take into account the eventual combination between the different degradation mechanisms. Hence, a special focus will be given on multiple stress testing methods in the next section with the presentation of a new model M-STORM (Multi-phySics mulTi-stressOrs predictive Reliability Model), whose construction is based on the Multiple Temperature Operational Life (MTOL) method [17].

## III. PRESENTATION OF M-STORM MODEL FOR RELIABILITY PREDICTION

The main principle of MTOL method is to identify the operating degradation mechanisms in an electronic circuit and to consider each failure mode as a sub-element. In [17], standard HTOL tests generally reveal multiple failure mechanisms during testing, which would suggest also that no single failure mechanism would dominate the failure rate in the field. Therefore, a preferable approximation is that all failures are linearly proportional, equally likely and the resulting overall failure distribution resembles constant failure rate process. This is consistent with the approach proposed by [13] and is still applicable for other type of stresses (humidity, vibration...). As stated in [24], multiple failure mechanisms may occur in a single set of time-to-failure data but without obvious points of inflection to help separate the mechanisms. This limitation has been recognized in the latest JEDEC standard [16]: when multiple failure mechanisms and thus multiple acceleration factors are involved, then the sum-of-the-failure rates method is required.

In order to solve the theoretical combination of the different laws modeling the degradation mechanisms, a matrix-based approach [19] has been studied and allows linking the different acceleration factors of each degradation mechanism to the corresponding Mean Time To Failure (MTTF) which is given by equation (1) with  $\lambda$  the failure rate. Electronic devices should be considered as comprising several failure mechanisms that degrade simultaneously [16]. As stated in [18], each mechanism ‘competes’ with the others to cause an eventual failure. When more than one mechanism exists in a system, then the relative acceleration of each one must be defined and averaged at the applied condition. Every potential failure mechanism should be identified and its unique

acceleration factor should then be calculated at a given stress condition (e.g. temperature and voltage) so that its failure rate  $\lambda_i$  can be approximated separately from the other mechanisms. Then, as is described by (2), the final failure rate  $\lambda$  of a circuit is the sum of the failure rates  $\lambda_i$  associated to degradation mechanisms which are supposed independent. In this work, these failure rates are computed according to the physics-of-failure models defined in [17] and weighted by constant terms related only to the technology.

$$MTTF = \frac{1}{\lambda} \quad (1)$$

$$\lambda = \sum_{i=1}^4 \lambda_i \quad (2)$$

Whereas each intrinsic mechanism is known to have different statistical distributions, the combination of distributions becomes, at the ensemble level, approximately constant rate as well known by Drenick [25]. This theorem justifies the summation of failure rate approach suggested here, also as explained in [16].

The MTOL method is based on the linear system presented in (3) which relates the failure rates of the main degradation mechanisms to the stress conditions and technology-dependent constants [26]. The matrix-based approach begins by assuming that each component is composed of multiple failure mechanisms based on its operation, rather than simply a sum of sub-components. EM, HCI, NBTI and TDDB are each seen as sub-components of the complete chip. Each mechanism is supposed to have its own acceleration factor related to voltage, temperature, frequency, cycles, etc. Each sub-component is assumed to approximate the relative likelihood of each mechanism as a proportion of the system failure rate. Then, each component can be seen as a summation of intrinsic degradation by individual failure mechanisms multiplied by its relative proportion.

Each row of (3) describes the linear equation given for an over-voltage, current and over-temperature stress conditions ( $V_i, I_i, T_i$ ), where  $i$  denotes the applied stress ( $i \in [1;4]$  for the four main degradation mechanisms in CMOS devices). The matrix  $\lambda$  is the failure rate expressed in Failure In Time (FIT). It requires the definition of a failure or degradation criterion by the experimenter. For example, in [20], it was computed according to a degradation criterion which defined as the drift of the propagation delays of a digital IC. Matrix  $AF$  contains the acceleration factors ( $A_i, B_i, C_i, D_i$ ) associated to the degradation mechanisms, which are computed according to models given in [16]. As the FPGA is a CMOS circuit, only the four main degradation mechanisms: EM, TDDB, NBTI and HCI are considered. They describe the overall effect of a specific accelerated stress condition compared to that at a reference stress. The reliability matrix  $P_i$  refers to the proportionality constants which characterize the impact of one degradation mechanism to the overall reliability of the circuit. These parameters are supposed independent of the applied stress conditions and the functions implemented on the circuit.

They dependent only on the technology of the circuit.

$$\begin{bmatrix} A_1 & B_1 & C_1 & D_1 \\ A_2 & B_2 & C_2 & D_2 \\ A_3 & B_3 & C_3 & D_3 \\ A_4 & B_4 & C_4 & D_4 \end{bmatrix} \cdot \begin{bmatrix} W \\ X \\ Y \\ Z \end{bmatrix} = \begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \\ \lambda_4 \end{bmatrix} \quad (3)$$

$$[AF][P] = [\lambda] \rightarrow [P] = [AF]^{-1} \cdot [\lambda] \quad (4)$$

The construction of the reliability matrix is based on the obtained results with the M-HTOL (Multiple High Temperature Over-stress Life) accelerating test under different conditions in order to activate the four main degradation mechanisms mentioned in II-A. That's why at least four stress conditions are needed to evaluate the contribution of each degradation mechanism. Each stress will see a strong contribution of one mechanism relative to the others, which describes a well-defined failure point location based on the physic-of-failure model (e.g. those defined in [16]).

The process of construction of the MTOL model is based on a calibration phase that allows the extraction of the constants  $P_i$  according to the tested operating conditions with the computed parameters ( $\lambda$  and  $AF$ ), as shown in (4). This linear matrix is solved by multiplying  $AF^{-1}$  with  $\lambda$  at each condition. The solution will give the coefficients  $W$  to  $Z$  which make up the relative contribution of each failure mechanism on the system. Once the reliability matrix is constructed for specific stress conditions, it is possible to extrapolate the model using the proportionality constants according to (3) and to obtain the MTTF to reach a degradation criterion for untested operating conditions according to (1).

The goal of solving the reliability matrix is the reliability prediction for any other operating conditions (e.g. nominal operating conditions) that were not tested using the interpolation and extrapolation of the constructed reliability model. The BAZ (Boltzmann-Arrhenius-Zhurkov) model [19] has been combined to MTOL model and led to the creation of M-STORM which is a multi-dimensional tool that can be used in a concrete situation of Deep Submicron (DSM) technologies. BAZ model is a mathematical generalized model [16] that assumes that one or more external stress acts as a catalyst for the reaction and decreases the activation energy required to switch from an initial nominal operating state to a final state of failure.

The new reliability prediction methodology was developed and validated on DSM commercial components designed in 28 and 45 nm technologies [20]. We can assume that for the same CMOS technology embedded in two different components, the degradation mechanisms activated by a multi-stress of voltage and temperature will be similar. Hence, the constructed reliability model using M-STORM model will be considered in this study in order to predict the IC reliability for untested operating conditions and integrate the degradation criterion in the EMC model.

#### IV. PRESENTATION OF THE CASE STUDIES

##### A. The circuit under test

The circuit under test is a XC6SLX16-FT256 Spartan 6 Xilinx FPGA, manufactured in CMOS 45-nm process. M-STORM model was developed for this technology previously [20]. The circuit includes 9152 configurable logic blocks (CLB) and up to 186 user I/Os. It is mounted in a Fine pitch Thin Ball Grid Array 256 balls (FTBGA256). The internal structure of this component is complex. It comprises six different power supply domains summarized in Table I for the core structure of the FPGA (VCCINT), the different IO standards and the JTAG chain (VCCO<sub>x</sub>).

As the study concern the construction of a long-term predictive ICEM-CE model, a specific test board has been designed for EMC measurement. It consists of a six layer board with complete power and ground planes compliant to the IEC61967-1 standard. A 1 Ω probe, as defined by the IEC61967-4 standard [21] has been placed between the ground pins of the FPGA and the ground reference of the test board in order to measure the return current flowing outside the circuit. The FPGA is mounted on a RF socket in order to test several samples. Moreover, a burn-in test board was developed in order to configure and over-stress several FPGAs simultaneously. The circuits are mounted on a burn-in socket.

##### B. Configurations

The experiments are defined according to a twofold objective: measure the failure rate of the FPGA and monitor the drift of CE level. As explained in Section III, the failure rate depends on a degradation criterion which must be defined prior to accelerated aging tests. In this study, we expected a reduction of the CE level due to the increases of propagation delays of FPGA CLBs. Thus, the CLB propagation delay increase is selected as degradation criterion. It will be expressed as a maximum relative increase compared to the initial propagation delay measured before aging. If the propagation delay measured after a period of stress exceeds the degradation criterion, the FPGA under test is considered as failed. The stress time to reach this level of degradation is the Time To Failure (TTF).

Several configurations were implemented in order to assess the evolution of the following parameters:

- The propagation delay through the different CLBs using a ring oscillator configuration. The ring oscillator consists of the configuration of  $(2N+1)$  inverters in chain. The output frequency is  $f_{out} = \frac{1}{2.N.T_p}$  where  $T_p$  is the propagation delay per inverter and includes the interconnections propagation delays whose drift will be considered as our degradation criterion. 99 inverters are implemented in order to fix the output frequency to around 10 MHz. Furthermore, the same design has been implemented in different areas at the FPGA floorplan level in order to consider each area as a single sample which allows increasing the number of aged components for the statistical analysis.

- Conducted emissions measurements are performed using the 1 Ω method [21] for the delay line configuration, in order to study the effect of aging on the CE level. In this case, the configuration is set for 10 inverters per block, and 900 delay lines will be implemented in series to maximize the dynamic power consumption.

#### V. METHODOLOGY OF ACCELERATED AGING TEST

The accelerated aging test must be performed for different stress conditions and several parameters are measured in order to assess the impact of the aging on EMC performance. The process of accelerated aging tests needs long time of stress and several measurements for different samples, which is not adapted to industrial applications that aim to reduce the qualification tests duration. Hence, in order to optimize the accelerated aging test protocol, a new methodology has been established. An increased step-stress is applied to define the voltage limits of the circuit at the same time as Multiple High Temperature Operating Life Test (M-HTOL) to combine the voltage and temperature stresses.

##### A. Step-stress Accelerated Life Test (SSALT)

Since the manufacturer does not give exactly the voltage values that lead to the components burn-out, the DC voltage maximum ratings values are not precise enough to determine the voltages to be applied to the FPGA in each step of the step-stress. Therefore, prior to the SSALT, a preliminary study has been performed on three FPGA samples and consists of over voltage stress tests to determine the voltage burn-out limit. The test consists of applying the nominal voltages on the FPGA, then increasing the voltage on each power domain until obtaining a burn-out. Table I presents a comparison between the nominal operating voltages  $V_{nom}$ , the maximum rating  $V_{max\_rating}$  given by the manufacturer datasheet and the maximum voltages  $V_{max}$  that lead to the components burn-out that were obtained during the applied preliminary study. It should be noted that the measured voltage burn-out limit were repeatable between the three tested samples.

After the definition of the voltage values for burn-out limit for each power domain, the step-stress is used to define the voltage values where the component drifts according to a degradation criterion. In this study, the degradation criterion is the drift of propagation delay of FPGA CLB, deduced through the measurement of the output frequency of a ring oscillator structure. During this stage it is necessary to control the ambient temperature (for example 20 °C.) that should not change during the step-stress experience.

TABLE I. COMPARISON BETWEEN THE NOMINAL VOLTAGE AND THE MAX RATING AND BURN-OUT LIMIT VOLTGES

Power Domain	$V_{nom}$	$V_{max\_rating}$	$V_{max}$
VCCINT	1,2	1,32	4,7
VCCO <sub>0,1,2</sub>	3,3	5,75	6,7
VCCO <sub>3</sub>	1,5	1,65	6,7

The diagram presented in Fig. 1 shows the step-stress workflow, which consists of initial measurements for a set of specified configuration to follow up the FPGA degradation according to a predefined degradation criterion. Then an initial over voltage stress  $V+\Delta V$  is applied to supply the tested FPGAs (where  $V$  is the nominal voltage and  $\Delta V$  is the incremental stress voltage) for a duration of 168 h. Here, the step-stress duration and the incremental stress voltage are fixed to be constant, however, in a step-stress test, it is possible to have different stress periods and the stress levels do not have to be uniformly spaced. At the end of each step recovery measurements are performed under the FPGA nominal operating conditions. Hence, if there is no degradation on the tested configuration the over voltage stress  $\Delta V$  must be incremented. Otherwise, the voltage limit will be set at the operating conditions of the step  $N-1$ . No voltage stress will be applied beyond this limit during the life test. The voltages defined at the  $N-1$  step will be noted  $V_{STEP}$ .

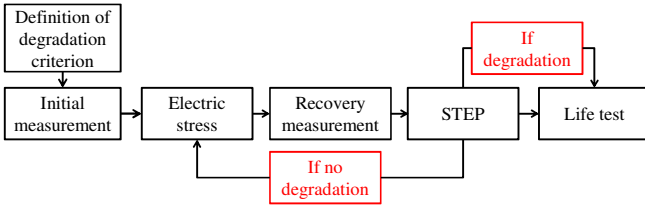


Fig. 1. Workflow of the step-stress accelerated life test

### B. Multiple High Temperature Operating Life Test

The M-HTOL testing method is based on the voltage over-stress combined to the temperature over-stress. For the studied FPGA, the evolution of the current consumption according to the voltage and the temperature is not known. However, the activation of the degradations mechanisms are linked to the device current density which leads to an increase of the junction temperature. Hence, prior to the life test, a preliminary study must be performed to understand the link between the three parameters: current, voltage and temperature. The preliminary test involves the selection of different temperatures, and different core supply voltages ( $VCCINT$ ) and IO power supplies ( $VCCO$ ), in order to establish a design of experiment that will define the life test operating conditions ( $V, T$ ). In this preliminary study, the static and dynamic currents are measured to estimate the junction temperature for each voltage and current consumption and ambient temperature combination.

The preliminary study leads to the construction of a linear function between the applied ambient temperature and voltage to compute the junction temperature  $T_j$  as given by (5), in order to select the stress conditions with respect to the burn out limit, the value thermal resistance  $R_{th}$  ( $30.2 \text{ }^\circ\text{C/W}$  as specified by the manufacturer).

$$T_j = T_a + R_{th} \cdot (VCCINT \cdot ICCINT + VCCO \cdot ICCO) \quad (5)$$

The objective is to choose the stress conditions (i.e. couple

( $V, T$ )) such as significant degradation of the FPGA under test may be measured in a reasonable stress duration, in order to limit the total duration of the test and its cost. In this study, the maximum stress duration was limited to 1000 hours, which is similar to the maximum test duration defined by industrial standards. Using the step-stress and the preliminary test results, three operating conditions have been defined to ensure that the degradation criterion may be reached in less than 1000 hours. Normally, four stress conditions should be defined to extract the reliability matrix  $P$  according to (4) since CMOS ICs are affected by four main degradation mechanisms, as explained in Section III. However, as shown in [20], TDDDB is insignificant in this CMOS 45-nm technology. Its influence is neglected in this study so the number of stress conditions can be limited to three.

Hence, at the end of the life test, the reliability parameters can be computed and compared to M-STORM model for its validation. The life test workflow is presented in Fig. 2 and consists of initial measurements at ambient temperature to define the initial characteristics of the tested FPGAs. Then, the stress application at the defined parameters ( $V_i, T_i$ ) over a time  $t_j$ , where  $i$  is the stress number and  $t_j$  is the duration of stress in hours. According to the MIL-STD-883H standard, the duration  $t_j$  varies following the TTF for the specified stress conditions. Recovery measurements in the nominal operating conditions are performed to follow the drift of the tested configurations. If the components do not show important degradations, a new stress is performed for a duration  $t_{j+1}$ . Otherwise, the end of the life test occurs for ( $V_i, T_i$ ).

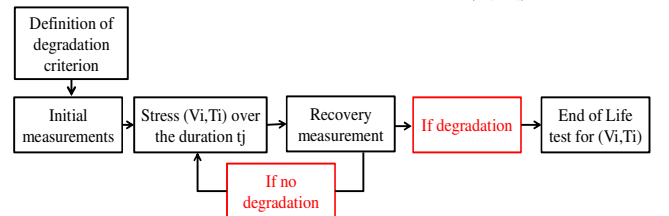


Fig. 2. Workflow of M-HTOL test method

### C. Presentation of the experimental results of accelerated aging test

Five FPGAs have been stressed under three different stress conditions presented in Table II which were set considering the SSALT and the preliminary study to the M-HTOL test in order to respect the operating conditions limits of the FPGA and not reach the burn-out limit.

TABLE II. SELECTED STRESS CONDITIONS FOR THE M-HTOL TEST

Stress N°	VCCINT (V)	VCCO (V)	$T_j$ ( $^\circ\text{C}$ )
1	2,3	4,1	115
2	2,3	4,8	135
3	2,8	5,2	115

On the other hand, as presented in Fig. 3, the aging leads to the increase of the propagation delays in the different tested FPGAs. Hence, the switching frequency becomes slower.

According to the applied stress conditions, the variation of ROs output frequencies will have a different level. When the degradation is plotted according to the square root of the stress time, the trend is linear whatever the stress condition. Thus, the time required to reach a certain level of degradation can be extrapolated.

The aging affects the FPGA timing performances and make it less reliable. In the next paragraphs, FPGA will be considered as faulty when the variation of the RO frequency, and thus the CLB propagation delay, exceeds a given percent of the initial frequency. The degradation criterion will be noted "X % drift", where X will be the maximum increase allowed by the degradation criterion.

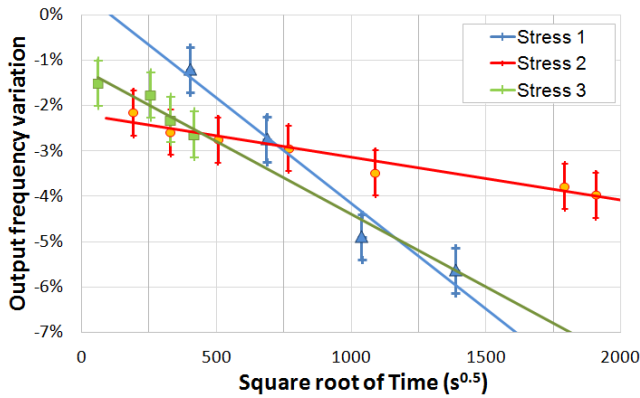


Fig. 3. Evolution of the output frequency of the ring oscillator for each stress condition

Moreover, the measurements of CE using the  $1 \Omega$  probe have shown that the level of the voltage fluctuations decreases after aging as seen in Fig. 4. This reduction is due to the degradation of the internal transistors of the CLB which modifies the transient current produced by the FPGA activity. In frequency domain, the reduction of the conducted emission spectrum is more pronounced below 300 MHz, where the noise produced by CLB dominates. At higher frequencies, the conducted emission is mainly due to the clock input buffer, which was not degraded during the M-HTOL test.

#### D. Construction of M-STORM model

From the measurement of drift of its intrinsic parameters, a reliability model of the studied FPGA can be built according to a specified degradation criterion (e.g. data path delay). The reliability models based on Weibull's distribution will be used to calculate the failure rate for each stress condition and compared to those provided by the M-STORM model. Weibull's distribution for the statistical analysis of the failure mode allows modeling the three life stages of semiconductor components (infant mortality, useful life, wearout). Its probability density function is given by (6), where  $\alpha$  is referred as the characteristic *TTF* and  $\beta$  is Weibull slope or shape parameter. Failure rate in each life stage can be expressed by different values of the Weibull parameter  $\beta$ . Both parameters can be extracted experimentally from the plot of the cumulative distribution function of the measured failures

according to the time [22]. That's why this distribution is widely used in the analysis of the reliability of electronic circuits and systems.

$$f(t) = \left(\frac{\beta}{\alpha}\right) \left(\frac{t}{\alpha}\right)^{\beta-1} e^{-\left(\frac{t}{\alpha}\right)^{\beta}} \quad (6)$$

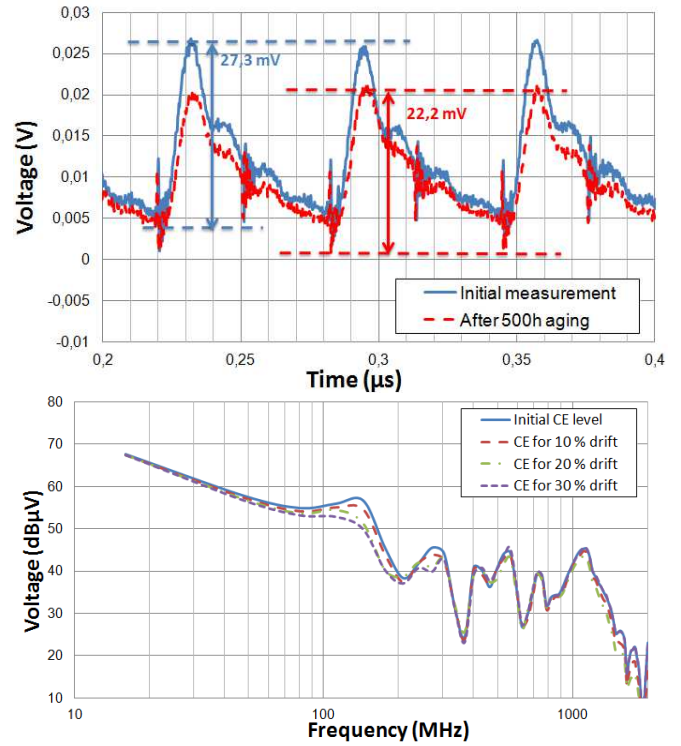


Fig. 4. Conducted emission measurements using the  $1 \Omega$  probe before and after aging: in time (up) and frequency domains (bottom)

For the calculated MTTF with Weibull's distribution, the numbers of FIT have been computed. Furthermore, the different stress conditions for the core power supply VCCINT and the junction temperature  $T_j$  are included in the M-STORM model in order to predict the FIT. Fig. 5 presents the Arrhenius plot experimentally measured and modelled by J. Bernstein et al. [20] on the FPGA 45 nm technology. It relates the logarithm of the mean time-to-failure MTTF (x-axis) to a temperature scale (y-axis) which is linear in the inverse of absolute junction temperature,  $1/T_j$  but is marked with the corresponding Celsius scale on the right hand side. The degradation criterion to determine the plotted MTTF is a drift of 20% on RO's frequency. The dashed lines represent the 90% confidence limits interval calculated for each stress voltage condition. The slope of a portion of curve is proportional to the activation energy of a related failure mechanism. The three failure mechanisms (HCI, NBTI and EM) are observed simultaneously but depend on stress conditions. It is easy to see the slopes of the curves for certain range of temperature as they are not constant but depend on stress conditions: at low temperature the slope is negative



hence the activation represents the HCI failure mechanism, since it is accelerated in low temperature condition. At medium temperature and above a certain limit, the slope becomes positive and is related to NBTI failure mechanism while at high temperature the electromigration is activated with another slope. Thus the M-STORM model has demonstrated the activation energy of a DSM 45 nm technology depends on stress conditions applied and is not constant at all. The actual experiments (red and blue dots) show the MTTF associated to the same degradation criterion (20% frequency drift) under some condition of stress (as mentioned in the caption) and are well positioned within the 90% confidence level close to the predictive model. It demonstrates the main failure mechanism activated under our condition of stress is clearly the NBTI. Even if the number of measurement points is not sufficient to prove the validity of M-STORM definitively, the correlation between models built by two different teams from two different experimental setups provides a good confidence on the relevance of M-STORM results.

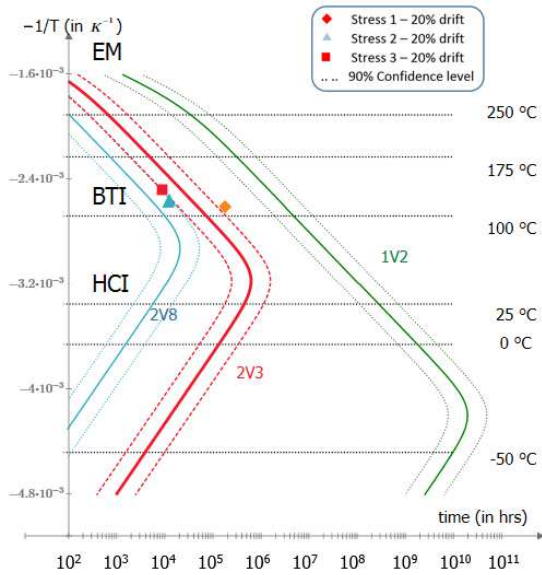


Fig. 5. Arrhenius plot (based on constant failure rate Weibull’s distribution). Red and blue points are our experiments for the three stress conditions compared to the M-STORM model [20]

### VI. CONSTRUCTION OF AN ICEM-CE MODEL TAKING INTO ACCOUNT THE AGING

The construction of the ICEM-CE model of the studied FPGA is detailed in a previous work [23]. It consists of the estimation of the dynamic power consumption using the power estimation tools provided by the FPGA manufacturer. The objective of this work is the introduction of the drift induced by the aging in the ICEM-CE model in order to predict the long-term CE level of the FPGA.

In order to study the parameter influencing the internal activity of the FPGA, the obtained data from the ring oscillator measurements are considered for the variability of the propagation delay using the equation (7), where  $d$  is our

degradation criterion i.e. the drift percentage on the propagation delays after aging. The output frequency of the ring oscillator is inversely proportional to the propagation delay  $\tau$  between the different logic blocks of the FPGA. Furthermore, the maximum current amplitude  $I_{max}$  due to the switching activity of the FPGA is inversely proportional to the propagation delay (8). Thus, the current peak-to-peak amplitude will decrease with the aging and it can be expected that the external voltage measured across the  $1 \Omega$  probe will also decrease with aging.

$$\tau_{stress} = \tau_{initial} + d \cdot \tau_{initial} \tag{7}$$

$$I_{max} = \frac{2P_{dyn\_avg}}{f_{clk} V_{DD} \tau} \tag{8}$$

TABLE III. COMPARISON BETWEEN THE M-STORM DATA AND THE COMPUTED RELIABILITY PARAMETERS FOR THE IA CONSTRUCTION

Delay line Configuration	Estimated Dynamic Power (mW)		Data path delay (ns)		IA amplitude (mA)
	Logic	Clock	Logic	Clock	
Before Aging	40	4	8	0,7	521
After 500h aging	40	4	8,44	0,7385	484

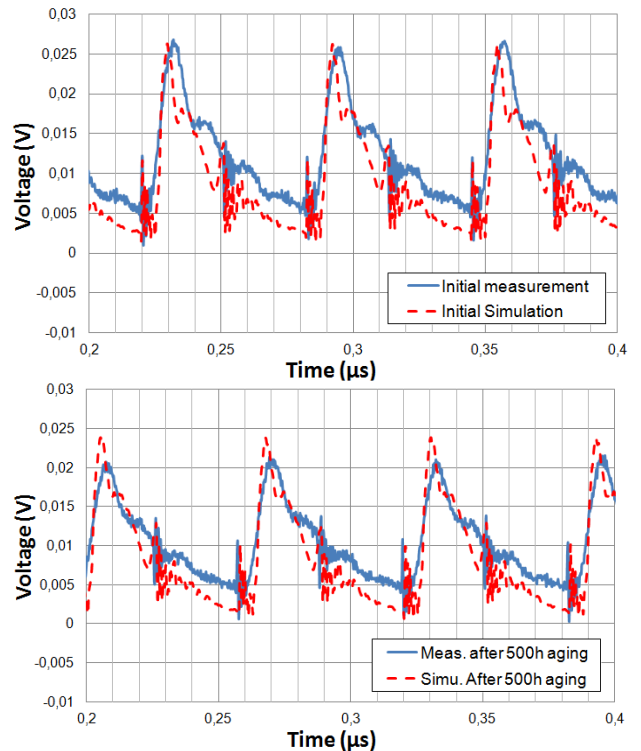


Fig. 6. Comparison between the measured and simulated CE in the time domain before (up) and after aging (down)

The comparison between the measured and simulated conducted emission using the  $1 \Omega$  probe is performed for the initial measurement and after 500 h under the stress condition 2 as presented in Fig. 6. The simulated CE before aging shows



a good prediction of the peak-to-peak amplitude (27.3 mV) in the time domain. After aging, the simulated CE amplitude (23.4 mV) slightly overestimates the measured peak-to-peak amplitude (21.8 mV), but overall, the constructed ICEM-CE model after aging provides a good prediction of the CE level drift in the time domain.

The comparison between the measurement and simulation of CE level before and after aging in the frequency domain has shown that at the initial state (before aging), the simulated envelope can predict the general trend of the CE with a calculated average RMS error around 6.79 dB. After aging, the simulated envelope of CE in the frequency domain provides a good prediction of the measured with a calculated average RMS error is 6.21 dB. Fig. 7 presents the variation of the measured and simulated CE spectrum at 144 MHz, where the variation is more significant and for other frequencies (208 MHz, 304 MHz), before and after 500 h aging at stress condition 2. Although the simulation underestimates the variation of the CE degradation level but it is able to predict the trend up to 2 %.

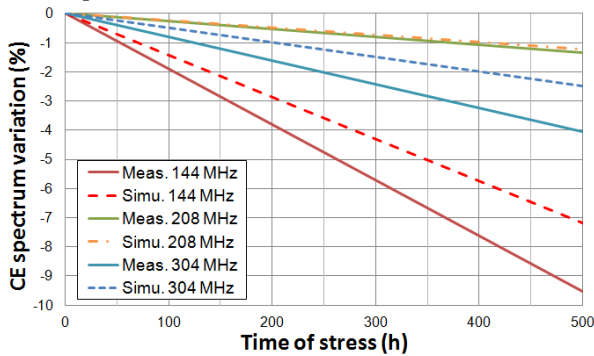


Fig. 7. Comparison between the variation of the measured and simulated CE spectrum from the initial state and after 500 h aging

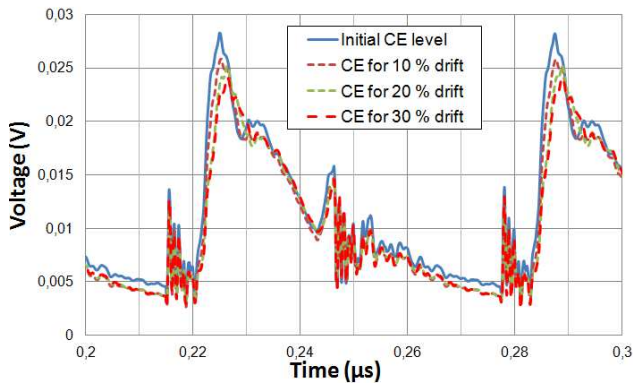


Fig. 8. CE level prediction for different drift criterion on propagation delays in the time domain

In order to evaluate the simulated trend of CE for the different drifts studied in the previous section, CE simulation were performed for increased propagation delays  $\tau_{stress}$  up to 10 %, 20 and 30 % from the initial value  $\tau_{initial}$  and the maximum amplitude of the current sources are constructed according to each propagation delay evolution. Fig. 8 presents the prediction of CE in the time domain for each drift. The

figure shows the decrease of the peak-to-peak amplitude of the external voltage simulated using the 1  $\Omega$  probe when the drift percentage increases.

Fig. 9 shows the predicted TTF for each CE degradation in the time and frequency domains. In the time domain the variation is calculated for the simulated CE peak-to-peak amplitude. In the frequency domain, the variation is calculated for the simulated CE at 144 MHz where the CE evolution is more significant. The M-STORM tool allows the prediction of the TTF for any degradation criterion at any operating conditions. In nominal operating conditions, the electromagnetic emission level of the FPGA remains rather stable with time since about 500 millions hours, i.e. nearly 60000 years, are required to expect a reduction of 15 % of the peak-to-peak amplitude of the CE. Our prediction methodology proves that there is no risk of long-term emission issues with this component.

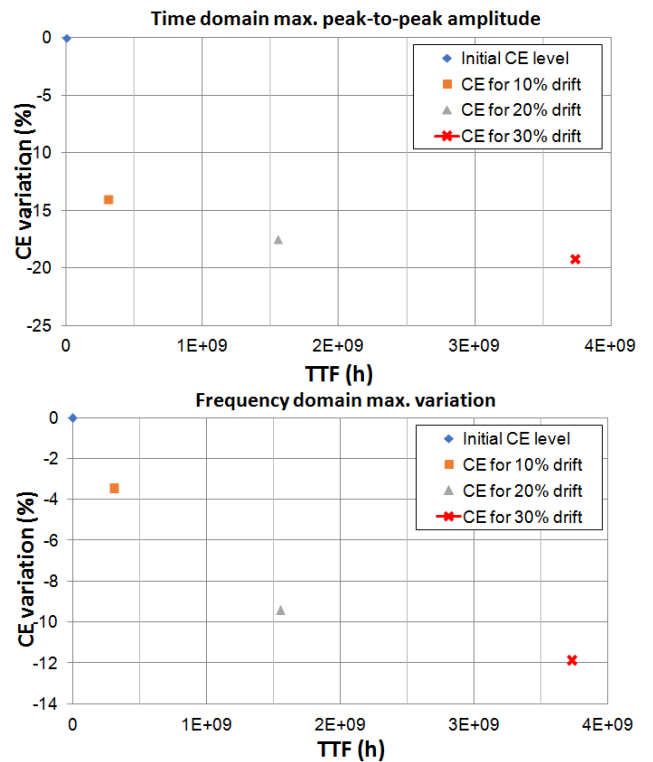


Fig. 9. TTF prediction for CE variation for different degradation criteria at nominal operating conditions in the time domain (up) and frequency domain (down)

## VII. CONCLUSION

In this paper, the aging effect induced in a multi-stress environment (high temperature and overvoltage) on conducted emission level of the FPGA was studied using a combination of a predictive reliability model (M-STORM) and a predictive EMC of IC model (ICEM-CE). The test experiments have demonstrated a good correlation with the M-STORM model for the 45 nm technology. The Arrhenius plot and MTTF assessments versus stress conditions were deduced using

Weibull's distribution and have confirmed the prediction capability of the M-STORM model. The comparison has shown that the computed parameters are located in the 90 % confidence level of M-STORM model.

The ICEM-CE model was modified in order to reproduce the CE of the FPGA after aging. The methodology is based on the integration of the drift in the pulse duration of the IA Core. This variation on the measured drift of the propagation delays of programmable logic blocks is extracted from the prediction made by M-STORM model. This methodology was confirmed by comparison between CE simulation and measurements. Using the proposed methodology, the evolution CE level can be predicted by ICEM-CE model for any stress conditions handled by M-STORM model. Moreover, the corresponding TTF is also determined.

The proposed model that combines M-STORM and ICEM-CE models integrates the statistical distribution for a user defined degree of confidence level which allows the prediction of the risk of EMC non-compliance using the confidence interval. The prediction of the long-term EMC level of integrated circuits allows the evaluation the risk of non-conformity at the nominal operating conditions, and evaluating the relevance of EMC margins. Moreover, it can be useful to set the adequate EMC troubleshooting devices, e.g. the shielding size or the filtering devices.

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