# A generic method of pulse width modulation applied to 3-Level T-type NPC inverter

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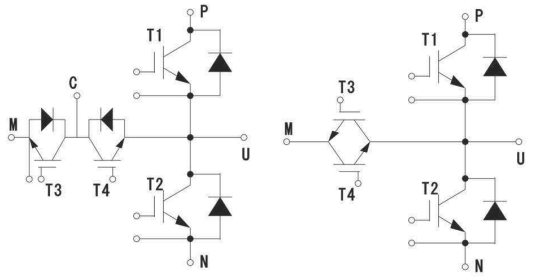
***Abstract*—This paper illustrates the application of a method based on the resolution of linear systems to an uncommon inverter switching cell. This study describes the mathematical model of the modulated inverter leg associated at the considered structure. The generalized inverse of a matrix is used to generate the admissible conduction rates. Among the modulation strategies obtained, three specific modulation schemes are proposed and discussed thanks to the generic mathematical standpoint used.**

## I. Introduction

Electrified systems are of growing importance in many applications developed today. Among them, some widespread common applications such as, pipeline pumps [1], fans [2], water pumping stations [3], traction applications [4] concern medium voltage converters. New trends for converter design, emerging from eco-friendly applications are nowadays studied such as grid integration of renewable-energy sources [5], reactive-power compensation [6] in order to maximize the system efficiency and so on. It is noted that these applications need a control over the exchanged energy. Consequently, the converter architecture mainly concerns inverter topology.

Emergence of wide band gap semi-conductors combined with new limits for usual silicone devices leads to new interest for developing original inverter topologies. Indeed, studies work on the correlation of a given architecture and its dedicated modulation strategy with an application. Among these studies, the multi-levels architecture and particularly those using the Neutral Point Clamped were widely studied. Firstly dedicated to high power application, a spin-off topology, named three level T-type converter - $3LT^2C$, is under interest. Effectively, this topology benefits of its ability at being used in high power photovoltaic systems [7], as well as variable speed drives for low voltages applications, [8]. Moreover, it has been demonstrated that a $3LT^2C$ increases the converter efficiency compared to similar multilevel inverters, with respect to power losses, and more precisely compared to a 3-levels Neutral Point Clamped -NPC- topology, [9], [13].

Studies demonstrated that the modulation strategy of a 3-level NPC can also be applied to this topology. Indeed, usual carrier based Pulse Width Modulation - PWM associated with 2 carriers waveforms [10], or Space Vector Modulation - SVM which allows harmonic selection [11], have been successfully tested. Nevertheless, the major drawbacks of such inverter topology concern the control of the common mode voltage or the unbalance voltage of DC input sources. Most of the modulation strategies aim at solving these topology drawbacks.




(a) (b)

Fig. 1. T-type switching cells [14]. (a) Normal, (b) RB-IGBT based.

It appears to our knowledge that it does not exist any generic modulation model of $3LT^2C$ converter. The aim of the study is to adapt the modeling technique proposed in [12] in order to establish a generic inverter modulation model of such structure, that can match the following criteria:

- to be applied to carrier based PWM;
- to be extended to SVM principles;
- to highlight how to implement a generic modulation scheme;
- to define modulation admissible solutions.

The first part of the paper is devoted to describe the considered structure and proposes a mathematical model. The second part deals with determination of control strategies by using a generic mathematical method. Finally, among the whole solution set, 3 specific modulation strategies are highlighted and discussed.

## II. T-type switching cell

From a practical point of view, a $3LT^2C$ inverter is made of three legs based on a common switching cell structure. The switching cell can be built from 2 ideas, as illustrated in Fig. 1. This figure depicts electrical equivalent circuits of available commercial modules. As far as the modulation model is concerned, the switching cell can be considered as three elementary ideal switches, associated to two independent and perfect input voltage sources as illustrated in Fig. 2.

The inverter cell considered is made of three switches, named $K_1$, $K_2$, $K_3$ respectively. As this cell is an elementary switching cell, only one switch can be turned on at once.

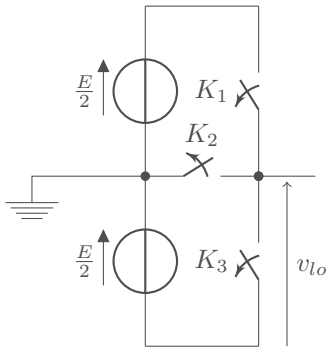



Fig. 2. Elementary cell structure.

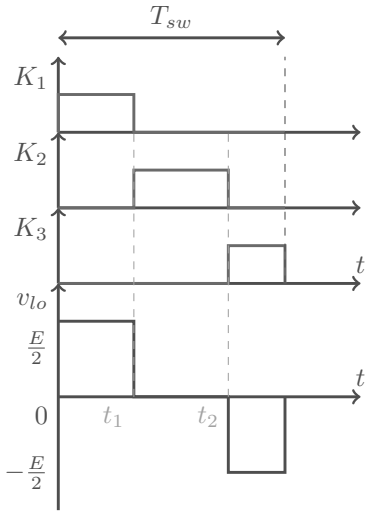



Fig. 3. Example of a switching sequence.

Moreover, due to the switches connection, there is no short-circuit of the input voltage sources. Each switch is able to apply a given voltage to the output line $v_{lo}$ as given in Table I. The other possibilities are not allowed.

TABLE I
OUTPUT VOLTAGES.

| $K_1$ | $K_2$ | $K_3$ | $v_{lo}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | $E$ |
| 0 | 1 | 0 | $\frac{E}{2}$ |
| 0 | 0 | 1 | 0 |

Fig. 3 gives an example of a switching sequence and the corresponding line voltage during $T_{sw}$. For notational comfortness, the switching frequency $f_{sw} = \dfrac{1}{T_{sw}}$ is used in the following of the paper.

As examplified in Fig. 3, $t_1$ is the time when $K_1$ is closed. Then $K_2$ is switched on from $t_1$ to $t_2$, and finally $K_3$ between $t_2$ and $T_{sw}$. Let us define, $\tau_i$, $i \in \{1;2;3\}$ as the conduction rates of switch $K_i$ over $T_{sw}$:

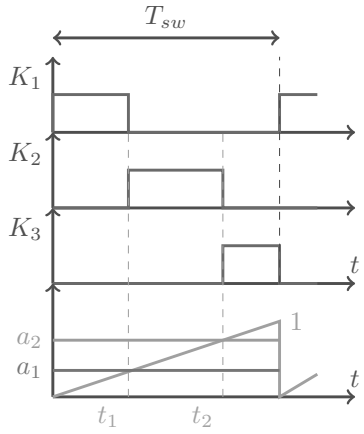



Fig. 4. Command orders generation principle.

$$\begin{aligned} \tau_1 &= \frac{t_1}{T_{sw}} \\ \tau_2 &= \frac{t_2 - t_1}{T_{sw}} \\ \tau_3 &= \frac{T_{sw} - t_2}{T_{sw}} \,. \end{aligned} \tag{1}$$

Let us denote $a_1$ and $a_2$ as

$$\begin{cases} a_1 = \tau_1 \\ a_2 = \tau_1 + \tau_2 \,. \end{cases} \tag{2}$$

The switching time $t_1$ and $t_2$ are used for command orders generation. They are then obtained comparing $a_1$ and $a_2$ to a sawtooth signal defined between 0 and 1 at frequency $f_{sw}$ as illustrated in Fig. 4. It is noted that the command order for $K_3$, is obtained thanks to $T_{sw} - t_2$. It is obvious that these values of $c_i$ are deduced from Tab. I. Consequently, this modulation scheme ensures only one or zero switching, of a given switch within $T_{sw}$.

Such elements lead to the expression of the mean value of the line voltage over the switching period, noted $V_{lo}$, as

$$< v_{lo} >_{T_{sw}} = V_{lo} = \frac{E}{2}\left(-a_1 - a_2\right) + \frac{E}{2} \,. \tag{3}$$

Defining $V_{lo}^* = V_{lo} - \frac{E}{2}$ leads to the relationship

$$V_{lo}^* = -\frac{E}{2} A a \tag{4}$$

where $A = \begin{bmatrix} 1 & 1 \end{bmatrix}$ and $a = \begin{bmatrix} a_1 & a_2 \end{bmatrix}^T$. Immediately, an advantage of such a model appears: a carrier based modulation scheme is used, associated with a single carrier easily generated. The control strategy vector $a$ appears as the solution of the linear system described in (4).

## III. Control strategies

### A. Generic solutions

$\text{rank}(A) = \text{rank}\,[A\, V_{lo}]$ thus, the system model (4) is consistent. Due to the fact that $\text{rank}(A) = 1$, while the number of columns of $A$ is $n = 2$, it exists an infinity of solutions for $a$. Consequently, some degrees of freedom will be highlighted. It will be demonstrated in the following section how to accurately determine these degrees of freedom. Let us denote $V^*_{ref}$ the voltage which should be obtained when measuring $V_{lo} - \frac{E}{2}$. The set of solutions to modulate the reference voltage $V^*_{ref}$ is thus defined using the generalized inverse theory [15]. Among the possible generalized inverse of $A$, the pseudo-inverse, denoted $A^\dagger$, will be used. It is unique and because $A$ is full row rank matrix [15], a simple expression for $A^\dagger$ can be computed:

$$A^\dagger = \left(AA^T\right)^{-1} A^T = \frac{1}{2}\begin{bmatrix}1\\1\end{bmatrix}. \tag{5}$$

Thus the solution of (4) can be written

$$a = -\frac{2}{E}A^\dagger V^*_{ref} + \left(I - A^\dagger A\right) z \tag{6}$$

where $z$ is an arbitrary 2-dimensional vector. Then, the solutions can be split in two parts summed up as:

- a fixed solution: $-\frac{2}{E}A^\dagger V^*_{ref}$, which can be written $a_{ref}\begin{bmatrix}1 & 1\end{bmatrix}^T$ with $a_{ref} = -\frac{1}{E}V^*_{ref}$;
- a free solution $\left(I - A^\dagger A\right) z$.

Looking at the free solution, it appears that some degrees of freedom are revealed from $\left(I - A^\dagger A\right) z$. The number of degrees of freedom $n_\lambda$ is

$$n_\lambda = dim(Ker(A)) = n - \text{rank}(A) = 1\,. \tag{7}$$

To express the degree of freedom $\lambda$, the goal is to define a $(n \times n_\lambda)$ sized matrix $M$ such as, it exists a $N$ matrix as $MN = I - A^\dagger A$ and $Nz = \lambda$. This factorization is not unique. Nevertheless, the maximal rank factorization eases the degree of freedom exhibition such as

$$\left(I - A^\dagger A\right) z = \begin{bmatrix}1 & -1\\ -1 & 1\end{bmatrix} z = \begin{bmatrix}-1\\1\end{bmatrix}\begin{bmatrix}-1 & 1\end{bmatrix} z = \begin{bmatrix}-1\\1\end{bmatrix}\lambda\,. \tag{8}$$

Finally, the final control vector is obtained as

$$a = a_{ref}\begin{bmatrix}1\\1\end{bmatrix} + \lambda\begin{bmatrix}-1\\1\end{bmatrix}. \tag{9}$$

### B. Implementation constraints

Among the solution set expressed in (9), some solutions are constrained from the system considered. Indeed, components of $a$ have to be in $[0, 1]$, and, they are to be ordered. Finally, three main relationships are taken into account:

- $0 \le a_i \le 1$, applied to $a_1$ and $a_2$ respectively in order to check the linearity functioning zone of the inverter. Consequently, it is obvious that over-modulation is not concerned by this modelling method;
- $a_2 \ge a_1$ because $t_2 - t_1 \ge 0$ to avoid short-circuit of the upper voltage source. This ensures the feasibility of the switching sequence illustrated in Fig. 4.

All the physical constraints can be summarized with

$$0 \le a_1 \le a_2 \le 1. \tag{10}$$

Therefore, the first step in order to set the degree of freedom of the system, aims at guaranteeing the practical conditions compatibility for implementation. To do so, lower and higher margins for the degree of freedom $\lambda$, respectively $\lambda_{low}$ and $\lambda_{high}$, are defined such as

$$\lambda_{low} \le \lambda \le \lambda_{high}\,. \tag{11}$$

Taking into account the constraint $a_2 \le 1$ allows to define a limit

$$\begin{aligned} & a_2 = a_{ref} + \lambda \le 1 \\ \Leftrightarrow\quad & \lambda \le 1 - a_{ref}\,. \end{aligned} \tag{12}$$

In a similar manner, another limit for $\lambda$ is expressed and computed from the constraint $0 \le a_1$:

$$\begin{aligned} & a_1 = a_{ref} - \lambda \ge 0 \\ \Leftrightarrow\quad & \lambda \le a_{ref}\,. \end{aligned} \tag{13}$$

The third constraint leads to

$$\lambda \ge 0. \tag{14}$$

Finally, the boundaries for $\lambda$ given in (11) are set, thanks to (12) (13) and (14) so that:

$$\begin{aligned} \lambda_{low} &= 0 \\ \lambda_{high} &= \min\left(a_{ref}, 1 - a_{ref}\right)\,. \end{aligned} \tag{15}$$

As a first consequence, the maximal (resp. minimal) $V_{lo}$ is $\frac{E}{2}$ (resp. $-\frac{E}{2}$). Thus, the maximal fundamental magnitude of a modulated sinusoidal waveform of such a structure, is $\frac{E}{2}$. To conclude, all positive $\lambda$ chosen between the margins expressed in (15) satisfies (10). Thus, Eq. (15) guaranties the linearity of the modulation function.

However, $\lambda$ still has to be defined among this interval. Fig. 5 depicts the fixed solution $a_{ref}$ and the margins $\lambda_{low}$ and $\lambda_{high}$. The domain in which $\lambda$ satisfies the system constraints is highlighted. The magnitude of the reference voltage is here set first at $\frac{E}{3}$ (from $t = 0$ to 50 ms) and then at $\frac{E}{2}$ (from $t = 50$ to 100 ms). When the magnitude of the reference voltage equals $\frac{E}{2}$, at some points, the only $\lambda$ satisfying the system constraint is $\lambda = 0$.

### C. Setting specific solutions

In this study three $\lambda$ are considered:

1) $\lambda = \lambda_{low} = 0$ defines $t_1 = t_2$, leading to a classical switching cell by not using $K_2$;
2) $\lambda = \lambda_{high}$ fixes $t_1 = 0$ or $t_2 = T_{sw}$, leading to a reduction of the switching losses ($K_1$ or $K_3$ is not used) while getting $\frac{E}{2}$ edges on $V_{lo}$;
3) $\lambda = \frac{\lambda_{low} + \lambda_{high}}{2}$ leading to the maximization of the time between the switching ($\lambda$ is as far from $\lambda_{low}$ and from $\lambda_{high}$).

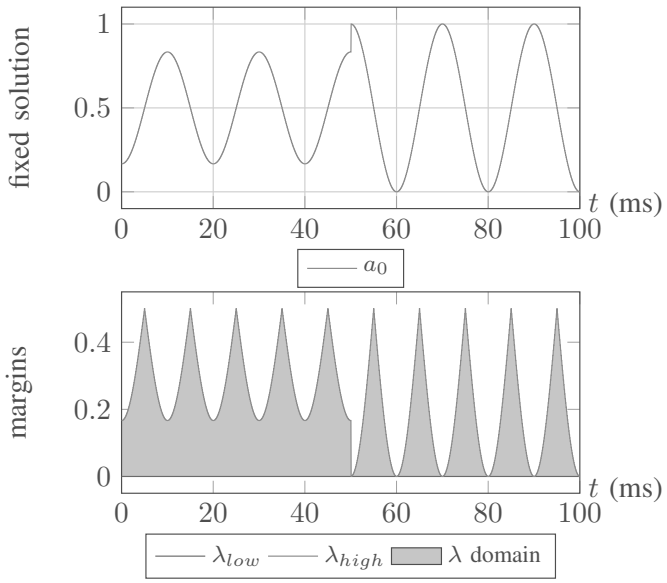



Fig. 5. Fixed solution and margins for the degree of freedom $\lambda$.

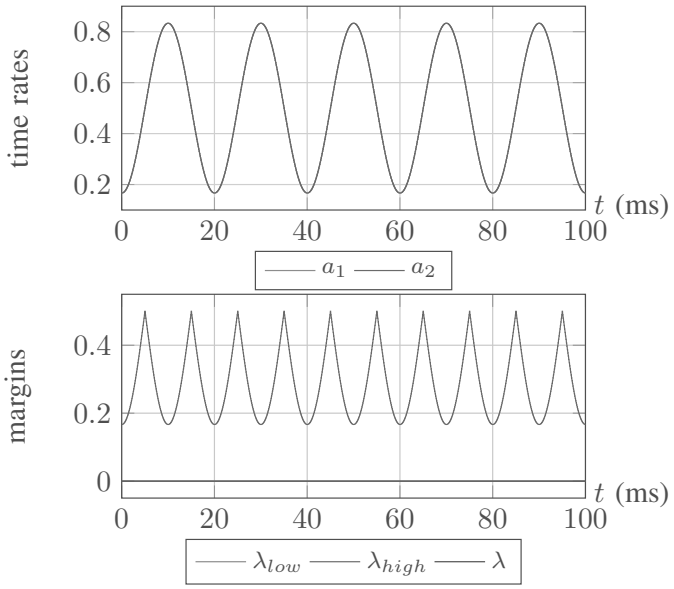



Fig. 6. $\lambda = 0$, time rates and margins

## IV. Simulation

A Scilab [16] testbench based on the switching cell given in Fig. 2 has been developed to test the three strategies proposed. The cell is connected to a $E = 100\,\text{V}$ DC bus. The switching frequency is set at $f_{sw} = 10\,\text{kHz}$. The three modulation strategies have been tested by modulating a $50\,\text{Hz}$ $50\,\text{V}$ peak sinusoidal waveform.

The proposed strategies are able to generate a signal which fundamental correspond to the desired reference voltage.

### A. $\lambda = \lambda_{low} = 0$

This strategy introduces no shift between $a_1$ and $a_2$ (Fig. 6). Consequently, the switch $K_2$ is not used - $K_2$ is off - and the switching cell is working as a usual two-levels/two-switches cell (Fig. 7). They are plotted for half a period of the sinusoidal waveform. On the one hand, $K_2$ never switches which reduces the switching losses by reducing the number of switching at each switching period. On the other hand, this strategy increases the harmonic distortion of the switched current, due to the lower number of switching. Moreover, the high magnitude of the switching edges, $\Delta v_{lo} = E$ seems to be an important factor - and also a drawback - concerning resonance phenomenons as well as overall quality of currents induced.

### B. $\lambda = \lambda_{high}$

Choosing $\lambda = \lambda_{high}$ introduces a difference between $a_1$ and $a_2$ as illustrated in Fig. 8. The three switches are thus used as displayed in Fig. 9. However, this figure points out that $K_2$ is switched all along the period of $V_{ref}$, while $K_1$ and $K_3$ are used on half a period only. Such a strategy leads to clamp alternatively the time rates to 0 for $a_1$, and 1 to $a_2$. Indeed, $K_1$ and $K_3$ are only used during the lower, respectively higher, part of $V_{ref}$. Similarly as the previous strategy, it can be guaranteed some low switching losses, and high harmonic distortion also. Let us notice that this strategy does not suffer from the same drawback as the resonance sensitivity is concerned. Indeed, the voltage edge is smaller: $\Delta v_{lo} = \dfrac{E}{2}$.

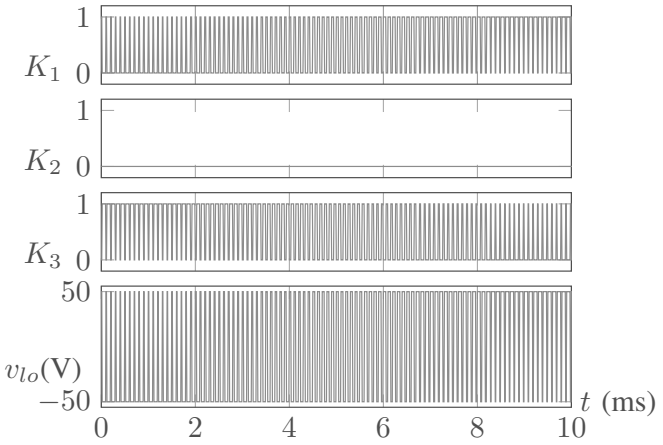



Fig. 7. $\lambda = 0$ switches sequence and output voltage

### C. $\lambda = \frac{\mu_{low}+\mu_{high}}{2}$

This strategy involves all the switches of the cell at each switching period. It implies no saturation of $a_1$ at 0 or $a_2$ at 1 for more than one switching period, as shown in Fig. 10. Thus, compared to previous strategies already described, it leads to an increase of the switching losses: three switching occur at each switching period (Fig. 9). A first advantage is to obtain a low distortion signal. Moreover, due to the mitigated voltage edge encountered, $\Delta v_{lo} = \dfrac{E}{2}$ and $v_{lo} = E$, the influence of connection parasitic elements on resonant phenomenons is limited as displayed in Fig. 12. This figure, highlights that

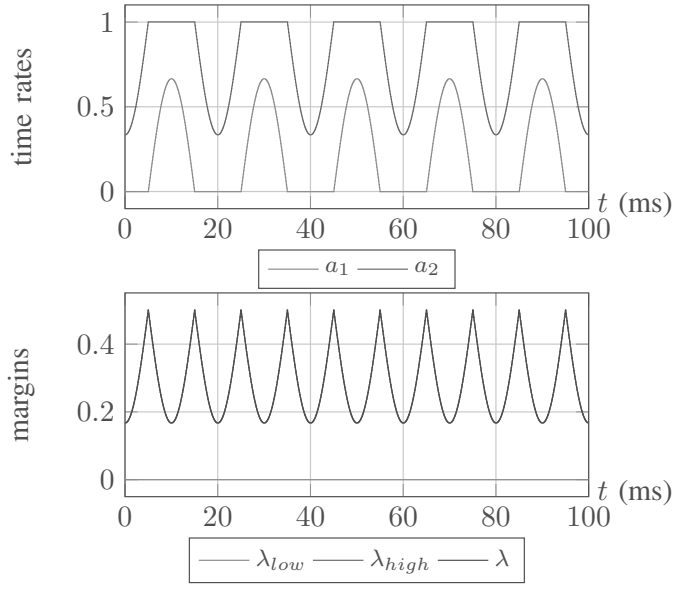



Fig. 8. $\lambda = \mu high$

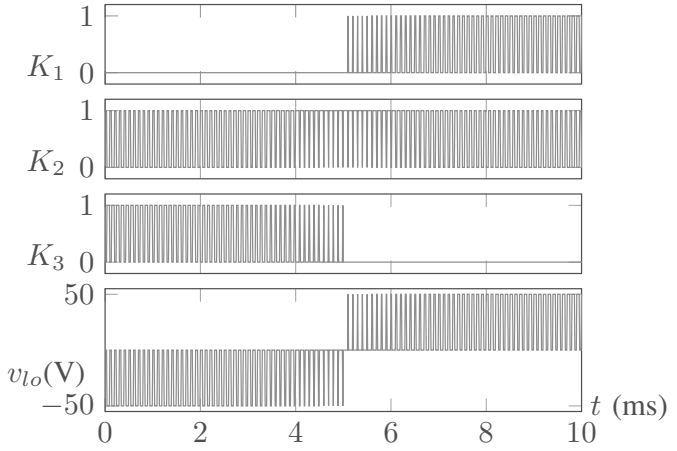



Fig. 9. $\lambda = \frac{\mu_{low}+\mu_{high}}{2}$ switches sequence and output voltage

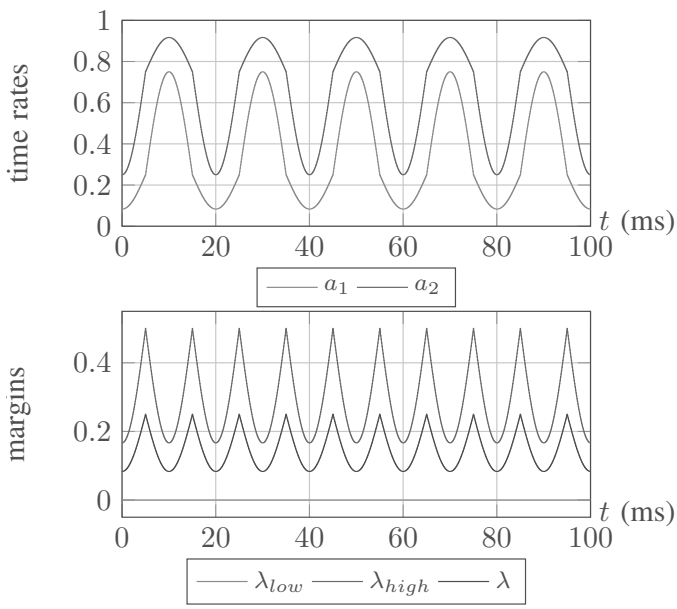



Fig. 10. $\lambda = \frac{\mu_{low}+\mu_{high}}{2}$

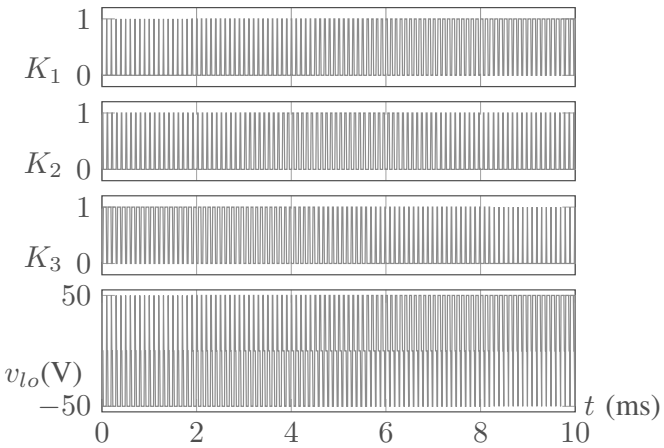



Fig. 11. $\lambda = \frac{\mu_{low}+\mu_{high}}{2}$ switches sequence and output voltage

modelling scheme given in Fig. 4 is fulfilled. Let us remark that the rising edges can be split by using a triangle carrier. Consequently, it will produce only $\Delta v_{lo} = \frac{E}{2}$ voltage edges. Moreover, every carrier waveforms is suitable to the proposed modulation scheme.

## V. Conclusion

This paper illustrates the application of a method based on the generalized inverse to solve linear systems. It is applied to a $3LT^2C$ inverter switching cell. In a first step, the study describes the mathematical model of the modulated inverter leg. The modulation scheme revealed, is based on a carrier based PWM scheme. Then a pseudo-inverse is used to generate the admissible solution set. Among the solution set obtained, 3 specific solutions are discussed. They are compared from the

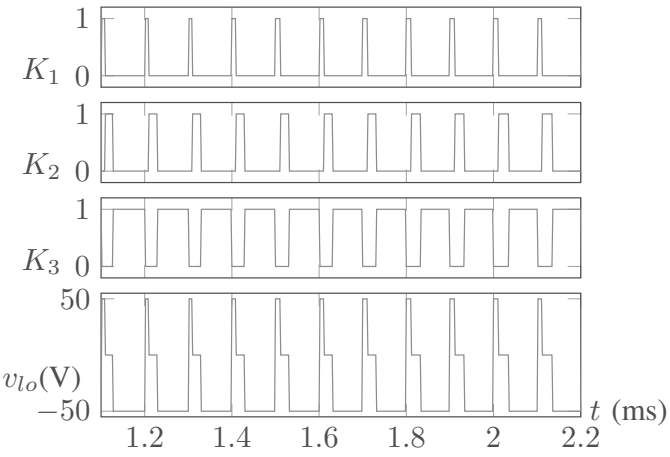
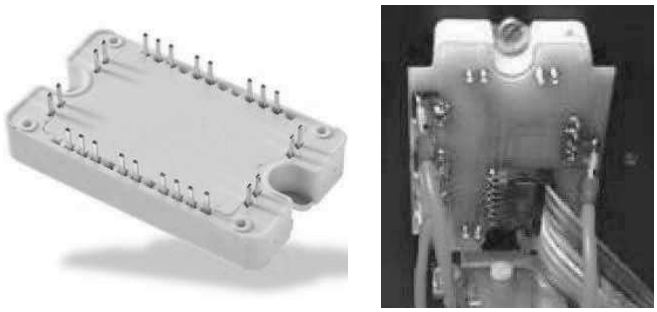



Fig. 12. Zoom on output voltage $v_{lo}$



(a) Supplied module. (b) Instrumented module.

Fig. 13. Microsemi T-type module.

switching losses and voltage edges, point of view. Simulation results are provided.

As far as the method is concerned, it is pointed out that a single carrier is needed while all possible solutions are highlighted. Because the modulating signal obtained is compatible to a time rate and related to a switching time, it can be inserted in a SVM scheme. This is due to the fact that the modulation modelling method is generic.

This study considered an insulated 3-switches cell. It is obvious that this structure can be connected to similar structures to build a 3-phases inverter. As far as the modulation model is considered, this method can be applied. Indeed, the model of the lines voltage of 3-phases inverter can be obtained by duplicating the line model on the three phases. The load model is then used to obtain the load voltage.

The model obtained is still consistent and also admits an infinity of solutions. Thus, the generalized inverse remains a suitable tool to handle the solution definition. The current work aims at dealing with the maximal rank factorization that exhibits the degrees of freedom of such a system.

Future work will provide experimental results of the proposed approach. The 3-phases inverter of the experimental testbench will be made of three normal T-type switching cells modules (APTGLQ40HR120CT3G from Microsemi in Fig 13). A classical scheme will be used for the control/command layer: the command signals will be send to the switches trough a DSPACE device embedded with FPGA in order to format the signals (i.e. inclusion of the dead time).

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