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Quentin Molin[a], Mehdi Kanoun[b,a], Christophe Raynaud[c,a], Hervé Morel[c,a]
[a]Supergrid Institute, 21 rue Cyprian, Villeurbanne 69611 CEDEX, France
[b]EDF R&D, Moret-sur-Loing 77818, France
[c]Univ Lyon, INSA Lyon, , Ampère UMR 5005, F-69621, France
quentin.molin@supergrid-institute.com

***Abstract*—The threshold voltage instability is a main reliability issue of Silicon Carbide MOSFET transistors. It is a critical parameter when it comes to give a failure in time rate for industrial power applications. In this context, a static ageing test based on JEDEC standard is proposed and the resulting gate oxide degradation is studied and discussed in this paper. Complementary testing was performed with dynamic reliability on the gate and the results obtained are used to add insight to the current discussion of SiC MOSFET reliability standards. Additionally, test bench and characterization protocols are detailed.**

Keywords—Silicon Carbide MOSFET, threshold voltage instability, gate bias stress, robustness, Keysight B1506A, JEDEC, reliability testing

I. Introduction

In power applications, the use of Silicon Carbide (SiC) material is now largely common. Its potential is indeed superior to Silicon (Si) [1]. For example, it has a wider bandgap of ~ 3.2 eV against 1.12 eV for Si and a critical field strength around ten times stronger resulting in that SiC transistors sustain a much higher voltage with lower static and commutation losses. These few semi-conductor parameters make SiC MOSFET devices good challengers for Si power module substitutions for HVDC applications.

However, the current state-of-the-art of this technology is not yet fully mature. There are still a lot of reliability issues that remain to be understood such as oxide degradation [2], threshold voltage instability [3], [4] and short-circuit behaviours [5], [6] and [7]. Industrial people are worried about some future power applications.

Reliability standards about ageing such components [8] are well documented, yet they have been established for Si power switches. Behaviour of SiC transistors during ageing is not like Si ones [9] and the scientific community is forced to question whether these standards are also suitable for SiC devices and how they should be modified [10]. However, standard tests are still a known base to provide more appropriate ageing test in a near future for SiC devices. This paper studies the gate instability behaviour in several ageing conditions: static HTGB (High Temperature Gate Bias [11]) and dynamic HTGS (High Temperature Gate switching [2], [12]) tests. The test bench designed for such reliability tests is also presented, along with the conditions of measurements of V_{TH}, which is a key parameter.

As previously shown [13], gate oxide of SiC MOSFET instability may come from its small barrier height ensuring easier injection. For conduction mode, a strong electric field in the dielectric is required because of the wide bandgap mentioned before.

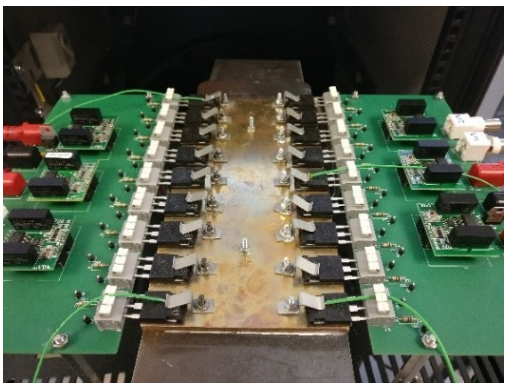
II. Experimental Set-Up

A. Test bench and ageing test definition

A test bench, see Fig. 1 (a), has been designed to run ageing tests on up to 18 MOSFETs at the same time. It allows to perform both static "HTGB" and dynamic "HTGS" reliability tests.

HTGB+ (resp. -) consists in ageing the device by applying a positive (resp. negative) bias on the gate. Because it is the mostly used nowadays in industrial data, this test was the first performed. HTGS consists in ageing the device by applying a rectangular bias on the gate (switching alternatively from V_{GS}^{Low} to V_{GS}^{High}, with a given duty cycle). This test is not a standard one.

(a)



(b)

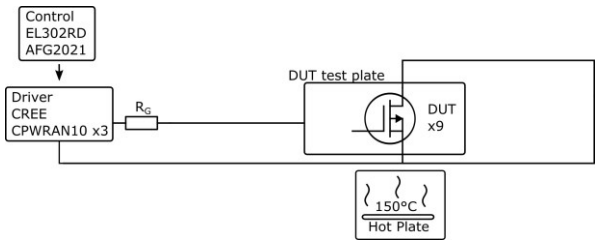


Fig. 1. (a) Ageing setup on the hotplate (tests running at 150°C). 18 MOSFETs (9x2) can be aged simultaneously (b) Scheme of ageing test

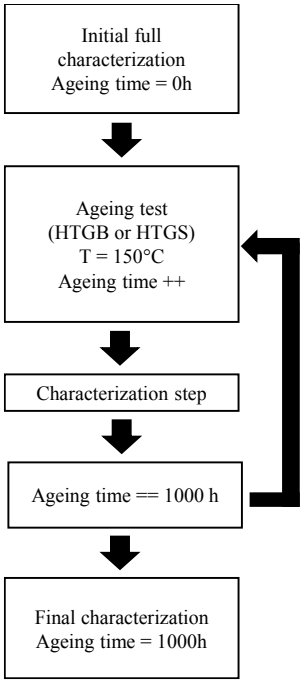


Fig. 2. Measurement protocol chart

During these tests, source and drain can either be short-circuited or be let floated. After performing both conditions, no significant differences were noted.

Using gate drives [14] able to drive three MOSFETs simultaneously, one PCB can age at full capacity 9 MOSFETs and two tests can run in the same time.

The gate drives showed in the Fig. 1 (b) allows a maximum range of 35 V between V_{GS}^{Low} and V_{GS}^{High}, and can operate at a maximum frequency of 100 kHz in this configuration (limited by the supplied current of the AL302RD power supply). The DUTs are disposed on a VECSTAR hotplate upgraded for this particular test bench with a maximum temperature shift of 2°C on its surface. Because of the time required to perform a reliability test (~1000 h) and the equipment availability at the time, choices were made to do a single HTGB+, and only two HTGSs. The complete ageing plan is presented in TABLE I. The positive HTGB ageing test was performed on 7 DUTs (D29 to D37).

HTGS2 (-8 V < V_{GS} < 25 V at 20 kHz) and HTGS3 (-10 V < V_{GS} < 20 V at 20 kHz) ageing tests have been performed on 9 DUTs each (TABLE 1) with three different duty cycles (α=20%, 50% and 80%).

B. Measurements Protocols

A Keysight B1506 was used to perform a datasheet-like (named thereafter "full") characterization of each component at a given time during ageing. The full ageing characterization process is presented in Fig. 2.

The main tracked parameters are the threshold voltage V_{TH}, the gate leakage current I_{GSS} at V_{GS} = 20 V and the on-state resistance R_{DSON} which is defined for V_{GS} = 20 V at the nominal current value I_{DS} = 50 A of the device. Those last two parameters were used only as qualitative indicators and it is important to say that R_{DSON} shift was negligible compared with the V_{TH} shift. The I_{GSS} value measured at 20 V was used to check the integrity of

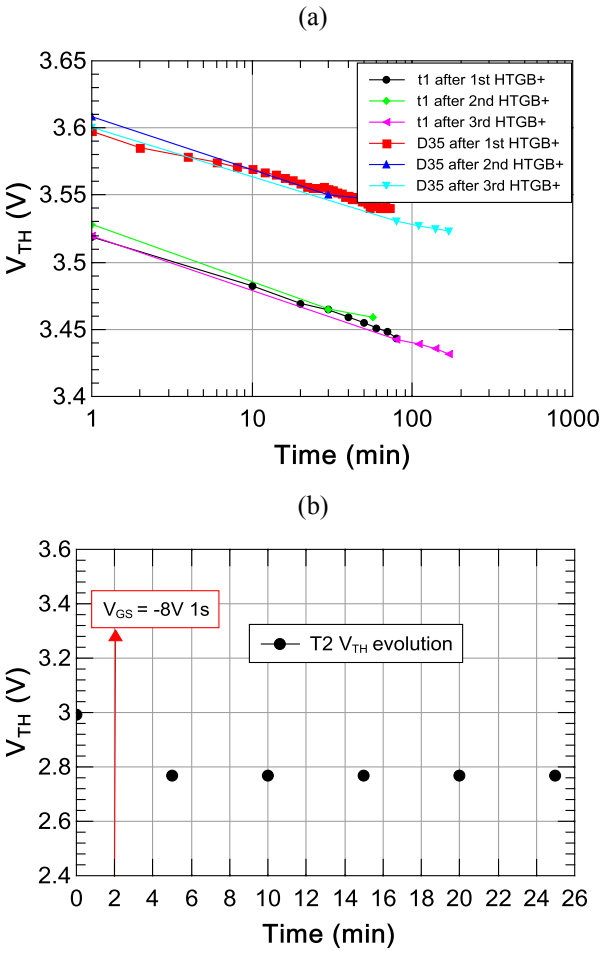


Fig. 3. (a) V_{TH} shift post stress at ambient temperature. D35 was already aged and T1 is brand new. Each component saw 3 runs of 20 min HTGB+ and 3 subsequent V_{TH} measurements with different steps in time. 1st run had 10 min measurement step, 2nd run had 30 min measurements steps and 3rd run had a 80 min wait then 30 min steps. (b) Validation of the V_{TH} measurement protocol on a clean component "T2" aged during 20 min at V_{GS} = 20V and ambient temperature T = 26 °C.

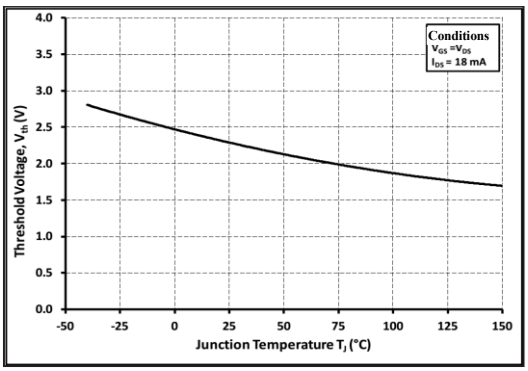


Fig. 4. V_{TH} behavior vs. junction temperature, measured at V_{GS}=V_{DS} when I_{DS} = 18 mA. [10]

the gate oxide. When I_{GSS} goes above a maximum value (fixed at 600 nA as stated on the electrical characteristics of the datasheet) the device was considered as failed one.

The stress test was interrupted regularly and the device went through a full characterization i.e classic direct and reverse I-V characteristics, C-V measurements (not shown in this paper).

TABLE I. AGEING TESTS AND PARAMETERS

	Tests (1000 h 150 °C)		
	HTGB+	*HTGS2*	*HTGS3*
VGS	20 V	-10 V 25 V	-8 V 20 V
VDS	Floating		
Ageing mode	Static	Dynamic f = 20 kHz	
DUTs	D29 → D37	$\alpha_{20\%}$: D10, 11, 12 $\alpha_{50\%}$: D13, 14, 15 $\alpha_{80\%}$: D16, 17, 18	$\alpha_{20\%}$: D25, 26, 27 $\alpha_{50\%}$: D22, 23, 24 $\alpha_{80\%}$: D19, 20, 21
Parameters	V_{TH}, R_{DSON}, I_{GSS}		

For the threshold voltage measurement we applied the datasheet recommendations which consist on shorting Drain and Source and sweeping the voltage bias between the Gate and the Source until I_{DS} = 18 mA. The recorded V_{GS} at this point corresponds to the V_{GS}.

Unfortunately, as shown on the Fig. 3 (a) there is a time dependent shift on the threshold voltage which seems to be related to the recent ageing. No stabilization has been observed up to ~ 200 min. To avoid this phenomenon a negative bias of -8 V for ~ 1 s was applied before measuring V_{TH}. Fig. 3 (b) shows the V_{TH} measurement recorded with this method. As it can be noticed V_{TH} is rapidly stabilized. All following measurements have been performed with this protocol.

It is also worth noticing the strong dependence of the gate voltage on the temperature as represented on Fig. 4. If the room temperature goes from 25 °C to 35 °C for example, the shift on the threshold voltage according to those 10 °C difference is equal to approximately ΔV_{TH} = 50 mV. This value is of the same order of magnitude as the degradation of the ageing DUT. Ambient temperature monitoring during characterization is critical. Hence threshold voltage values have been corrected to take into account this phenomenon.

C. *Reliability testing plan*

C2M0045170D devices were bought and went under the stress setup plan presented on the Fig. 2.

So far, at our best knowledge, no ageing data on industrial 1700V 45 mΩ SiC MOSFET have been published. During the tests there was no current flowing into the device as it was decided to separate stressing accelerated factors from each other's [8].

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. *HTGB+ static test*

I_{GSS} and R_{DSON} data have been monitored but as they do not show any significant shifts, only V_{TH} parameter variations are described in the following.

All the presented DUTs went under a full characterization at t = 0 h (before any stress). Fig. 5 shows the recorded initial V_{TH} for each measured device. Note that the spreading of V_{TH} could reach 1.05 V, which is very high. This observation adds some questioning about the industrial processes of the gate voltage on market available components. Moreover, this is critical for paralleling power switches. Indeed, although each component will finally have a similar R_{DSON} thanks to its positive

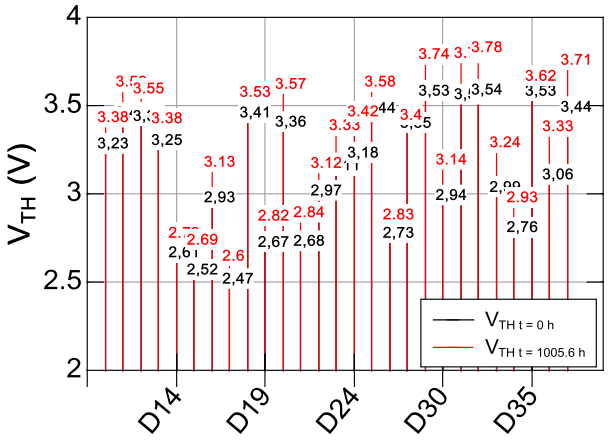


Fig. 5. Initial V_{TH} @t = 0 h in black and final in red @t = 1030.1 h on all DUTs under HTGB (D29 -> D37) and HTGS (D10 ->D27) test at ambient temperature.

temperature coefficient and balancing phenomena, some devices will heat more than others and then could prematurely age.

The Fig. 6 (a) shows the variation of the normalized V_{TH} to the initial value. As we can notice, a positive shift on the threshold voltage occurs. This can be explained by negative charge trapping either in the SiO_2/SiC interface states or in deeper traps in the oxide.

For each component of HTGB+, the minimum positive shift is about 5% with a maximum of 8% for D36.

The degradation kinetic does not seem to saturate and the curves do not seem to get stable, which means that the degradation can even be worse if the test runs longer and maybe reach a saturation mode at some point. In addition, this behavior is not similar to the one already published by the supplier on the previous generation (1200 V MOSFET). This could be either due to the immaturity of this generation process or to the non-adapted stress conditions we used in this study.

B. *HTGS dynamic test*

Working only on static ageing test is not representative of the power device applications. In this matter, dynamic ageing is more interesting to look into. Influences of V_{GS}^{High} and V_{GS}^{Low}, high commutation frequency and duty cycle are all parameters that companies are interested in. In this part, influence of several parameters such as V_{GS} values, commutation frequency and duty cycle were investigated on 18 other similar devices.

The frequency of 20 kHz has been chosen because it is representative of the industrial application reality. It is common to extrapolate ageing data to see the critical parameters shift in a longer period of time. 10 years (~100 000 h) represent the average lifetime requirement for power converter applications.

Fig. 6 (b) shows the ageing data of the HTGS2 for three different duty cycles. Those testing conditions result in a mean positive shift on all the 9 DUTs of approximately V_{TH}^{HTGS2} = 170 mV. Except for D18, they all saw a >5% positive shift on their initial threshold voltage value. No significant differences are observed in Fig. 6 (c) for HTGS3 ageing data.

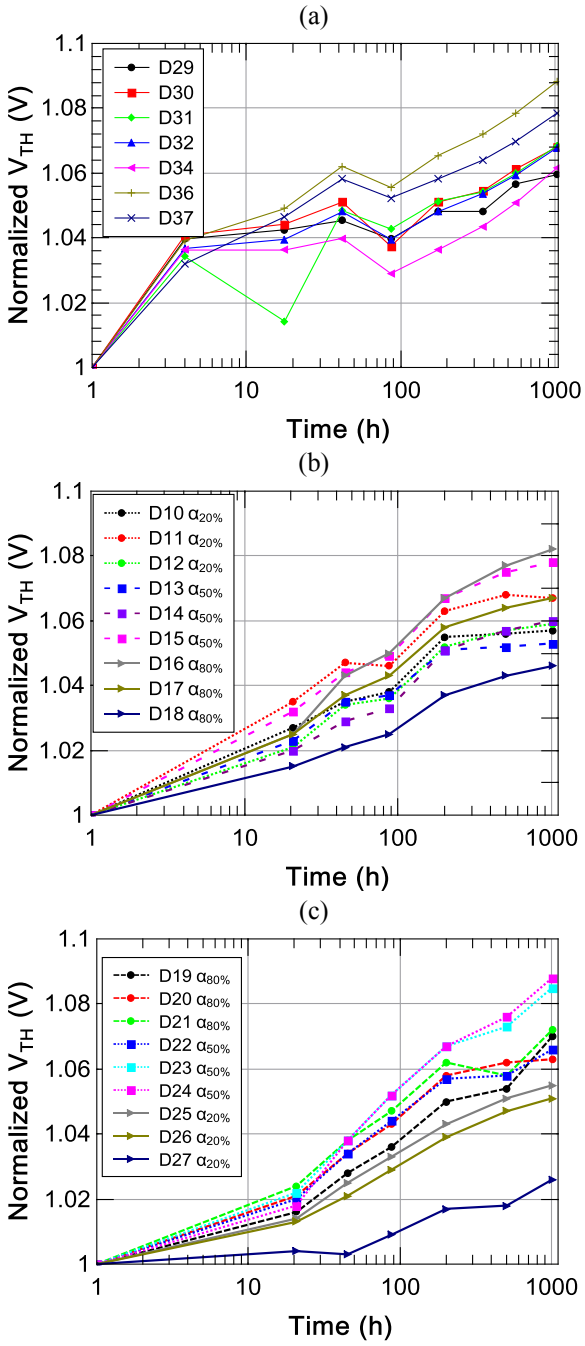


Fig. 6. (a) Normalized threshold voltage shift during HTGB+ static ageing at ambient temperature. (b) Normalized threshold voltage shift during HTGS2 dynamic ageing. (c) Normalized threshold voltage shift during HTGS3 dynamic ageing.

It is interesting to look at the influence of the duty cycle on the Fig. 7 (a):

$\alpha_{20\%}$: 6.1% positive shift
$\alpha_{50\%}$: 6.4% positive shift
$\alpha_{80\%}$: 7.2% positive shift

Although the high impact of the duty cycle was already pointed out in the literature we did not see its influence in our experimental results. This could be due to the higher frequency of 20 kHz used in our experiments in regards to the frequency of 10 kHz used in [12]. Fig. 6 (c) shows similar results to the HTGS2 ageing test but with a higher $V_{GS}^{High} = 25$ V (HTGS3).

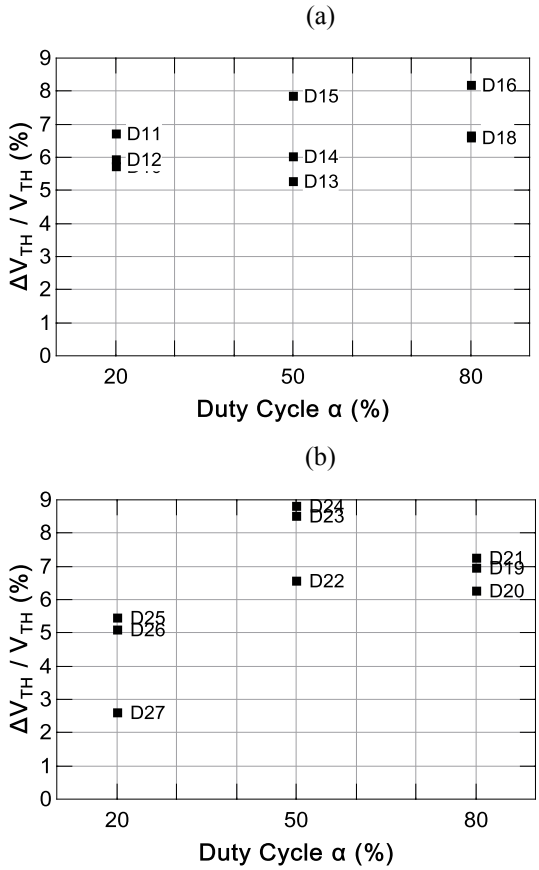


Fig. 7. (a) HTGS2 $\Delta V_{TH}/ V_{TH}$ (%) for three different duty cycle, α = 20%, 50% and 80% (b) HTGS3 $\Delta V_{TH}/ V_{TH}$ (%) for three different duty cycle, α = 20%, 50% and 80%

All the data gathered during this test show a mean positive shift of $V_{TH}^{HTGS3} = 160$ mV which is similar to that obtained in the previous test. No differences are noticed. The relative positive shift does not depend monotonically of the duty cycle: 6.8%, (resp. 8%) for a duty cycle of 20% (resp. 50%), but only 5.3% for a duty cycle of 80%. Due to the low number devices tested for each duty cycle, this little difference is probably not representative.

However, extrapolated relative V_{TH} shift at 100000 h (~10 years), is ~15%. This result is of the same order than that observed in 1200 V SiC MOSFET. It is a crippling factor for MOSFET uses in power electronics.

On Fig. 6 (c) and Fig. 7 (b) one particular behaviour is to notice from those graphs is the non-ageing curve of DUT D27. This device failed during ageing between the 200th hour of the characterization step and the 504th hour. I_{GSS} value went from some pA value on the Keysight B1506 to the compliance that has been set to 1mA. As the gate leakage value was monitored, there was absolutely zero sign of strong degradation of the gate oxide. As mentioned before in the literature such as [16], I_{GSS} cannot be used as an indicator to predict failure on MOS devices. However, the gate leakage current characterization at $V_{GS} = 20$ V can be used to show failure. All other parameters on D27 did not show any signs of degradation and I_D-V_D had the same values.

This failure was unexpected as those components were industrial, and under HTGS ageing. Nevertheless, the

recommended rating of 20 V for V_{GS}^{High} and -5 V for V_{GS}^{Low} on the gate voltage was not respected.

Concerning HTGS2, DUT with α = 50% seems to have reached an asymptote at 1000 h of ageing. Changing the duty cycle at such a high frequency must be something to be treated with caution though in some applications that require such a parameter to be set.

IV. CONCLUSION

This paper presents the first ageing study on 1700 V 45 mΩ SiC-MOSFET. Standard reliability HTGB test was performed to investigate the behaviour of the gate oxide. The non-saturation of the V_{TH} with time we have observed in this study is quite worrying. Nonetheless extrapolating the ageing time up to 100 000 hours shows a positive shift of the threshold voltage around 15 %. This result is comparable to the one obtained on 1200 V SiC MOSFET and hence it is non-critical.

A SiC MOSFET is used mainly for the high commutation frequency. For this purpose HTGS is presented in this work. It is a rather new ageing test which is quite representative of the actual operation mode of such power devices. The positive V_{TH} derive, under HTGS, observed in this work implies that the devices are not mature yet. Moreover, those results address the importance of this specific reliability test which is not accounted as a standard one. It could be worth to include the HTGS test in the reliability qualification protocol.

In this paper we have pointed out a very important phenomenon related to the stability of the recorded V_{TH} after ageing. Indeed, a discharging phenomenon is observed and a measurement protocol was proposed. A deeper investigation and a better understanding of this phenomenon are needed in the near future.

V. ACKNOWLEDGEMENT

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REFERENCES

[1] G. Liu, B. R. Tuttle, and S. Dhar, "Silicon carbide: A unique platform for metal-oxide-semiconductor physics," *Appl. Phys. Rev.*, vol. 2, no. 2, p. 021307, Jun. 2015.

[2] R. Ouaida, M. Berthou, J. Leon, X. Perpina, S. Oge, P. Brosselard, and C. Joubert, "Gate Oxide Degradation of SiC MOSFET in Switching Conditions," 2014.

[3] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[4] T. Kikuchi and M. Ciappa, "Modeling the threshold voltage instability in SiC MOSFETs at high operating temperature," in *Reliability Physics Symposium, 2014 IEEE International*, 2014, p. 2C–4.

[5] M. Berthou, P. Bevilacqua, J. Fonder, and D. Tournier, "Repetitive Short-Circuit tests on SiC VMOS devices," *proceedings of the 10th ECSCRM*, 2015.

[6] A. Castellazzi, T. Funaki, T. Kimoto, and T. Hikihara, "Short-circuit tests on SiC power MOSFETs," in *Power Electronics and Drive Systems (PEDS), 2013 IEEE 10th International Conference on*, 2013, pp. 1297–1300.

[7] C. Chen, D. Labrousse, S. Lefebvre, M. Petit, C. Buttay, and H. Morel, "Robustness in short-circuit Mode of SiC MOSFETs," in *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, 2015, pp. 1–8.

[8] JEDEC, *Temperature, Bias, and Operating Life - 22A108D*. 2011.

[9] L. C. Yu, G. T. Dunne, K. S. Matocha, K. P. Cheung, J. S. Suehle, and K. Sheng, "Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments," *Device and Materials Reliability, IEEE Transactions on*, vol. 10, no. 4, pp. 418–426, Dec. 2010.

[10] "ECPE SiC & GaN User Forum: Potential of Wide Bandgap Semiconductors in Power Electronic Applications." .

[11] A. J. Lelis, R. Green, and D. B. Habersat, "SiC MOSFET reliability and implications for qualification testing," in *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. 2A–4.1–2A–4.4.

[12] A. Fayyaz and A. Castellazzi, "High temperature pulsed-gate robustness testing of SiC power MOSFETs.," *Microelectronics Reliability*, vol. 55, no. 9–10, pp. 1724–1728, 2015.

[13] R. Singh and A. R. Hefner, "Reliability of SiC MOS devices," *Solid-State Electronics*, vol. 48, no. 10–11, pp. 1717–1720, Oct. 2004.

[14] Wolfspeed, "CPWR-AN10, REV -C SiC MOSFET Isolated Gate Driver." 2014.

[15] P. Fiorenza, A. Frazzetto, A. Guarnera, M. Saggio, and F. Roccaforte, "Fowler-Nordheim tunneling at SiO2/4H-SiC interfaces in metal-oxide-semiconductor field effect transistors," *Applied Physics Letters*, vol. 105, no. 14, p. 142108, 2014.

[16] D. Othman, S. Lefebvre, M. Berkani, Z. Khatir, A. Ibrahim, and A. Bouzourene, "Robustness of 1.2 kV SiC MOSFET devices," *Microelectronics Reliability*, vol. 53, no. 9–11, pp. 1735–1738, 2013.