



## Impact of a $\gamma$ -Al<sub>2</sub>O<sub>3</sub>(001) barrier on LaAlO<sub>3</sub> metal-oxide-semiconductor capacitor electrical properties

L. Becerra, C. Merckling, M. El-Kazzi, N. Baboux, B. Vilquin, Guillaume Saint-Girons, C. Plossu, G. Hollinger

### ► To cite this version:

L. Becerra, C. Merckling, M. El-Kazzi, N. Baboux, B. Vilquin, et al.. Impact of a  $\gamma$ -Al<sub>2</sub>O<sub>3</sub>(001) barrier on LaAlO<sub>3</sub> metal-oxide-semiconductor capacitor electrical properties. Journal of Vacuum Science & Technology B Microelectronics and Nanometer Structures, 2009, 27 (1), pp.384-388. 10.1116/1.3065437 . hal-01939927

**HAL Id: hal-01939927**

**<https://hal.science/hal-01939927>**

Submitted on 17 Nov 2022

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

# Impact of a $\gamma$ -Al<sub>2</sub>O<sub>3</sub>(001) barrier on LaAlO<sub>3</sub> metal-oxide-semiconductor capacitor electrical properties

L. Becerra,<sup>a)</sup> C. Merckling, and M. El-Kazzi

*Institut des Nanotechnologies de Lyon, Université de Lyon, INL-UMR 5270, CNRS, Ecole Centrale de Lyon, 36 Avenue Guy de Collongue, Ecully F-69134, France*

N. Baboux

*Institut des Nanotechnologies de Lyon, Université de Lyon, INL-UMR 5270, CNRS, INSA de Lyon, 7 Avenue Jean Capelle, Villeurbanne F-69621, France*

B. Vilquin and G. Saint-Girons

*Institut des Nanotechnologies de Lyon, Université de Lyon, INL-UMR 5270, CNRS, Ecole Centrale de Lyon, 36 Avenue Guy de Collongue, Ecully F-69134, France*

C. Plossu

*Institut des Nanotechnologies de Lyon, Université de Lyon, INL-UMR 5270, CNRS, INSA de Lyon, 7 Avenue Jean Capelle, Villeurbanne F-69621, France*

G. Hollinger

*Institut des Nanotechnologies de Lyon, Université de Lyon, INL-UMR 5270, CNRS, Ecole Centrale de Lyon, 36 Avenue Guy de Collongue, Ecully F-69134, France*

(Received 8 June 2008; accepted 8 December 2008; published 9 February 2009)

Amorphous LaAlO<sub>3</sub> high- $\kappa$  oxides were grown in a molecular beam epitaxy reactor on *p*-Si(001) employing a thin  $\gamma$ -Al<sub>2</sub>O<sub>3</sub> epitaxial layer as buffer. Interfaces are free of SiO<sub>2</sub> and silicates and remain abrupt even after high temperature annealing as demonstrated by x-ray photoelectron spectroscopy. Electrical measurements performed on as-deposited samples reveal dielectric constant values close to the bulk ones, small equivalent oxide thickness, and low interface state densities. Some negative charges are present leading to a flatband voltage shift. Postdeposition annealing can correct this effect. © 2009 American Vacuum Society. [DOI: 10.1116/1.3065437]

## I. INTRODUCTION

To prevent direct tunneling current leakage and satisfy the International Technology Roadmap for Semiconductors (ITRS),<sup>1</sup> high- $\kappa$  dielectrics have recently been introduced into the last generation of metal-oxide-semiconductor field-effect transistors. However problems will occur and solutions should be found for the 22 nm and sub-22 nm nodes. The main objective, and difficulty, will be to obtain very small equivalent oxide thickness (EOT) as low as 0.5 nm with an abrupt high- $\kappa$  oxide/silicon interface, while keeping a tolerable gate leakage current.

LaAlO<sub>3</sub> (LAO) lanthanum aluminate oxide is identified as one of the most promising candidate for future technology generations. In a former study,<sup>2</sup> we have demonstrated the potentialities of LAO to reach small EOTs according to the ITRS recommendations.<sup>1</sup> Used in its amorphous phase and taking care to keep the interface free of silicates, we succeeded in obtaining good electrical features.<sup>2</sup> Nevertheless, the amorphous LAO/Si(001) system presents one non-negligible drawback: after postdeposition annealing (PDA), an interfacial layer growth is often observed leading to an increase of the EOT.<sup>3</sup> To prevent this reaction of SiO<sub>2</sub>-silicate formation, we have developed an interface engineering strategy. A thin  $\gamma$ -Al<sub>2</sub>O<sub>3</sub>(001) crystalline layer is

grown by molecular beam epitaxy (MBE) on the Si(001) substrate before LAO deposition. We selected Al<sub>2</sub>O<sub>3</sub> as a buffer layer because it is known to be thermodynamically stable on silicon at high temperature. Consequently, as demonstrated in our previous works,<sup>4,5</sup> the Al<sub>2</sub>O<sub>3</sub> buffer layer allows growing LAO with an abrupt interface at high temperature even if oxygen is introduced in the reaction chamber at an early stage of the growth. Moreover Al<sub>2</sub>O<sub>3</sub> has a large energy band gap of 9 eV. Although its dielectric constant ( $k \approx 10$ ) is moderate compared to LAO one, it remains relatively high compared to SiO<sub>2</sub>. By limiting the interfacial Al<sub>2</sub>O<sub>3</sub> layer thickness, it is then possible to reach low EOT without any significant increase in tunneling current compared to LAO layers directly grown on Si and having the same EOT. As an illustration, Fig. 1 compares simulated current density-voltage (*J-V*) characteristics of both stacks with the same 1 nm EOT, obtained using a homemade quantum simulator (TCV).<sup>6</sup> This software allows fast calculations of capacitance-voltage curves based on tabulated charge versus band bending data obtained from a Poisson-Schrödinger solver. The LAO and Al<sub>2</sub>O<sub>3</sub> dielectric constants have been, respectively, taken equal to 20 and 10. For the LAO/Si stack, the LAO physical thickness is 5.13 nm. For the LAO/Al<sub>2</sub>O<sub>3</sub>/Si stack, the LAO thickness is 3.53 nm over an Al<sub>2</sub>O<sub>3</sub> interfacial layer of 0.8 nm. For reference, the *J-V* characteristic of a 1 nm SiO<sub>2</sub> gate oxide is also shown. As expected, tunneling currents are drastically reduced for LAO and LAO/Al<sub>2</sub>O<sub>3</sub> stacks compared to SiO<sub>2</sub> but are compa-

<sup>a)</sup> Author to whom correspondence should be addressed; Tel.: +33 (0)4 72 18 60 49; electronic mail: loic.becerra@ec-lyon.fr

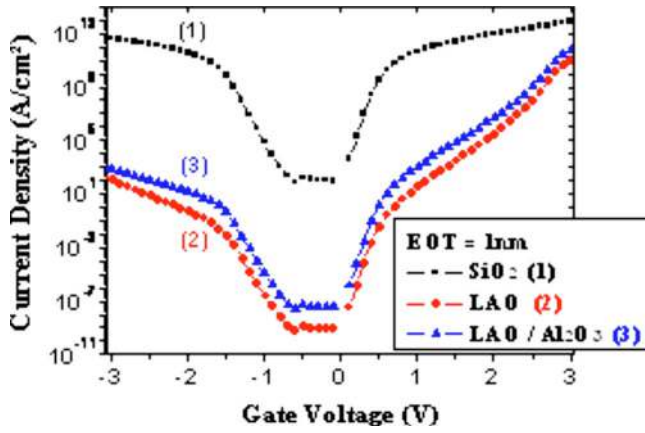


FIG. 1. (Color online) Simulated current-voltage characteristics of 1 nm EOT LAO/Al<sub>2</sub>O<sub>3</sub> and LAO gate stacks compared to 1 nm SiO<sub>2</sub>. Parameters used for simulations are metal gate work function  $\Phi_M=4.5$  eV; LaAlO<sub>3</sub>: dielectric constant  $k=20$ , effective electron mass  $m_{\text{eff}}=0.3m_0$ ,  $m_0$  being the electron mass, band gap  $E_g=5.6$  eV, potential barrier height at the silicon interface  $\Phi_B=1.8$  eV; Al<sub>2</sub>O<sub>3</sub>:  $k=10$ ,  $m_{\text{eff}}=0.35m_0$ ,  $E_g=9$  eV,  $\Phi_B=2.8$  eV; SiO<sub>2</sub>:  $k=3.9$ ,  $m_{\text{eff}}=0.5m_0$ ,  $E_g=9.1$  eV,  $\Phi_B=3.1$  eV.

rable for the two high- $k$  systems (one decade larger for LAO/Al<sub>2</sub>O<sub>3</sub>). Therefore, even if the introduction of a 0.8 nm Al<sub>2</sub>O<sub>3</sub> barrier leads to a reduction of the entire gate stack physical thickness for reaching the same EOT, it has no important impact on leakage current.

In this contribution, we report on improvements about the gate stack thermal stability thanks to the interfacial Al<sub>2</sub>O<sub>3</sub> layer and we discuss electrical results obtained on MOS capacitors.

## II. EXPERIMENT

The samples were grown by MBE on  $p$ -type Si(001) substrates (doping concentration  $\approx 1 \times 10^{16}$  cm<sup>-3</sup>) in an ultra-high vacuum Riber 2300 reactor. Bulk LAO and Al<sub>2</sub>O<sub>3</sub> were evaporated using an electron beam gun. The growth was followed *in situ* by reflection high energy electron diffraction (RHEED) monitoring using a 30 kV RHEED system. For samples with alumina at the interface, a thin pseudomorphic  $\gamma$ -Al<sub>2</sub>O<sub>3</sub>(001) layer was deposited at 850 °C with an oxygen pressure of  $10^{-8}$  Torr.<sup>4,5</sup> A streaky RHEED pattern appears after the growth of this layer, showing a  $1 \times 5$  reconstruction along the [001] direction. RHEED also shows that the Al<sub>2</sub>O<sub>3</sub>/Si interface is coherent. For more details, see Ref. 5. The deposition of amorphous LAO was then performed at 400 °C with an oxygen pressure around  $5 \times 10^{-6}$  Torr. Oxygen was introduced in the reactor at the beginning of the LAO growth. For samples without interfacial Al<sub>2</sub>O<sub>3</sub>, LAO was directly deposited at 400 °C on the  $2 \times 1$  reconstructed Si surface, tuning the oxygen pressure to prevent interface degradation and to minimize oxygen vacancies in the oxide. Thermal stability was studied by performing postdeposition annealings under N<sub>2</sub> or forming gas atmosphere, either in a tubular furnace at 200 or 300 °C during 30 min or in a rapid thermal furnace (RTA) during a few seconds, for temperatures varying between 300 and 600 °C under atmospheric pressure.

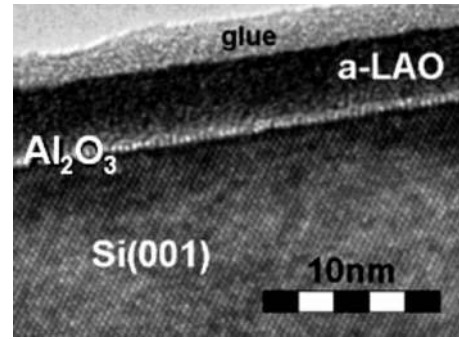


FIG. 2. TEM image showing 3.8 nm of amorphous LaAlO<sub>3</sub> on 0.8 nm of crystalline  $\gamma$ -Al<sub>2</sub>O<sub>3</sub>(001) on a Si(001) substrate. The entire stack presents abrupt interfaces.

The physical properties of the films were investigated using x-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM). To study electrical properties, MOS capacitors were fabricated by a lift-off technique and by evaporating Ni (3 nm)/Au (300 nm) metal square ( $95 \times 95$   $\mu\text{m}^2$ ) electrodes on LAO. The bulk contact was taken at the wafer backside. Variable frequency capacitance-voltage ( $C$ - $V$ ) measurements were performed using an Agilent 4284 impedance meter. Main electrical parameters such as EOT and flatband voltage were extracted by fitting experimental curves with TCV simulations<sup>6,7</sup> taking into account quantum effects in the silicon substrate. The interface state density was estimated by comparing experimental  $C$ - $V$  curves obtained at low and high frequencies.

## III. RESULTS AND DISCUSSION

TEM experiments were performed on LAO/Al<sub>2</sub>O<sub>3</sub>/Si stacks to measure the physical thicknesses of the two dielectric layers. A typical TEM image is shown in Fig. 2 which reveals the presence of a  $3.8 \pm 0.2$  nm thick LAO layer on a crystalline alumina layer with a uniform thickness of  $0.8 \pm 0.2$  nm. The Si-Al<sub>2</sub>O<sub>3</sub> interface is sharp at the atomic scale and no presence of silicates or SiO<sub>2</sub> is revealed. The LAO surface is flat.

Thermal stability was first investigated by XPS measurements. Samples with equivalent EOT values, with and without interfacial Al<sub>2</sub>O<sub>3</sub> were annealed under N<sub>2</sub> atmosphere. Figure 3 compares XPS spectra of Si 2s core levels obtained before and after annealing in both tubular [Fig. 3(a)] and RTA [Figs. 3(b) and 3(c)] furnaces. The sharp and strong peak at 150.9 eV is attributed to the Si 2s component of the silicon substrate. The apparition of a component around 154 eV is associated with the formation of SiO<sub>2</sub> and silicates at the silicon interface. All as-deposited stacks exhibit silicate free interface. After annealing, the interface of Al<sub>2</sub>O<sub>3</sub> with the Si substrate remains abrupt up to 500 °C [Figs. 3(a) and 3(c)] while silicates appear for the LAO/Si system above 300 °C [Figs. 3(a) and 3(b)]. Above 500 °C, silicates formation begins even for LAO/Al<sub>2</sub>O<sub>3</sub>/Si [Fig. 3(c)]. These XPS experimental results evidence the “protective” role of the crystalline alumina barrier during PDA under N<sub>2</sub> ambient, for temperatures up to 500 °C.

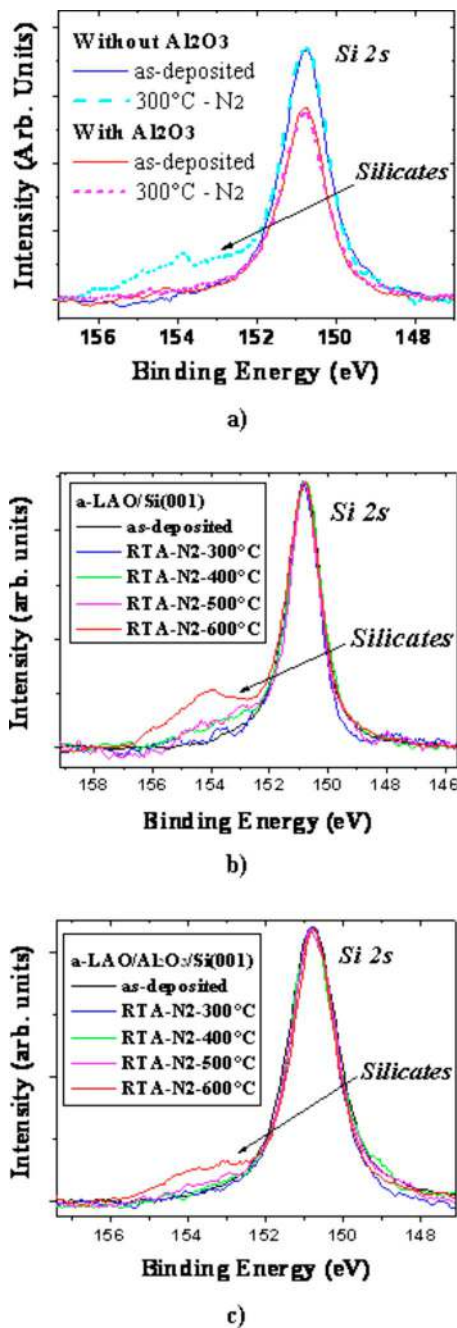


FIG. 3. (Color online) XPS spectra of Si 2s core level (a) LAO/Al<sub>2</sub>O<sub>3</sub>/Si and LAO/Si samples before and after annealing in a tubular furnace under N<sub>2</sub> atmosphere at 300 °C, (b) LAO/Si samples before and after annealing in a RTA furnace under N<sub>2</sub> atmosphere at 300, 400, 500, and 600 °C, (c) LAO/Al<sub>2</sub>O<sub>3</sub>/Si samples before and after annealing in a RTA furnace under N<sub>2</sub> atmosphere at 300, 400, 500, and 600 °C.

Figure 4 shows typical capacitance versus gate voltage (*C-V*) measurements of as-deposited LAO/Al<sub>2</sub>O<sub>3</sub> capacitors performed at various frequencies between 1 kHz and 1 MHz, in the impedance-meter serial measurement mode. One can observe that the maximum equivalent series capacitance in accumulation regime (negative gate voltages) is weakly dependent on the measurement frequency. This proves that the leakage current of the dielectric stack ( $\sim 10^{-4}$  A/cm<sup>2</sup> for a gate voltage of  $-1.5$  V) is low enough to ensure that the

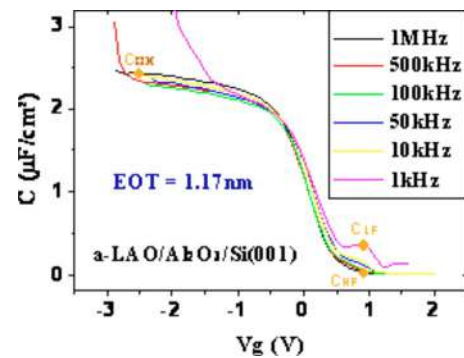


FIG. 4. (Color online) Frequency *C-V* measurements from 1 kHz to 1 MHz on as-deposited Au/Ni/LAO/Al<sub>2</sub>O<sub>3</sub>/Si MOS capacitors.

parallel conductance of the device under test has a negligible influence on the displayed series capacitance measured in accumulation regime.<sup>8</sup> Therefore this displayed capacitance is really representative of the dielectric stack capacitance and allows a reliable determination of the dielectric stack EOT. Using the TCV simulator<sup>6</sup> to fit experimental *C-V* [Fig. 5(a)], EOT is estimated to be  $1.31 \pm 0.02$  nm. Then, assuming an Al<sub>2</sub>O<sub>3</sub> dielectric constant of 10, and using the LAO and Al<sub>2</sub>O<sub>3</sub> physical thicknesses evaluated by TEM measurements (6 and 0.8 nm, respectively, for this sample), the calculated dielectric constant of the amorphous LAO layer is 23.4

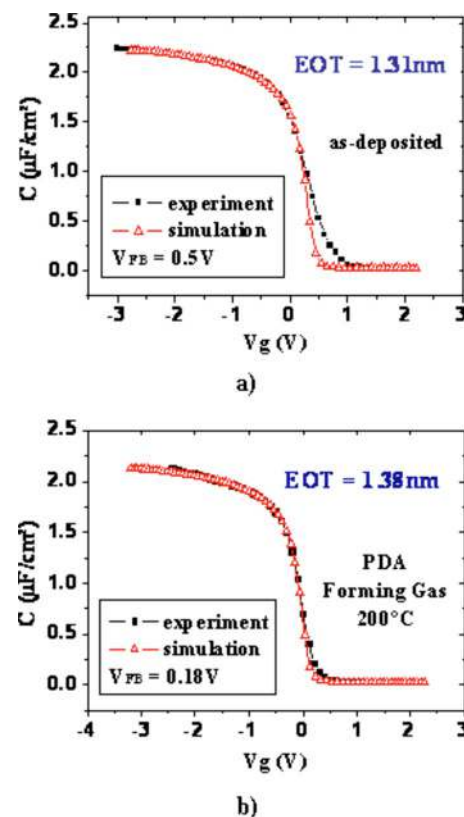


FIG. 5. (Color online) Comparison of experimental (1 MHz) and simulated *C-V* characteristics of Au/Ni/LAO/Al<sub>2</sub>O<sub>3</sub>/Si capacitors. (a) As-deposited EOT=1.31 nm and (b) after a 200 °C PDA in a tubular furnace, EOT=1.38 nm.



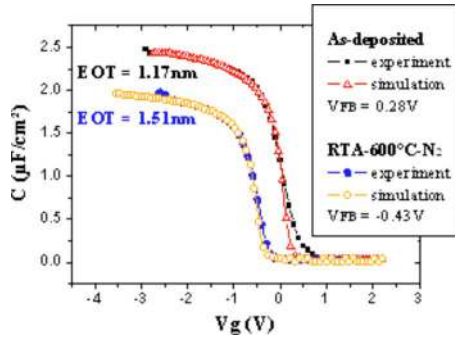


FIG. 6. (Color online) Comparison of experimental (1 MHz) and simulated C-V characteristics of Au/Ni/LAO/Al<sub>2</sub>O<sub>3</sub>/Si capacitors, as deposited (EOT=1.17 nm) and after a 600 °C RTA annealing (EOT=1.51 nm).

which is very close to the theoretical value (25) (Refs. 9 and 10) of bulk LAO. The smallest EOT we obtained for LAO/Al<sub>2</sub>O<sub>3</sub> system is  $1.10 \pm 0.02$  nm. However it should be noted that a quick theoretical calculation shows that a 0.96 nm LAO ( $\kappa=20$ )/0.8 nm Al<sub>2</sub>O<sub>3</sub> ( $\kappa=10$ )/Si stack leads to an EOT equal to 0.5 nm. The flatband voltage  $V_{FB}$  of as-deposited samples was extracted from C-V simulation of Fig. 5(a).  $V_{FB}$  is found equal to 0.5 V which is much higher than the theoretical  $V_{FB}$  (−0.5 V) of Ni gate MOS capacitors without any bulk oxide charge. The positive shift ( $\Delta V_{FB} = 1$  V) between theoretical and extracted  $V_{FB}$  values indicates that as-deposited samples exhibit a large amount of negative charges in the bulk dielectric. Moreover the discrepancy in the depletion regime between experimental and calculated (without any interface states) C-V curves in Fig. 5(a) indicates the presence of interface states at the silicon interface. This is confirmed by the influence of the measurement frequency in depletion regime on experimental C-V curves in Fig. 4. For a given gate voltage, between 0 and 1 V, the measured capacitance gradually increases with decreasing frequency. This is attributed to the capacitance associated to the response of fast interface states at the silicon interface. The interface state density  $D_{it}$  can be roughly determined using the Castagné and Vapaille method<sup>11</sup> according to the following equation:

$$D_{it} = \frac{1}{q} \left[ \left( \frac{1}{C_{LF}} - \frac{1}{C_{ox}} \right)^{-1} - \left( \frac{1}{C_{HF}} - \frac{1}{C_{ox}} \right)^{-1} \right], \quad (1)$$

where  $q$  is the electron charge,  $C_{ox}$ ,  $C_{LF}$ , and  $C_{HF}$  are, respectively, the capacitance per unit area measured in accumulation regime, in depletion regime at low frequency (1 kHz) and at high frequency (1 MHz). We estimated a  $D_{it}$  value of  $2.4 \times 10^{12}$  eV<sup>−1</sup> cm<sup>−2</sup> for as-deposited samples. To address the issue of bulk negative charges, we have performed post-deposition annealings in different conditions. The influence of PDA on bulk and interface state densities is shown in Fig. 5 for the case of a 200 °C PDA in a tubular furnace and in Fig. 6 for a 600 °C RTA annealing. A 30 min PDA at 200 °C in a forming gas atmosphere was found to decrease the fixed charge density since  $V_{FB}$  was reduced from 0.5 to 0.18 V. The interface state density  $D_{it}$  was reduced by a factor of 2 while the EOT is very slightly affected, demonstrating that

the interfaces are still abrupt after a 200 °C PDA as predicted by XPS results. A RTA annealing at 600 °C (Fig. 6) greatly improves  $V_{FB}$  (−0.43 V) leading to a very low bulk oxide charge level. The interface state density is also reduced. Unfortunately it can be observed in Fig. 6 that the maximum capacitance decreases after RTA annealing so that the EOT increases from 1.17 to 1.51 nm. This is not surprising since the formation of silicates after annealing at temperature above 600 °C was revealed by XPS measurements of Fig. 3(c).

#### IV. CONCLUSION

We succeeded in accomplishing capacitor stacks with high- $\kappa$  oxides by MBE. A thin  $\gamma$ -Al<sub>2</sub>O<sub>3</sub> crystalline buffer is first grown to prevent SiO<sub>2</sub> or silicates formation at the silicon substrate interface. Then, an amorphous LAO layer with a high permittivity close to that of bulk LAO one is deposited. Small EOTs down to 1.1 nm and moderate interface charge densities were achieved. Nevertheless a great amount of bulk negative charges was evidenced in as-deposited stacks. We have shown that a postdeposition annealing in forming gas atmosphere at a moderate temperature partly cures the bulk charge and improves the silicon interface quality. Although the bulk charges can be further reduced by a high temperature (600 °C) RTA annealing, this induces an increase in EOT due to the formation of silicates at the silicon interface as predicted by XPS measurements. Consequently, a compromise must be found: the PDA temperature must be high enough to minimize bulk and interface states but sufficiently low (<600 °C) to avoid the formation of silicates at the silicon interface.

We believe that the appearance of an interfacial layer of SiO<sub>2</sub> or SiO<sub>x</sub> is not due to interfacial reactions between LAO and Si or Al<sub>2</sub>O<sub>3</sub> and Si. Rather we think that we have some hydrated or carbonaceous species adsorbed on the oxide surface. So, during annealing, the surface oxygen species are believed to diffuse to the interface and to react with Si to give an interfacial layer. Moreover, oxygen vacancies could favor diffusion of oxygen species. One of our ideas will be now to limit sample exposure to air and use a two steps treatment. The first step will be used to desorb the surface contamination species under vacuum. These ideas are currently in progress. We think also to use atomic oxygen treatments to minimize oxygen vacancies and to limit diffusion toward the interface with Si. In principle, we should not expect any interface reaction since it was demonstrated in literature that Si is stable on LAO.<sup>12</sup>

#### ACKNOWLEDGMENTS

This work was partially supported by the French NANO2008 project and by the European Commission IST Program (“PULLNANO” Project No. IST-026828).

<sup>1</sup>The international Technology Roadmap for Semiconductors, ITRS, 2007, <http://www.itrs.net>.

<sup>2</sup>L. Becerra, C. Merckling, N. Baboux, C. Plossu, O. Marty, M. El-Kazzi, G. Saint-Girons, B. Vilquin, and G. Hollinger, Appl. Phys. Lett. **91**, 192909 (2007).

- <sup>3</sup>X. B. Lu *et al.*, Appl. Phys. Lett. **84**, 2620 (2004).
- <sup>4</sup>C. Merckling, M. El-Kazzi, G. Dalhaye, M. Gendry, G. Saint-Girons, G. Hollinger, L. Largeau, and G. Patriarche, Appl. Phys. Lett. **89**, 232907 (2006).
- <sup>5</sup>C. Merckling, M. El-Kazzi, L. Becerra, L. Largeau, G. Patriarche, G. Saint-Girons, and G. Hollinger, Microelectron. Eng. **84**, 2243 (2007).
- <sup>6</sup>C. Busseret, N. Baboux, C. Plossu, and A. Poncet, Proceedings of SIS-PAD, 2006 (unpublished), p. 188.
- <sup>7</sup>P. Palestri *et al.*, IEEE Trans. Electron Devices **54**, 106 (2007).
- <sup>8</sup>K. J. Yang and C. Hu, IEEE Trans. Electron Devices **46**, 1500 (1999).
- <sup>9</sup>J. Robertson, Rep. Prog. Phys. **69**, 327 (2006).
- <sup>10</sup>L. Yan, H. B. Lu, G. T. Tan, F. Chen, Y. L. Zhou, G. Z. Yang, W. Liu, and Z. H. Chen, Appl. Phys. A: Mater. Sci. Process. **77**, 721 (2003).
- <sup>11</sup>R. Castagné and A. Vapaille, Surf. Sci. **28**, 157 (1971).
- <sup>12</sup>D. O. Klenov, D. G. Schlom, H. Li, and S. Stemmer, Jpn. J. Appl. Phys., Part 2 **44**, L617 (2005).