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Electrical characterisation and predictive simulation of defects induced by keV Si^+ implantation in n-type Si

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In this work, we focused on the analysis of implantation-induced defects, mainly small interstitial clusters (ICs) and {311} defects introduced in n-type Si after ion implantation using deep level transient spectroscopy (DLTS). Silicon ions (at 160 keV or 190 keV) of fluences ranging from $(0.1–8.0) \times 10^{13}$ cm^{-2} have been implanted into n-type Si and annealed at temperatures between 500 °C and 800 °C specifically to create small ICs or {311}s rod-like defects. In samples dominated by small ICs, DLTS spectra show prominent deep levels at Ec − 0.24 eV and Ec − 0.54 eV. After increasing the fluence and temperature, i.e., reducing the number of small ICs and forming {311} defects, the peak Ec − 0.54 eV is still dominant while other electron traps Ec − 0.26 eV and Ec − 0.46 eV are introduced. There were no observable deep levels in reference, non-implanted samples. The identity and origin of all these traps are interpreted in conjunction with recently developed predictive defect simulation models. © *2013 AIP Publishing LLC*.
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I. INTRODUCTION

The continuous scaling down of semiconductor devices requires the optimization of advanced ultra-shallow junction (USJ) fabrication processes. Several challenges have been identified by the International Semiconductor Technology Roadmap (ITRS) in the source/drain (S/D) area.[1] In addition to the well known problems associated to anomalous transient enhanced diffusion (TED), which increases the junction depth and dopant clustering (induced by the high implant doses), the major challenge for future 22 nm CMOS transistors and beyond is represented by the control of the device leakage currents.[1] Source/drain junction leakage is particularly sensitive to implantation-induced extended defects, which may not be fully removed after state-of-the-art low-thermal budget annealing processes, which today include, spike rapid thermal anneal (RTA), flash lamp or laser annealing. In particular, depending on the implantation and annealing conditions interstitial defects can occur in the form of small interstitial clusters (ICs), {311} rod-like defects or circular dislocation loops (DLs).[2] However, the electrical behaviour of these defects has not yet been taken into account in the physical models implemented in technology computer-aided design (TCAD) simulators for the prediction of the leakage currents, explaining why fundamental studies aiming at evaluating their electrical properties are today necessary.

Several studies on the electrical characterization of implantation induced defects have been reported in the past decade, mostly until the end of the 1990s.[3–9,11–17] However, the correlation of energy levels to the extended defects has not been definitely established. For instance, the most dominant level observed by several authors[4,5] in n-types Si samples dominated by ICs has an activation energy in the range E_C – (0.50–0.58) eV (this energy level being close to the mid band gap is therefore a strong candidate for the generation of leakage currents). In particular, Benton *et al.*[4] observed prominent electron traps at E_C − 0.29 eV and E_C − 0.58 eV, after implantation of n-type Si with 1.2 MeV Si ions with a fluence of 1×10^{12} Si cm^{-2} and annealing at temperatures between 500–750 °C for 30 min (defects mainly ICs), and after implanting a higher dose of 5×10^{13} Si cm^{-2} and annealing at temperatures upto 750 °C for 30 min, similar defect levels were also observed. It must be noted that the later implantation conditions results in the transformation of ICs to {311} defects. So far, only Benton *et al.*[5] have attributed a hole trap, E_C – 0.50 eV observed in p-type Si to {311} defects. Finally, Kisielowski *et al.*[6] also observed electron traps with similar activation energies, at E_C − 0.27 eV and E_C − 0.55 eV after plastic deformation of n-type silicon at temperature between 450 °C and 650 °C.

Since then, the energetics, formation, and evolution mechanisms from point to extended defects are now significantly understood.[2,7] It is, therefore, possible to achieve a better understanding of the defect electrical properties by combining deep level transient spectroscopy (DLTS)[8] measurements with atomistic simulations of the defect nature, density, and size.

In this work, DLTS has been used to study the electrical properties of samples containing a controlled population of extended defects introduced by ion implantation into n-type silicon including small ICs and rod-like {311} defects. In particular, we have designed a special test structure that buried and placed the implantation defects within probing range

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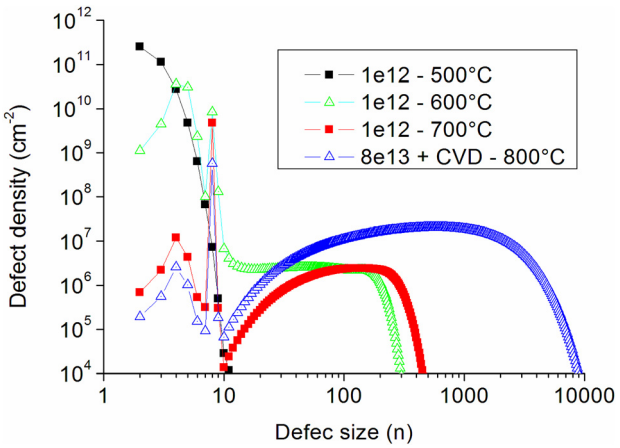

FIG. 1. Defect predictive simulations showing the defect anneal densities as a function of the defect sizes. The transition from IC to {311s} set at size n = 40 atoms.

of the DLTS technique. The DLTS results will be interpreted in conjunction with defect models and recently developed predictive simulations.

II. EXPERIMENTAL PROCEDURE

Phosphorus-doped bulk silicon samples have been implanted with 160 keV or 190 keV Si ions at room temperature. The first set of samples "A1–A3" consists of wafers implanted at LAAS-CNRS with 190 keV Si^+ to a fluence of 1×10^{12} cm^{-2} and annealed for 10 min at temperatures between 500 °C and 700 °C in N_2 gas ambient, placing the defect region at a depth close to the ions projected range ($R_p \sim 0.26$ μm). The uncompensated doping concentration after the implantation and annealing for this set of samples (measured by capacitance-voltage (CV)) is $\sim 1.5 \times 10^{15}$ cm^{-3}. The predicted defect size evolution with these implantation and annealing conditions, depicted in Fig. 1, have been calculated using the "FRENDTECH" defect model.[9,10] The types of defects in this series are mainly the ICs of various sizes. A summary of the defect sizes, and densities listed in Table I, indicating that the quasi-totality of defects in this series (>90%) are mainly of the interstitial (ICs) type. The second series of samples "B1 and B2" were fabricated at IHP Microelectronics, Frankfurt (Oder) and consisted of samples implanted with 160 keV Si ions and fluences of 1×10^{13} Si cm^{-2} or 8×10^{13} Si cm^{-2} followed by the growth of a 1 μm-thick epitaxial layer by chemical vapour deposition (CVD).[11] As detailed in Ref. 11, this special test structure places the implantation defects in the region probed by DLTS and also allows for quality metal-semiconductor Schottky contacts, thereby enabling reliable current-voltage (IV) and DLTS measurements to be performed on the same diode structure. The CVD growth was carried out at a temperature of 800 °C for 10 min, therefore, acting as an annealing step during which the extended defects, mainly rod-like {311} defects are formed as shown in the simulations in Fig. 1 and Table I and verified by TEM analysis.[11] In this case, the implanted ions projected range is $R_p \sim 0.25$ μm therefore after the epitaxial growth, the extended defects are located at 1.25 μm below the semiconductor surface. The implantation and annealing for this set of samples did not modify the initial uncompenstated doping concentration, which was measured on the reference "CVD-only" wafer (cf. Table I) as $\sim 4.0 \times 10^{14}$ cm^{-3}.

The defect simulation for samples B1 and B2 predict that unlike the first samples series, the formed defects mainly consists of {311} rod-like defects with an average size of 1080 and 1604 atoms, respectively. These results clearly show that for low implantation fluence/anneal temperature (e.g., sample A1), only interstitial clusters are formed, whereas for the higher fluence/anneal temperature (sample B2), all the interstitials clusters dissolve and/or transform into larger rod-like {311} defects.[2] In light of the simulation results, for this work, detailed results are presented for samples A2 and B2, and these two samples are throughout this report referred to as "ICs" and "{311}" samples, respectively.

Prior to metallization, the samples were chemically cleaned by a standard cleaning method, i.e., degreasing, then subsequently dipping in H_2SO_4:H_2O_2 (1:1) for 3 min, followed by etching in HF(5%) solution for 30 s before rinsing in de-ionized water and finally drying in N_2 gas. Immediately after the cleaning procedure, a 50 nm thick gold (Au), layer, was evaporated onto the front side of the sample. Standard lithography and gold etching was used to define

TABLE I. Samples details and implantation conditions.

	Sample fabrication						Defect simulations				
	Implantation				Anneals		Defect density				Total nb of atoms in defects
Sample ID	Ion	Em (keV)	Φ (cm^{-2}) ×10^{13}	CVD	T_{CVD} (°C)[a]	T_{anneal} (°C)[b]	Average defect size (nb of atoms)	Defects (cm^{-2})	ICs (%)	{311} (%)	Atoms (cm^{-2})
Reference	…	…	…	Yes	800	…	…	…	…	…	…
A1	Si	190	0.1	No	…	500	2.5	3.95×10^{11}	100	0	9.70×10^{11}
A2	Si	190	0.1	No	…	600	5	8.35×10^{10}	99.5	0.5	4.43×10^{11}
A3	Si	190	0.1	No	…	700	25	5.36×10^{9}	89.7	10.3	1.30×10^{11}
B1	Si	160	1	Yes	800	…	1080	3.70×10^{9}	2.3	97.7	4.00×10^{12}
B2	Si	160	8	Yes	800	…	1604	4.73×10^{10}	1.5	98.5	7.60×10^{13}

[a]Annealing during 1 μm epitaxial layer growth by CVD for 10 min.
[b]Post-implantation anneal for 10 min.

circular Schottky contacts. Silver paste was used as the backside ohmic contact.

Electrical measurements of the samples were performed on a Schottky barrier diode (SBD) structure. The IV measurements were used to monitor the diode qualities and leakage currents, whereas the CV measurements were used to extract the sample free carrier concentrations. The electronic properties of deep levels introduced after the ion implantation and post-implant annealing were characterized by DLTS. The "*signature*" of the observed deep levels (i.e., activation energy for electron emission, E_T, and the apparent capture cross section, σ_a), were determined from Arrhenius plots of $ln(T^2/e)$ vs. 1000/T. Here, e represents the electron emission rate, and T the measurement temperature in Kelvin.

III. RESULTS

A. Deep levels in "ICs" and "{311}" samples

Fig. 2 depicts DLTS spectra of (a) un-implanted sample, and after Si ions implantation with doses of (b) 1×10^{12} Si cm^{-2} and annealed at 600 °C ("ICs" sample) and (c) 8×10^{13} Si cm^{-2} and annealed at 800 °C ("{311}" sample). The reference sample (no implantation and with or without a CVD layer) did not reveal any defect peaks, within our system detection limit ($\sim 10^{11}$ cm^{-3}), as shown in Fig. 2(a). The DLTS spectra of the "ICs" sample (Fig. 2(b)) shows two prominent electron traps, E(0.24) and E(0.54). In this nomenclature, "E" is electron trap, and the number in the brackets is the activation energy for the thermal emission of electrons from the deep level to the conduction band, which may be written as $E_C - 0.24$ eV or $E_C - 0.54$ eV for the two deep levels, respectively. The defects activation energy and apparent capture cross section were extracted from the Arrhenius plots depicted in Fig. 3. It is important to note that this E(0.54) level exhibits similar electrical properties in the two samples, although the nature of the extended defects they contain is very different, as discussed in Sec. II (cf. Table I). In addition, it should be noted that the E(0.54) level is closer to a mid-gap state and, therefore, is a strong

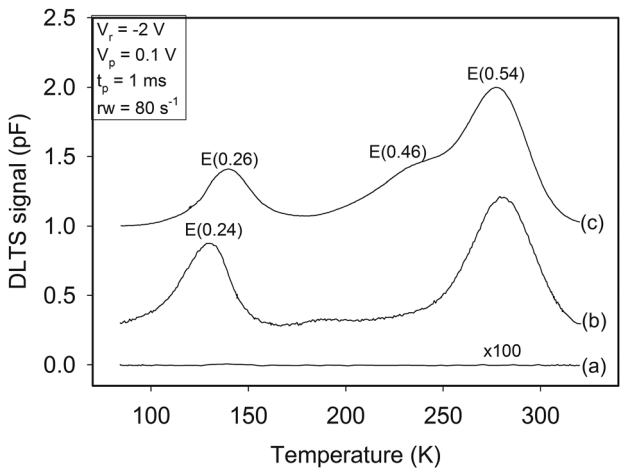

FIG. 2. DLTS spectra of (a) un-implanted sample, and after Si ions implantation with doses of (b) 1×10^{12} Si cm^{-2} and annealed at 600 °C ("ICs" sample) (b) 8×10^{13} Si cm^{-2} and annealed at 800 °C ("{311}" sample). Spectra b and c have been normalized and displaced vertically for clarity.

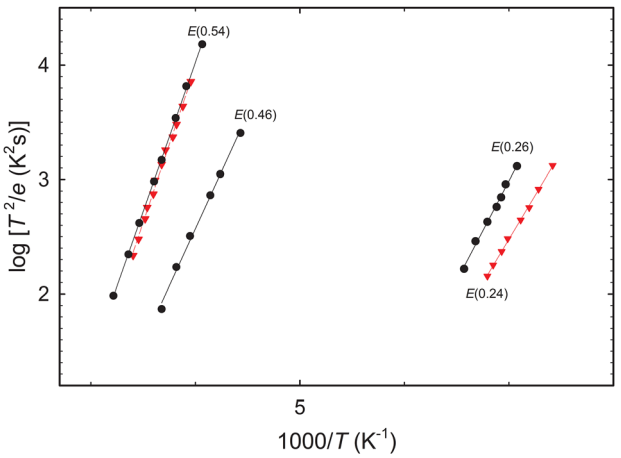

FIG. 3. Arrhenius plots for the defects (shown in DLTS spectra in Fig. 1) which were used to extract the defects activation energies for electrical active defects in "ICs" samples (triangles) and "{311}" samples (circles).

candidate for generation-recombination centers, which are responsible for leakage currents. Annealing studies of the samples containing only ICs ("ICs" sample), showed that the DLTS signal of E(0.54) level annealed-out at 700 °C, whereas in the samples containing only the {311} defects, the level was completely removed after a rapid thermal anneal at 950 °C. Further investigation on this particular defect level will, therefore, be discussed in the next sections.

B. Depth profile of E(0.54) level

The location and distribution of the defects within the depletion width is vital as it may provide clues on the origin of a defect. The depth profiles of dominant level E(0.54) recorded in the low dose "ICs" and high dose "{311}" samples are shown in Fig. 4 (extracted using fixed bias variable pulse method[12]). The defect concentration exhibits a peak at ~ 0.3 μm in the "ICs" sample and ~ 1.25 μm below the semiconductor surface in the {311} sample. These plots closely follow the ion implanted depth profiles, and hence show that these defects are directly related to the implantation damage.

C. DLTS peak broadening analysis

The distinction of a point defect from an extended defect can be derived from DLTS peak broadening analysis. Broadening of DLTS spectra may sometimes be attributed to a distribution of defect energy states (i.e., band-like extended defects) in the Si band gap rather than to field related effects from a single level (non-ideal point defect).[13] It is instructive to point-out here that all the measured deep levels did not exhibit any significant enhancement of the emission rates with electric field, i.e., Pool Frenkel effect,[14] hence eliminating the field related peak broadening effects. Therefore, if the broad peaks in the band gap are not associated to a single level with an activation energy E_0, but to a narrow band of levels that form a Gaussian distribution having a mean value E_0 and with a broadening factor, S, the DLTS signal ΔC can be described as[5,15,16]

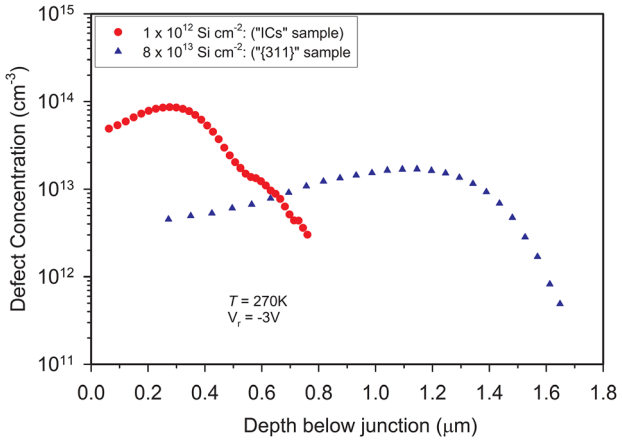

FIG. 4. Defect depth profiles for the electron trap E(0.54) in a "ICs" sample (circles) and a "{311}" sample (triangles) both recorded at T = 270 K. The profiles were recorded at a quiescent reverse bias of −3 V, a varying pulse height (fixed bias-variable pulse method[12]).

$$C(t) = \int_0^\infty g(E) C_o \exp[-e_n(E)t] dE, \tag{1}$$

where C_o is a normalizing factor and $g(E)$ is the broadening function given by[13,16]

$$g(E) = \frac{1}{\sqrt{2\pi S}} \exp\left[-\frac{(E - E_o)^2}{2S^2}\right]. \tag{2}$$

The DLTS spectra in Fig. 2 were simulated in two ways, by (i) a point-like defect model using experimentally extracted activation energy and capture cross section (solid line) and (ii) a defect band model (dashed line) by varying the broadening factor S to fit the experimental data described above. The simulation results of the "ICs" sample are depicted in Fig. 5. It is clear that the experimental DLTS spectra are much broader than expected for point-like defects and can be fit better with the energy band model than point-like defect model particularly for the E(0.54) level, although low temperature side for E(0.24) deviates from this model probably due to another closely spaced defect level appearing on the low temperature side, *albeit* of lower concentration. An S value of 10.0 and 15.5 meV were obtained for the levels E(0.24) and E(0.54) in the "ICs" sample, respectively. Similarly, as shown in Fig. 6, the experimental DLTS spectra for the "{311}" sample are much broader than for point-like defects, and the fitting is improved by assuming an energy spread S of 12.5 and 16 meV for the levels E(0.26) and E(0.54), respectively. The low temperature side of the level E(0.54) is slightly distorted due to the presence of E(0.46) on the shoulder. A summary of the defect electrical properties is listed in Table II. Libertino *et al.*[13] obtained (after ion implantation of p-type Si) an S value of 19.5 and 17 meV for their B-line hole traps B_1 ($E_V + 0.33$ eV) and B_2 ($E_V + 0.52$ eV), respectively, which they attributed to interstitial clusters. Omling *et al.*[15] extracted energy spread S of 22 and 16 meV for the traps "B" line E(0.29) and "D" line E(0.54), respectively, in plastically deformed n-type silicon. Ayres and Brotherton[16] obtained an energy spread S of as high as 35 meV for silicon samples with dislocation loops. Finally, these DLTS simulation results clearly show that the defects measured have a broadening parameter S < 20 meV, which is consistent with results for defect complexes such as ICs rather than dislocation loops, which normally have an S > 30 meV. The assigning of these defects to ICs by the DLTS modeling is further supported by the defect capture kinetics experiments presented next.

There are two distinct defect capture kinetics (i.e., simply the ability of a defect to trap a carrier as a function of time[15]) (a) exponential behavior exhibited by an ideal point defect, i.e., the DLTS signal saturates exponentially with pulse width since only a single carrier can be trapped at each level or (b) fully logarithmic behavior typically for band-like extended defect, in which case the DLTS signal does not saturate but increases logarithmically with an increase in pulse width since such a defect has a band of closely spaced level, which are able to accommodate more than one carrier. The later behavior usually results in the DLTS peak broadening for an extended defect. To extract the capture kinetics of the defects in "ICs" and "{311}" samples, the DLTS signal as a

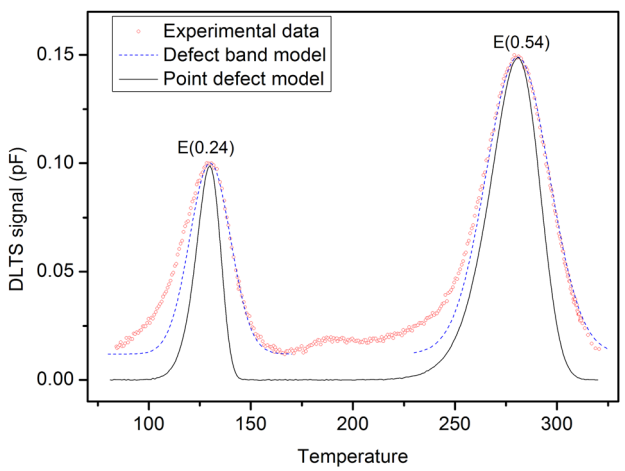

FIG. 5. DLTS spectra of defects in "ICs" sample for experiment data (circles), point-defect simulation (solid line), and defect band simulation (dashed line).

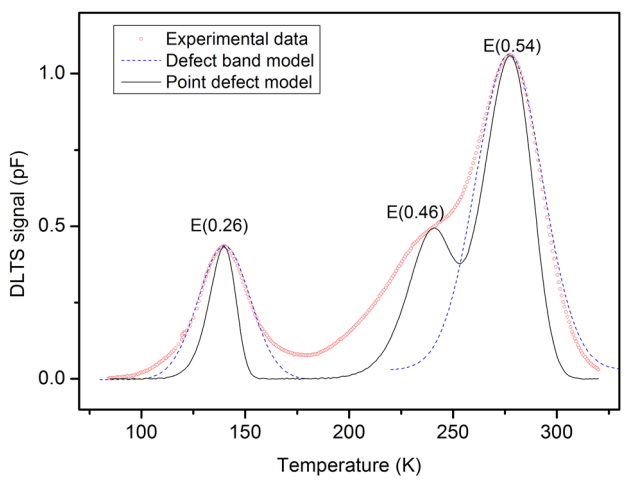

FIG. 6. DLTS spectra of defects in "{311}" sample for experiment data (circles), point-defect simulation (solid line), and defect band simulation (dashed line).

TABLE II. A summary of electronic properties of implantation-induced defects in n-type for the "ICs" sample and "{311}."

	"ICs" sample $\Phi = 1 \times 10^{12}$ Si cm^{-2}/600 °C			"{311}" sample $\Phi = 8 \times 10^{13}$ Si cm^{-2}/800 °C			
Defect ID	E_T (eV)	Φ_a (cm^2)	S (meV)	E_T (eV)	Φ_a (cm^2)	S (meV)	Defect origin
E(0.54)	$E_c - 0.54$	2.3×10^{-15}	15.5	$E_c - 0.54$	2.0×10^{-15}	16.0	ICs or {311} (this work)
E(0.46)	…	…		$E_c - 0.46$	7.7×10^{-17}	20.0	ICs[3]
E(0.26)	…	…		$E_c - 0.26$	4.9×10^{-13}	12.5	ICs[4,5]
E(0.24)	$E_c - 0.24$	4.6×10^{-14}	10.0				ICs[4,5]

function of filling pulse width experiment was performed. The capture kinetics characteristics of deep level E(0.24) and E(0.26) in the "ICs" and "{311}" samples, respectively, are shown in Fig. 7. Both defects exhibit fully exponential kinetics although as discussed before they exhibit DLTS spectra that are broader than for point defect, the origin of this behavior is not yet clear, although we can only speculate that their origins are related to the "smaller" ICs. The capture kinetics characteristics of deep level E(0.54) in the "ICs" and "{311}" samples are shown in Fig. 8. In the "ICs" sample, the capture kinetics can be described by a combination of logarithmic and exponential behaviors. At low filling pulse width (i.e., between 10^{-5} and 10^{-3} s), the DLTS signal is proportional to the logarithm filling pulse width, whereas for longer pulse width, $>10^{-3}$ s, the capture kinetics becomes dominantly exponential and this behavior has been associated with small interstitial clusters.[13,17] To explain this behavior, it is assumed that the defect cluster is bigger than a point defect, hence it can accommodate more than one charge carrier during the trapping process, similar to the extended defect (described by the linear region). Nevertheless, there is an upper limit to the number of carriers that can be trapped by a single level hence the signal eventually saturates at longer pulses (exponential region). In contrast, this same trap level shows a purely exponential capture kinetics behavior in the {311} sample, which is an attribute of point-like defect, however a marginally higher broadening factor of S = 16 meV (probably due to the influence of the shoulder peak at lower temperature side) has also been observed for this defect. The possible origin of this defect in the two samples is further discussed in Sec. IV.

IV. DISCUSSION

The experimental results shown so far clearly indicate that the "ICs" and "{311}" samples analysed in this work exhibit the similar electrical defect E(0.54) level while containing completely different structural defects (small ICs in the low dose sample, {311}s in the high dose one). In particular, the broadening of the DLTS spectrum for this level is similar in the two samples (S = 15.5 meV and 16 meV in the "ICs" and "{311}" samples, respectively, as summarized in Table II). This suggests that the atomic arrangement of atoms in an interstitial cluster and {311}s (or at least of those atoms giving rise to the electrical defects revealed by DLTS) must be very similar. However, a slightly different behavior is observed concerning the electron capture kinetics investigations. In the "ICs" sample, it exhibits a combination of logarithmic and exponential dependence, while in the "{311}" sample, the electron capture kinetics is purely exponential (see Fig. 8). This suggests that the source of the DLTS signal in {311} defects is more "localised" than in small ICs.

We first focus on the observed similarities of the electrical behavior of 311s and ICs. In order to identify a common "structural" origin for the observed electrical defects, we compared in Fig. 9 the defect concentrations obtained in the two investigated samples by DLTS measurements (open circles) with those obtained by defect simulations according to

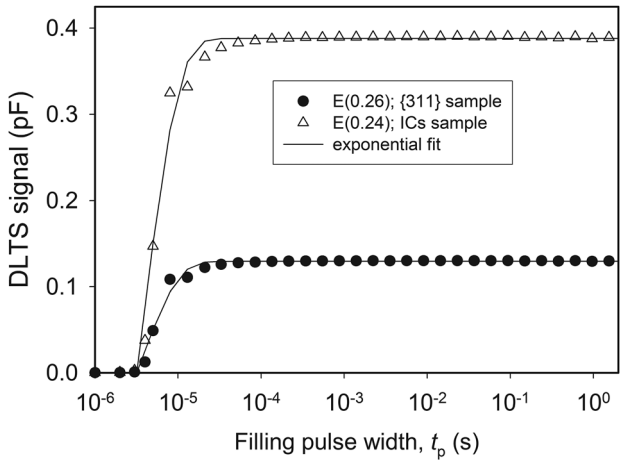

FIG. 7. Capture kinetics for the electron trap level E(0.24) in "ICs" sample (triangle) and E(0.26) in "{311}" sample (circle). The solid lines are the exponential fit for each curve.

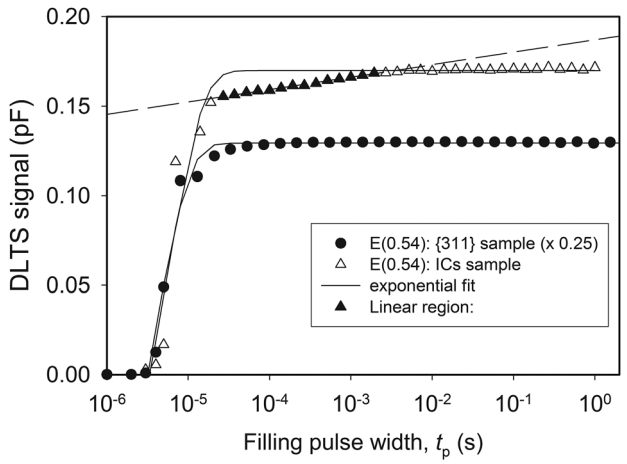

FIG. 8. Capture kinetics for the electron trap level E(0.54) in "ICs" sample (triangle) and "{311}" sample (circle). The solid lines are the exponential fit for each curve and the dashed line is the linear fit.

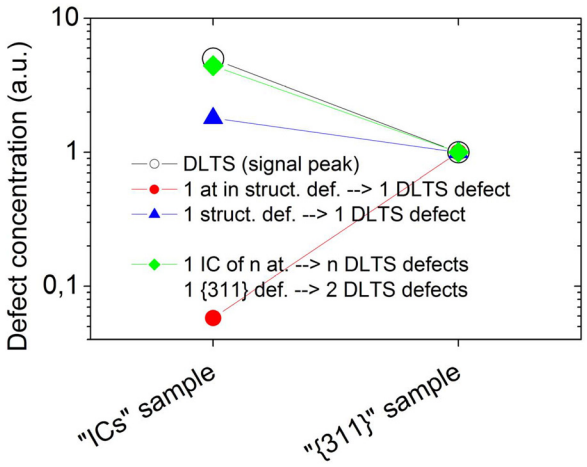

FIG. 9. Defect concentrations obtained in the "ICs" and "{311}" samples by DLTS measurements (open circles) or obtained by defect simulations according to different assumptions (filled symbols). The data are normalised with respect to the defect concentration in the "{311}" sample.

different assumptions (filled symbols). Because of the uncertainties related to the DLTS concentration values close to the surface region in Fig. 4, we have used the peak concentration value for the DLTS results (expressed in cm^{-3}) for the comparison, while the results of the defect simulations are expressed in cm^{-2}. We, therefore, normalised each data set with respect to the defect concentration in the "{311}" sample to simplify the comparison. The DLTS measurements indicate that the peak concentration of electrically active defects in the "ICs" sample is 5 times higher than in the "{311}" sample (open circles in Fig. 9). If we make the assumption that each Si interstitial atom contained in the defect complexes (ICs or {311}s) is electrically active, i.e., it gives rise to the dominant level E(0.54) defect, then defect simulations (cf. Table I) predict that the DLTS signal in the "{311}" sample should be almost 200 times higher than in the "ICs" one (Fig. 9, filled circles), which is in complete disagreement with the DLTS data. This suggests that the number of electrically active centers associated to a given {311} defect must be much smaller than the number of atoms it contains. Indeed, the proposed models for the {311} defect structure[18,19] along the defect length have no dangling bonds. Although this is easily understandable for the atoms located in the core of the defect, it is expected that at least the defect short edges, which are the preferential sites for the capture and emission of Si interstitial atoms during the defect growth, should exhibit some electrical activity. As a consequence, we considered as a second working hypothesis that each {311} or ICs structural defect introduces one DLTS defect, i.e., it is electrically active "as a whole." We therefore reported in Fig. 9 (filled triangles) the total number of defects (ICs or {311}s) that are predicted by defect simulations shown in Fig. 1. In this case, the defect concentration ratio between the two investigated samples (~2) is much closer to the one experimentally found by DLTS (~5) compared to the previous case, confirming that, to a first approximation, the structural defects are indeed electrically active "as a whole." Although the various uncertainties related to the DLTS measurements, as well as the method we used for the comparison of DLTS data with simulations of defect formation, do not allow to reliably push this analysis further, it is tempting to test a final assumption where each {311} defect provides 2 DLTS active centers (one per each defect edge), while small ICs (with an average size of 5 atoms) would provide as many DLTS centers as the number of atoms they contain, all of them being assumed to be "on the periphery" of the defect. The resulting "active" defect concentrations are reported in Fig. 9 (diamond), which are in a very good agreement with the DLTS data.

In fact, this last hypothesis, in addition to allowing an explanation for concentration values of the DLTS defects, also provides a possible explanation for the different behavior of the capture kinetics analysis exhibited by the two defects, i.e., slightly delocalized energy states (a combination of linear and exponential capture kinetic profile) for the "ICs sample" compared to the exponential signal from the {311} sample. Indeed, when considering that in the "ICs sample" contains only interstitial clusters, and because of the number of atoms around the cluster they can accommodate a number of electrons, but there is a limit to the number charges it can accommodate hence the signal eventual saturates during the filling process.[13] In contrast, if we assume for {311} defects that the DLTS signal only originates from the two short defect edges, which are the preferential sites for the capture and emission of Si interstitial atoms during the defect growth, then only a fewer atoms can be involved in the trapping process and it behaves like a quasi-point defect, consequently there is no logarithmic electron capture region.

V. SUMMARY

The ion implantation of n-type silicon with low (1×10^{12} Si cm^{-2}) to high (8×10^{13} Si cm^{-2}) and annealed upto 800 °C introduced a common deep level close to the middle of Si band gap, Ec – 0.54 eV (E(0.54)). In the samples containing only ICs, all the DLTS signals were annealed out at 700 °C, whereas in the samples containing only the {311} defects, the DLTS signals were completely removed after a rapid thermal anneal at 950 °C.

The E(0.54) defect is therefore associated to both interstitial clusters and {311} rod-like defects. The comparison between DLTS data and defect simulations allows us to conclude that, in the upper part of the Si bandgap, there is no peculiar deep level associated to either small ICs or larger {311}s. Instead, they both introduce a similar deep level located at Ec – 0.54 eV, whose concentration is closely related to the density of the formed defects. Based on the comparison between DLTS data and defect simulations, it is concluded that the concentration of E(0.54) defects is closely related to the density of the existing structural defects (interstitial clusters or {311}s), rather than to the number of Si interstitial atoms they contain, i.e., the structural defects are electrically active "as a whole."

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[1]See http://www.itrs.net/ for more information about International Technology Roadmap for Semiconductors.
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